Features

- **DAVIC/DVB®/ETS300.429 / ITU-T J.83 annex A, C Fully Compliant**
- **Direct IF Sampling (No Second IF Down Conversion Required) or Baseband Input**
- **Internal A/D Converter or possibility to use external A/D**
- **Internal DC Offset Compensation**
- **1024, 512, 256, 128, 64, 32, 16 QAM and QPSK Demodulation**
- **Roll-off Factor Adapted to Raised Cosine Filtered Signal (0.11 to 0.4)**
- **Fully Digital Timing Recovery**
- **Variable Symbol Rate Recovery**
- **Anti-aliasing Continuously Variable Digital Filtering with Symbol Rate Adaptive Bandwidth (1 to 18.75 Mbaud at the Same Sampling Frequency)**
- **Fully Digital Carrier Recovery (Coherent or Differential for QPSK)**
- **Robust Equalizer Acquisition**
- **Selectable Transversal or Decision Feedback Equalizer**
- **Dual Phase/Frequency Offset Recovery up to 12% of the Symbol Rate with No Degradation**
- **MPEG2 Frame Synchronization**
- **Reed Solomon Decoder (204, 188, 8)**
- **De-interleaving (I = 12 and I = 17)**
- **Energy Dispersal De-scrambling**
- **I^2C Interface - Switch for Separate Bi-directional I^2C Bus to Tuner to Avoid Phase Noise Problems Due to I^2C**
- **Integrated Clock Reference for Tuner, Especially Designed for NIU in CAN**
- **Two AGCs: Analog and Digital Gains**
- **3 Program Identifier (PID) Filtering**
- **IRQ Interrupt Request Generation to Simplify Monitoring**
- **Bit Error Rate and Packet Error Rate Monitoring**
- **Signal to Noise Ratio Estimation, Residual Phase Noise Estimation**
- **Automatic Spectrum Inversion**
- **JTAG Support**
- **0.35 micron CMOS Technology, 3.3 V Operation**
- **100-pin TQFP Package**

Description

The AT76C651 is a DVB compliant Quadrature Amplitude Modulation (QAM) demodulation circuit which can be used in DVB and other applications using Quadrature Phase Shift Keying (QPSK) or QAM transmission systems. The signal, after output from tuner and adjacent channels rejection filter, enters the analog input to the QAM demodulator device at IF frequency (either around 7-10 MHz or around 36-44 MHz by using down sampling).

The signal is converted to digital format, and goes through several processing steps required for demodulation: Automatic Gain Control, Baseband Down Conversion, Timing Recovery with Anti-aliasing Filtering, Squared Root Raised Cosine Receive Filtering, Carrier Recovery and Digital Gain Control, Equalization (Linear and Decision Feedback Dual Structure). The output from demodulation then goes through Forward Error Decoding: DVB/DAVIC de-mapping, frame synchronization, de-interleaving, Reed-Solomon decoding, spectrum de-randomization. The output before decoding may also be output directly for use with post-processing devices in applications other than DVB.

An additional block situated in the back-end may be used to filter out programmable PIDs, which provides additional flexibility in interactive solutions or DVB data-broadcast PC receive cards. It is especially designed for modem implementations with a 24-bit mask on 1 PID (Medium Access Control) and can be used for return channel implementation.

Digital Reception/ Transmission IC

AT76C651 Integrated DVB Compliant QAM Demodulator

Preliminary

DVB® Digital Video Broadcasting

Rev. 1293A–04/99

Figure 1. Symbol of the AT76C651 QAM Demodulator

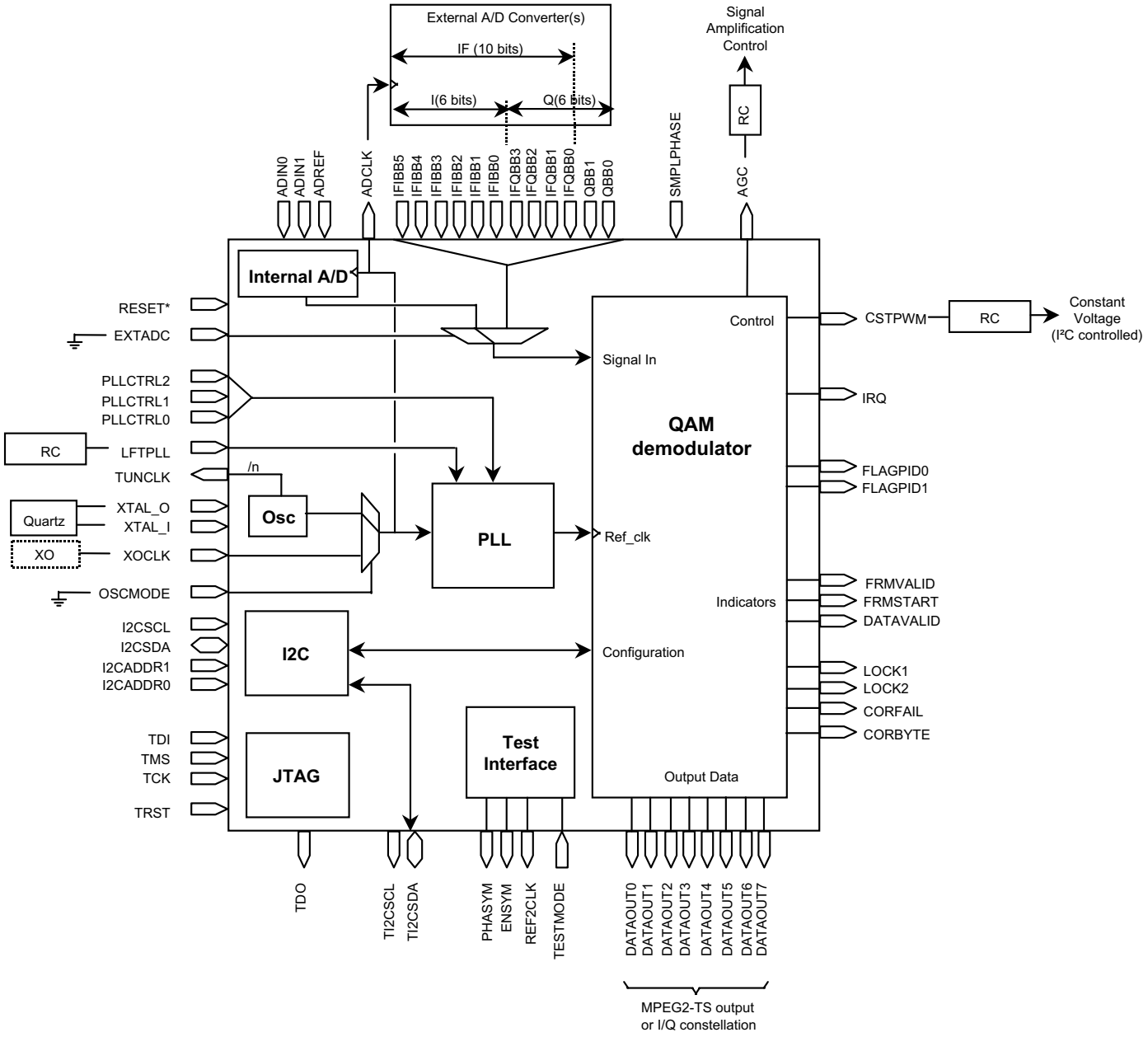


Table 1. Signal Description

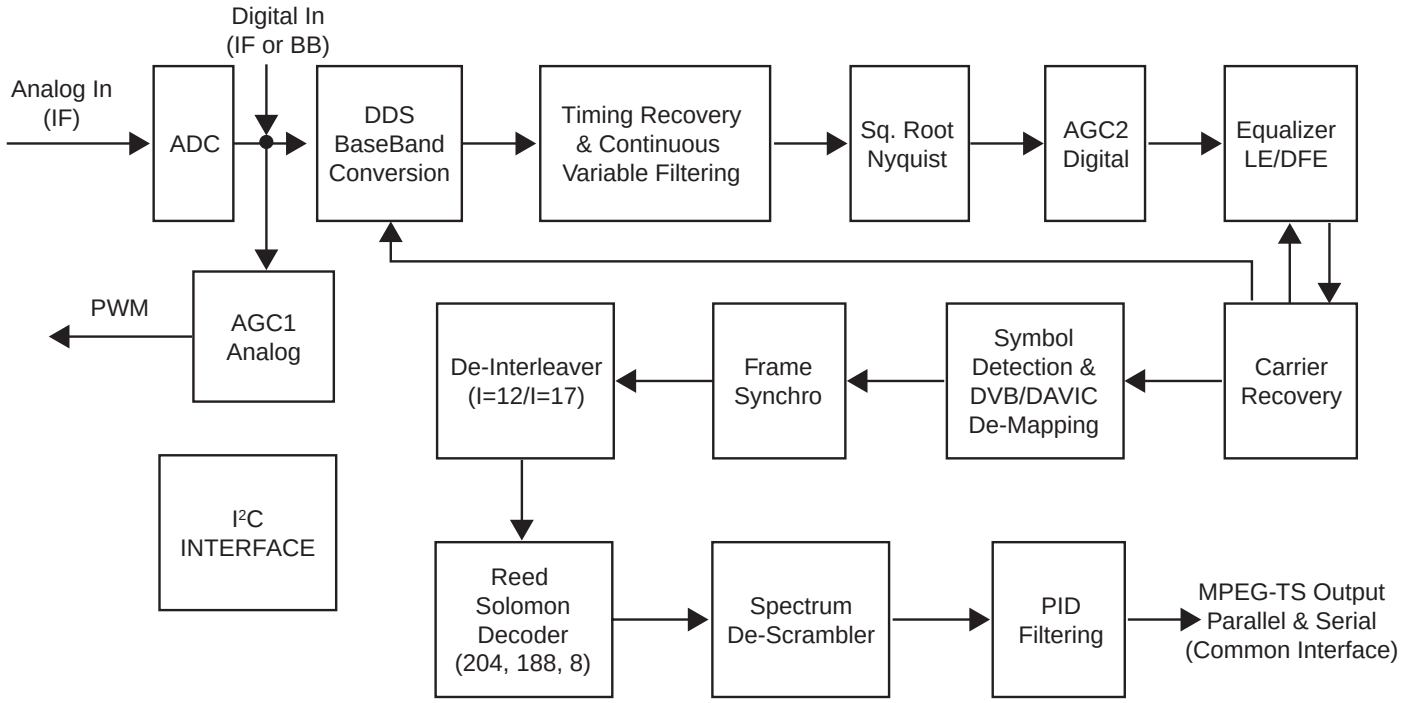
Signal Name	Function	Number of I/Os	Direction
ADIN	IF analog input to A/D converter	2	A
I2CADDR	I^2C circuit address selection	2	I
I2CSDA	SDA line of I^2C	1	I/O
I2CSCL	SCL line of I^2C	1	I
TI2CSDA	I^2C bus data line SDA to/from tuner through bi-directional switch	1	I/O
TI2CSCL	I^2C bus clock SCL to tuner through switch	1	O
IFIBB	IF 6 MSBs (A/D bypass) or I -baseband digital input	6	I
IFQBB	IF 4 LSBs (A/D bypass) or Q-baseband digital input 4 MSBs	4	I
QBB	Q-baseband digital input (2 LSBs)	2	I
PLLCTRL	PLL division/bypass control	3	I
XOCLK	Crystal oscillator input	1	I
XTAL_I	Crystal input	1	I
XTAL_O	Crystal output	1	O
OSCMODE	Oscillator input mode (0 for crystal, 1 for XO)	1	I
LFTPLL	Low pass filter input to PLL	1	A
EXTADC	Internal A/D enable	1	I
ADREF	Reference A/D voltage	1	A
ADIN1	Positive IF analog input A/D converter	1	A
ADIN0	Negative IF analog input A/D converter	1	A
ADCLK	Sampling clock for external A/D	1	O
SMPLPHASE	External A/D sampling phase	1	I
TDI	JTAG	1	I
TDO	JTAG	1	O
TMS	JTAG	1	I
TCK	JTAG	1	I
TRST*	JTAG	1	I
DATAOUT	MPEG2-TS parallel byte <0:7> or Serial bit stream output <0>	8	O
CORFAIL	RS packets not corrected	1	O
CORBYTE	Corrected byte indicator	1	O
DATAVALID	MPEG2-TS byte or bit output enable	1	O
FRMSTART	Start of MPEG2-TS frame	1	O
FRMVALID	Valid MPEG2-TS frame control in parallel mode output	1	O
FLAGPID	PID filtering Indicator	2	O
IRQ	Interrupt request	1	O
LOCK1	Maskable lock signal 1	1	O
LOCK2	Maskable lock signal 2	1	O
CSTPWM	Configurable value output with PWM	1	O

Table 1. Signal Description (Continued)

Signal Name	Function	Number of I/Os	Direction
AGC	Analog automatic gain control PWM	1	O
TUNCLK	4 MHz reference oscillator output to tuner	1	O
REF2CLK	Half digital clock	1	O
PHASYM	Test output signal	1	O
ENSYM	Test output signal	1	O
Power Supply			
GND	Ground		Gnd
I2CGND	I^2C ground		Gnd
ANAGND	A/D converter ground		Gnd
VDD	+3.3 V supply		Pwr
I2CVDD	I^2C power supply		Pwr
ANAVDD	A/D converter power supply		Pwr
Reset			
TESTMODE	Test pin	1	I/O
RESET*	Hard reset of circuit	1	I

All parameters identified by (*) are active low.

Figure 2. Block Diagram of the AT76C651



Functional Description

The following sections describe the main functions of all blocks included in the AT76C651 QAM demodulation IC.

A/D Converter (ADC)

An analog to digital converter (maximum sampling frequency 30 MHz, maximum signal frequency 70 MHz) is integrated into the device. It samples the IF input, producing a digital spectrum around Fo (and its images). The sample and hold operates at frequencies up to 75 MHz, thus enabling sub-sampling capability for signals at IF frequency up to about 70 MHz.The A/D converter is only usable when the signal is in IF frequency. In this case, inputs IFIBB, IFQBB and QBB should be pulled down to Ground.

It is also possible to use a 10-bit external A/D in case of a signal in IF frequency. Then the sampling clock of the A/D must be taken on pin ADCLK of the chip. The digital outputs of the external A/Ds must connect input IFIBB5 to IFIBB0 and input IFQBB3 to IFQBB0 (MSB to LSB). The pin SAMPLEPHASE can be used to select the phase of the internal A/D resampling clock, depending on the external A/D propagation delay (see waveforms in Appendix).

In case of a signal in baseband, two external 6-bit A/Ds must be used. The sampling clock of the A/Ds must be taken on pin ADCLK of the chip. The digital outputs of the A/Ds must connect input IFIBB5 to IFIBB0 for I input, input IFQBB3 to IFQBB0 and QBB1 to QBB0 for Q input (MSB to LSB). SAMPLEPHASE should be connected as decribed in the previous paragraph.

D/C Offset Control

An internal DC-offset compensation is done on the I and Q baseband signals in order to compensate potential offsets created by external A/D converters, if an internal A/D is not used.

Direct Digital Synthesizer (DDS) - Coarse Tuning

An IF to baseband conversion from Fo is then performed. The frequency Fo is configurable which reduces the constraint on the relation between the SAW filter center frequency and the chip oscillator. The frequency of the DDS is further adjusted by the carrier frequency recovery in order to adjust exactly the received spectrum to the receive filter.

“Analog” Automatic Gain Control (AGC1)

The signal level at the ADC input is adjusted through a first AGC loop. The power estimation block estimates the signal level at the output of the ADC, compares it to a given level and generates a Pulse Width Modulation (PWM) signal which controls the analog gain. The PWM output generates a very stable control, since power estimation is done by digital loop control, only the output is given in PWM format for simpler implementation on board (only an R-C filter with about 5 KHz cut-off bandwidth is required). The power estimation is made over the entire signal sampled by the ADC, thus including the adjacent channels and the target signal. This ensures that no analog saturation can happen due to the AGC feedback.

Also, the power estimation of the analog gain control can be used in conjunction with the AGC2 level (which indicates the power of the QAM signal only) in order to compute the power of adjacent channels. This may be used to adjust the takeover point (TOP) of external amplifiers when several amplifiers are required on the board (typically in the tuner and after the SAW filter). Note that an I^2C controllable PWM is available for this purpose.

Digital Timing Recovery

The baseband conversion output is then fed to the timing recovery block. This block integrates a digital timing loop which estimates the best resampling time. This information is provided to a time continuous filter which interpolates the baseband signal and produces QAM symbols at the recovered symbol rate.

The interpolating filter main property is its continuously autoadaptive bandwidth, which allows the demodulator to recover a wide range of symbol rate 1/Ts, with the same perfomance, and avoids signal aliasing during resampling operation.

Square Root Raised Cosine Nyquist Receive Filter (SRRC)

The SRRC filter, with roll-off factor allowing demodulation of Raised Cosine transmitted signals from 0.11 to 0.4, receives the signal from the timing recovery output and ensures an out-of-band rejection higher than 43 dB. This significant rejection increases the back off margin of the receiver against adjacent channels.

Digital Automatic Gain Control (AGC2)

The internal digital AGC performs a fine adjustment of the signal level at the equalizer input. This AGC only takes into account the QAM signal itself, since adjacent channels have been filtered out by the SRRC, and thus compensates digitally the analog AGC which may have reduced the input power due to adjacent channels.

Equalizer

The equalizer is based on algorithms which provide blind and robust acquisition. The equalizer compensates for the different impairments encountered on the network. Two equalizer structures can be selected: Transversal (powerful for long echoes) or Decision feedback (powerful for strong short echoes).

The equalizer central tap position is configurable. This allows an optimal compensation for post and pre-cursor echoes. The equalizer comprises 32 taps which represents a length of about 6.2 microseconds at 5 MBauds. This allows a large compensation for echoes with significant delays, and a total compensation for significant (small attenuation) short echoes.

Carrier Recovery - Fine Tuning

The carrier recovery block allows the acquisition and tracking of a frequency offset as high as 12% of the symbol rate, even for low signal to noise ratios. The phase comparator algorithm provides a high phase noise tolerance which reduces the tuner cost. The frequency offset recovered by the chip can be monitored through the I^2C interface. This information can be used to readjust the tuner frequency in order to reduce the analog filtering degradation on the signal and thus improves the Bit Error Rate. This information is also provided automatically to the DDS in order to recover the frequency with complete accuracy before receive filtering.

Differential Demodulation for QPSK.

A differential demodulation can be used in strongly distorted environment in the case of differentially encoded QPSK demodulation. This mode provides a stronger robustness against phase noise but reduces the performance of the receiver by 3 dB, as shown in theory. I^2C register QAMSEL must be configured to set this mode.

Phase and Additive Noise Estimation

Phase noise and additive noise estimations are performed. This information can be used to select the best carrier loop bandwidth giving the best trade off between phase noise and additive noise. The phase noise can come from the tuner and (or) the LNB in MMDS application. This feature can also be used to remotely monitor the various problems encountered by a STB or cable modem at the user installation.

Symbol Detection and DVB/DAVIC Demapping

The output is fed to the symbol threshold detector, then to the differential decoder, and finally to the DVB or DAVIC de-mapper which produces the recovered bit stream sent to the Forward Error Correction (FEC).

Frame Synchronization

The first function performed by the FEC is the frame synchronization. The bit stream is decomposed into packets of 204 bytes at the output starting with a frame synchronization word.

De-interleaving

The packets are then de-interleaved. Two depths can be selected for the interleaver: 12 (DVB/DAVIC) and 17. The depth 17 increases the robustness of the system against impulse noise, but assumes the signal has been interleaved with the same value at the modulator.

Reed-Solomon Decoder

The de-interleaved output is sent to the Reed Solomon (RS) input which performs a correction of a maximum of 8 errors (bytes) per packet. The RS also provides other information regarding the uncorrected packets and the position of the corrected bytes in the packet if there are some.

Spectrum De-scrambler

After RS decoding, the packets are de-scrambled (for energy dispersal removal).

PID Filtering

A Program Identifier (PID) filtering can be performed on the MPEG2 Transport Stream (TS) before feeding the packets to the output. Three PIDs can be selected at the same time. This block outputs an enable signal on the packet stream that goes to the component interfaced with the QAM demodulator. This provides an interesting feature for on board PC implementations, where either data or video and audio are processed directly by the PC processor. A mask is provided for one of the PIDs, offering a filter on the overall MPEG-TS packet header.

Note that one of the PIDs can be selected, so that a special Enable output can be used to filter out all MPEG-TS packets containing MAC messages (for In Band return channel implementations of the DVB-RC specification). This stream contains all the control information for the return channel, and is required by other components used for the return channel.

Interrupt Request (IRQ)

An interrupt request can be generated by the AT76C651 device when configurable events occur. This is controlled by the I2C register IRQMASK and OUTPUTCFG.

MPEG2-TS Output Interface

The output of the FEC is constituted of MPEG2 Transport Stream (TS) packets. The output can be either parallel or serial on DATAOUT. The data is present on either edge or low state of the DATAVALID pin in output mode. In serial output mode DATAOUT (7) to DATAOUT (1) are individually valid with each bit output in serial mode (see “Timing Waveforms” on page 32).

Oscillator and Phase-Locked-Loop

The fully digital clock and carrier recovery eliminates the need to implement external VCOs and VCXOs and thus reduces the total function cost. Only a simple crystal oscillator is needed by the chip to perform all the demodulation functions with variable symbol rate.

Either a crystal can be connected to the XTAL_I and XTAL_O pins of the chip with frequency:

$$25MHz \le f_{XTAL} \le 30MHz$$

or a crystal oscillator (XO) can be connected directly to the XOCLK input pin, with frequency:

$$f_{XTAL} \le 80MHz$$

In case of a crystal, the OSCMODE pin is connected to GND. In case of an XO, it must be connected to VDD.

The crystal must be first order, serial resonance and have a load capacitance of 10 pF.

The internal oscillator of the chip provides a direct jitter-free clock used to sample the input signal of internal or external A/D. For external A/D , this clock is available on the output pin ADCLK.

The internal reference clock of the chip is generated by using an internal PLL and its frequency is given by:

$$f_{REF} = \frac{n}{2} f_{XTAL} \qquad with \qquad n = 2, 4, 5, 6, 7$$

The frequency f_{REF} is the maximum output bit rate supported by the device and must be less than 80 MHz (see “Symbol Rate” on page 12). The value *n* is configured by the PLLCTRL2, PLLCTRL1, and PLLCTRL0 input pins, as shown in the following table.

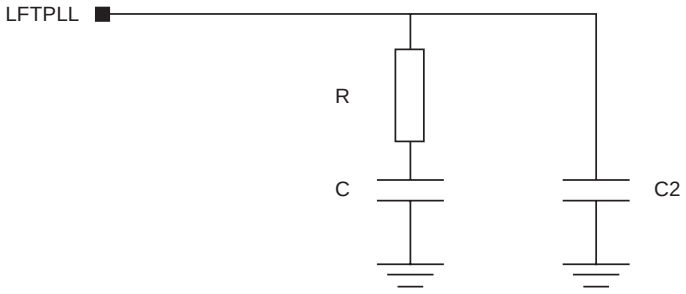
Table 1.

	PLLCTRL2	PLLCTRL1	PLLCTRL0
n = 2	1	0	0
n = 4	0	0	0
n = 5	0	0	1
n = 6	0	1	0
n = 7	0	1	1

The value n = 2 allows to input directly the reference clock at frequency f_{REF} (bypass the PLL).

The PLL pin LFTPLL must be connected to an R-C filter as shown in Figure 3. Values of resistance and capacitors should be R = 100 Ω, C = 10 nF, and optionally C2 = 2.2 nF.

Figure 3. RC Filter Connection to PLL Input of Device



Half the frequency of the reference clock generated by the internal PLL is sent to the output pin REF2CLK. A separate TUNCLK output pin provides a fraction of the crystal frequency given by:

$$f_{TUNCLK} = \frac{1}{p} f_{XTAL} \qquad with \qquad p = 2, 4, 8$$

which can be used as a reference for the tuner oscillator or any other reference frequency on the board. The value p is configured by the I^2C register OUTPUTCFG (see annex).

JTAG

A JTAG controller compatible with IEEE Std 1149.1 is provided in the device. The pin TRST* must be connected to a pull down on the board in order to have it connected to GND during functional operation of the chip. The JTAG provides a boundary scan chain on the pinout of the chip. The following instructions are available:

- BYPASS: the chip remains in functional mode and a single BYPASS register is connected between TDI and TDO. The bit code of this instruction is 11.
- SAMPLE/PRELOAD: the chip remains in functional mode and the boundary-scan register is connected between TDI and TDO. The bit code of this instruction is 01.
- EXTEST: the chip is in external boundary-test mode and the boundary-scan register is connected between TDI and TDO. The bit code of this instruction is 00.
- IDCODE: the chip is in functional mode and the device identification register is connected between TDI and TDO. The bit code of this instruction is 10.

The device identification register is 32-bits long and contains the value 0x00280B8F.

Special I/O Description

Special I/Os that are not described elsewhere in this specification are described in this section.

- ADIN0, ADIN1, ADREF: Analog input for IF signal input. ADIN0 and ADIN1 are current driven differential inputs of the signal. ADREF is a reference signal fixed internally by the chip.
- OSCMODE: when set to ‘1’, a crystal oscillator is used. When set to ‘0’, a crystal is used.
- TEST: Three test pins are available on the chip for testing.
  - TESTMODE: input test pin, connected to GND
  - PHASYM: output test pin, not connected
  - ENSYM: output test pin, not connected
- REF2CLK: clock output test pin, not connected

I²C Control

The chip is entirely controlled via an I²C interface. The chip address can be modified by connecting the ADDI2C pins to GND or VCC to select the two LSBs of the address. The chip address is:

0	0	0	1	1	ADDI2C(1)	ADDI2C(0)

I²C Write Mode

Registers can be written using a standard I²C bus with clock SCL and data SDA as described by - *The I²C-bus and how to use it - Philips Semiconductors - April 1995* -. The protocol used to write into I²C registers is described by the frame shown below.

Table 2.

S	chip address	0 (Write)	A	register address	A	data 1	A	...	data n	A	P

S: Start

A: Acknowledge bit

P: Stop

to chip
from chip

- data 1 is written at register address
- data 2 is written at register address + 1
- ...
- data n is written at register address + (n-1)

It is therefore possible to configure several successive registers with a single I²C frame (from first Start to Stop).

I²C Read Mode

Register values can be read from the chip by transmitting the following frame on the I²C bus.

Table 3.

S	chip address	0 (Write)	A	register address	A	S	chip address	1 (Read)	A	data X1	A

Table 4.

S	chip address	1 (Read)	A	data X2	A	...	S	chip address	1 (Read)	A	data Xn	A	P

- data X1 is read from register address
- data X2 is read from register address+1
- ...
- data Xn is read from register address + n-1

It is therefore possible to read from several successive registers with a single I²C frame (from first Start to Stop). Note that multiple byte registers must be read MSB / low address first. All LSBs of the complete data are only memorized at the time when MSBs are read and do not change during readings of LSBs.

Switch for Tuner I²C Bus

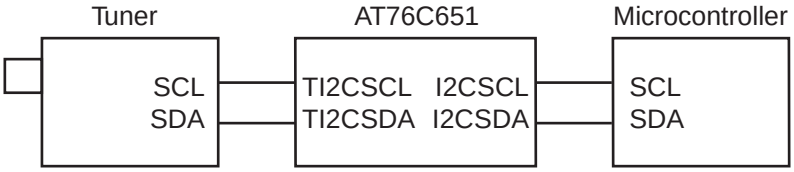
In order to avoid phase noise created by the I²C bus on the tuner, an active bidirectional switch provides a separate I²C bus for tuner configuration.

For this purpose, the I²C bus to the tuner must be connected to the AT76C651 TI2CSCL and TI2CSDA pins (see Figure 1). The I²C register called TUNI2CADD (see I²C registers table) must be configured with the I²C address of the tuner. The switch between the normal I²C bus and the tuner I²C bus can be enabled or disabled using the LSB of TUNI2CADD.

When disabled TI2CSCL/TI2CSDA lines are isolated from I2CSCL/SI2CDA.

When enabled, the switch copies SDA to (resp. from) TSDA when data is transmitted to (resp. from) the tuner. The switch should be enabled by the microcontroller only when the tuner is being configured.

Figure 4. I²C Connection between AT76C651 and Tuner



Automatic Configuration

In order to configure the chip, the following actions are required:

- Hard reset of chip
- Configure registers SYMRATE (Symbol rate), QAMSEL (QAM modulation type) and BBFREQ (IF frequency)
- Write value 0x01 into SETAUTOCFG in order to configure automatically all other registers
- Optionally modify some register values, if required
- Write value 0x01 into RESTART in order to restart the chip with the new values

The automatic configuration of all registers as a function of the QAM modulation, symbol rate and IF frequency offers a very simple use of the chip with a basic software driver.

Table 5. I^2C Registers List

Address	R/W	Name & Function	Meaning
General			
0x00 to 0x02	W/R	SYMRATE	Symbol rate
0x03	W/R	QAMSEL	QAM selection (and mapping type, DVB and others)
0x04 - 05	W/R	BBFREQ	IF input frequency
0x06	W	SETAUTOCFG	Sets automatic configuration of all parameters (see *)
0x07	W	RESTART	Restart chip without modifying configuration parameters
0x08 (*)	W/R	OUTPUTCFG	Select MPEG2 or other internal signals for test output
0x09 (*)	W/R	MASKLOCK1	Mask for lock 1 signal output
0x0A (*)	W/R	MASKLOCK2	Mask for lock 2 signal output
0x0B (*)	W/R	IRQMASK	Events Mask for Interrupt Request generation
0x0C (*)	W/R	TUNI2CADD	Tuner I^2C address for use of specific tuner I^2C bus
0x0E - 0x0F	R	CHIPID	Chip ID and version
Baseband Conversion and AGC1			
0x13(*)	W/R	AGC1NMIN	Minimum value authorized for AGC value
0x14(*)	W/R	AGC1NMAX	Maximum value authorized for AGC value
0x15(*)	W/R	BBCFG	General configuration of Baseband block
0x17(*)	W/R	CSTPWM	Constant value for PWM output
0x19	R	BBTOPCNT	A/D saturation rate over 16384 successive samples
Timing Recovery			
0x23 - 0x24 (*)	W/R	TIMLOOPCFG	Configuration of initial loop parameters
0x29	R	TIMLOOPMONIT	Variable loop bandwidth value
Carrier Recovery			
0x31(*)	W/R	CARALPHAACQ	Alpha parameter of loop bandwidth during acquisition phase of carrier
0x32(*)	W/R	CARBETAACQ	Beta parameter of loop bandwidth during acquisition phase of carrier
0x33(*)	W/R	CARALPHATRACK	Alpha parameter of loop bandwidth during tracking phase of carrier
0x34(*)	W/R	CARBETATRACK	Beta parameter of loop bandwidth during tracking phase of carrier
0x39 - 0x3B	R	CARCONST	Constellation points after carrier recovery
AGC2			
0x42(*)	W/R	AGC2CFG	AGC2 configuration
0x43 - 0x44(*)	W/R	AGC2INIT	AGC2 initial value
Equalizer			
0x51(*)	W/R	EQUCFG	Equalizer configuration
0x52(*)	W/R	EQUCENTRAL	Central tap configuration
0x53(*)	W/R	EQUTAPTORD	Coefficient to monitor
0x54 - 0x55	R	EQUTAPREAL	Real part of selected tap

Table 5. I^2C Registers List

Address	R/W	Name & Function	Meaning
0x56 - 0x57	R	EQUTAPIMAG	Imaginary part of selected tap
FEC			
0x60(*)	W/R	FECIQINV	I/Q invert mode
0x61(*)	W/R	FECFLEN	Frame length
0x62(*)	W/R	FECFSW	Frame Synch Word
0x63(*)	W/R	FECDILVILEN	Number of branches in interleaver
0x64(*)	W/R	FECDILVMLEN	Memory step size of interleaver
0x65(*)	W/R	FECDINH	FEC inhibitions configuration
PID Filtering			
0x70 - 0x71(*)	W/R	PID1	First PID filter
0x72 - 0x73(*)	W/R	PID2	Second PID filter
0x74 - 0x76(*)	W/R	PID3	Third MPEG-TS header filter
0x77 - 0x79(*)	W/R	PIDMSK3	Mask for third MPEG-TS header filter
General Monitoring			
0x80	R	LOCK	Lock status of AGC1, AGC2, TIMING, CARRIER, EQUALIZER, FEC
0x81 - 0x83	R	BER1	Bit error rate estimate
0x84	R	BER2	Bit error rate estimate based on frame synchronization word
0x85	R	NPERR	Number of uncorrectable frames
0x86 - 0x88	R	TIMFREQOFF	Symbol rate frequency offset with respect to SYMRATE
0x89 - 0x8A	R	DDSFREQOFFSET	Frequency offset recovered by DDS
0x8B - 0x8C	R	CARFREQOFFSET	Residual frequency offset (normalized to symbol rate)
0x8D - 0x8E	R	PHASENOISE	Phase noise estimation
0x8F - 0x90	R	ADDITIVENOISE	Additive noise estimation
0x91	R	AGC1LEVEL	AGC1 current value (external)
0x92 - 0x93	R	AGC2LEVEL	AGC2 current value (internal)

All parameters identified by (*) are automatically configured when writing 0x01 into SETAUTOCFG register.

Performance Specification

Modulation

Supports QPSK and 16, 32, 64, 128, 256, 512, 1024-QAM.

Roll-Off Factor

Greater than 0.11.

Symbol Rate

Up to $f_{REF}/8$ (9.36 Mbaud for $f_{REF} = 75$ MHz, $f_{XTAL} = 30$ MHz) with IF or baseband input, 32-taps equalizer.

Up to $f_{XTAL}/(2(1+\alpha))$ (13 Mbaud for $f_{REF} = 30$ MHz, ALPHA = 0.15) with IF input, 16-taps equalizer.

Up to $f_{REF}/4$ (18.75 Mbaud for $f_{REF} = 75$ MHz, $f_{XTAL} = 30$ MHz) with baseband input, 16-taps equalizer.

Note however, that the standard MPEG2-TS frame recovery and Forward Error Correction part of the chip can only be used when *bitrate* $\leq f_{REF}$. It is possible to use the constellation mode in the opposite case in order to use the demodulation part of the chip only and receive the symbols at the output. (See OUTPUTCFG register I^2C to configure this operating mode).

Bit Error Rate

Figures in the appendix indicate Bit Error Rate (BER) as a function of Carrier to Noise ratio (C/N) for different QAM modulations schemes. Theoretical curves are given to indicate how much degradation is observed with the real performance of the chip.

The following table indicates the degradation from theory (implementation margin) for uncoded QAM at BER = 10^{-4}.

Table 6.

Modulation scheme	C/N degradation at BER = 10^{-4}
QPSK	0.1 dB
QAM-16	0.2 dB
QAM-32	0.2 dB
QAM-64	0.2 dB
QAM-128	0.3 dB
QAM-256	0.4 dB
QAM-512	0.5 dB
QAM-1024	0.7 dB

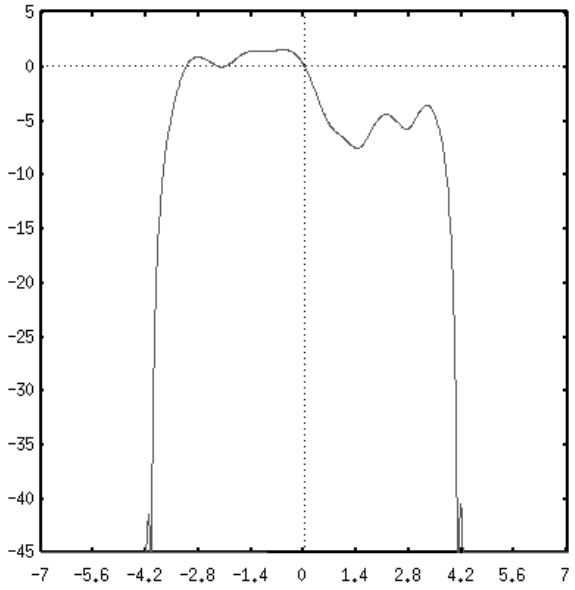
Echo Cancellation

The following table indicates the additional degradation between use of a theoretical equalizer and the real chip equalizer, for uncoded QAM at BER = 10^{-4}, when the channel has the transfer response shown in Figure 4.

Table 7.

Modulation scheme	C/N degradation at BER = 10^{-4}
QPSK	0.3 dB
QAM-16	0.3 dB
QAM-32	0.3 dB
QAM-64	0.3 dB
QAM-128	0.3 dB
QAM-256	0.3 dB
QAM-512	0.3 dB
QAM-1024	0.4 dB

Figure 5. Received Spectrum Used to Measure Degradation with Echoes



Phase Noise Tolerance

The following table indicates the additional degradation when a phase noise of -80 dBc at 10 kHz is present after the tuner, for uncoded QAM at BER = 10^{-4}.

Table 8.

Modulation scheme	C/N degradation at BER = 10^{-4}
QPSK	0.1 dB
QAM-16	0.1 dB
QAM-32	0.1 dB
QAM-64	0.1 dB
QAM-128	0.1 dB
QAM-256	0.1 dB
QAM-512	0.3 dB
QAM-1024	0.9 dB

AM Hum Tolerance

Input amplitude variation of 20% peak-to-peak can be supported by the demodulation at frequencies 100-120 Hz.

Locking Time

- 5 to 10 ms, when no echoes are present,
- 20 ms typical when echoes are present (see Figure 5).

Carrier Offset

Up to 12% of the symbol rate: +/- 1 MHz at 8 Mbaud.

Timing Offset

Up to 4000 ppm of the symbol rate (+/- 30 kHz at 8 Mbaud).

Electrical Characteristics

Table 9. Electrical Specification

Signal Name	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD5}	I^2C DC supply voltage	I^2C and AGC1 I/Os	V_{DD3}	5	5.3	V
V_{DD3}	DC supply voltage	Core and standard I/Os	3.0	3.3	3.6	V
V_I	DC input voltage		0		VDD	V
V_O	DC output voltage		0		VDD	V
TEMP	Operating free air temperature range	Commercial	0		+70	°C

Table 10. Absolute Maximum Ratings

Signal Name	Parameter	Conditions	Min	Max	Unit
V_{DD3}	DC supply voltage	Core and standard I/Os	-0.3	4.6	V
V_I	DC input voltage, 3.3V I/Os		-0.3	VDD3 + 0.3, 4.6 max	V
	DC input voltage, 5V I/Os		-0.3	VDD5 + 0.3, 5.5max	V
V_O	DC input voltage, 3.3V I/Os		-0.3	VDD3 + 0.3, 4.6 max	V
	DC input voltage, 5V I/Os		-0.3	VDD5 + 0.3, 5.5max	V
TEMP	Operating free air temperature range	Commercial	0	+70	°C

Table 11. DC Characteristics

Signal Name	Parameter	Conditions	VDD	Min	Max	Unit
TEMP	Temperature			-40	+85	°C
V_{IL}	Low level input voltage	Guaranteed input low voltage	3.0 to 3.6	-0.3	0.3 x VDD3	V
V_{IH}	High level input voltage	Guaranteed input high voltage	3.0 to 3.6	+0.7 x VDD3	VDD3 + 0.1V	V
V_{OL}	Low level output voltage	IOL = 0.3mA	3.0		VSS + 0.1V	V
V_{OH}	High level output voltage	IOH = 0.3mA	3.0	VDD3 -0.1		V

Schematic Diagrams

Figure 6. Standard Use of AT76C651 in Set Top Box Front End

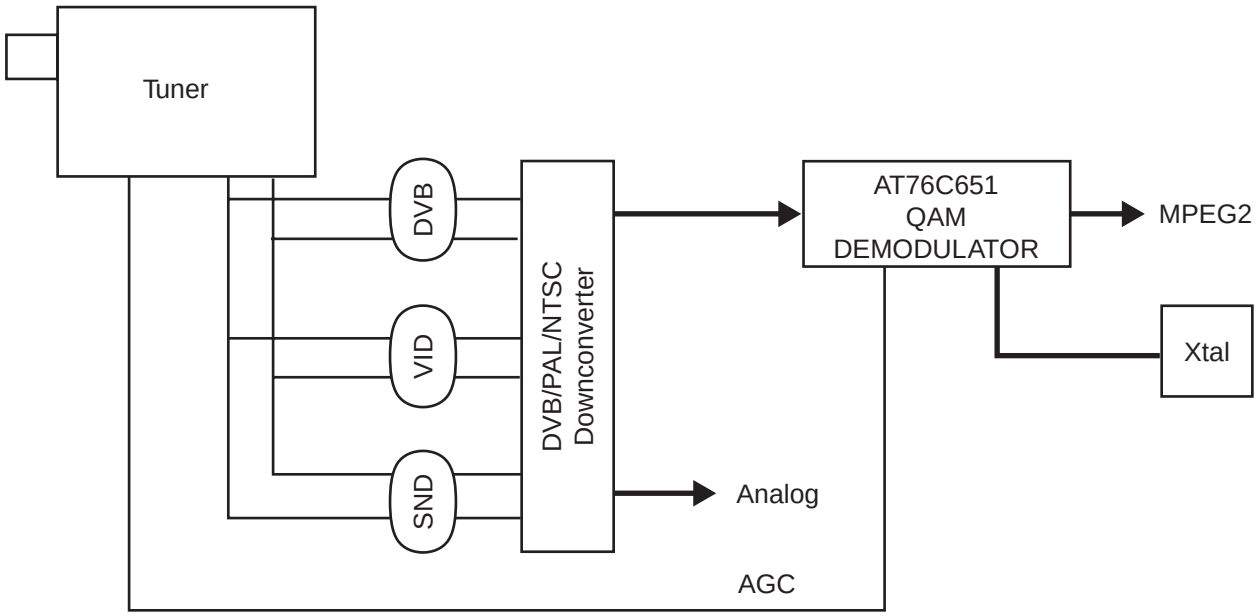
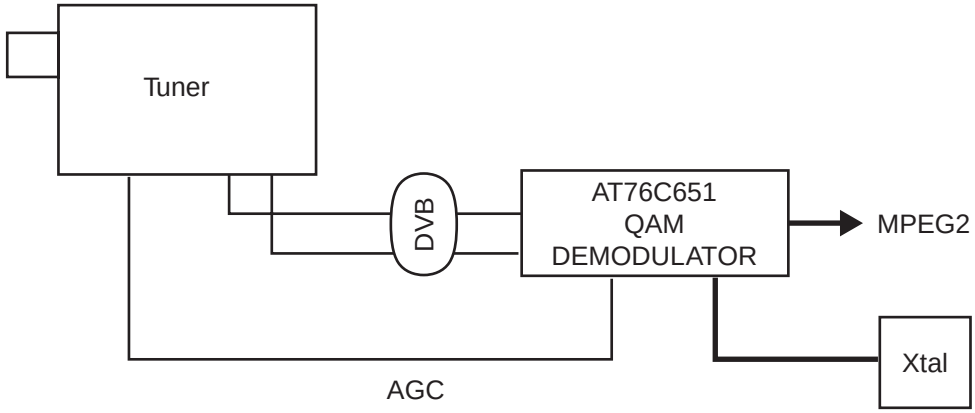


Figure 7. Simplified Use of AT76C651 When no Analog TV Demodulation is Required



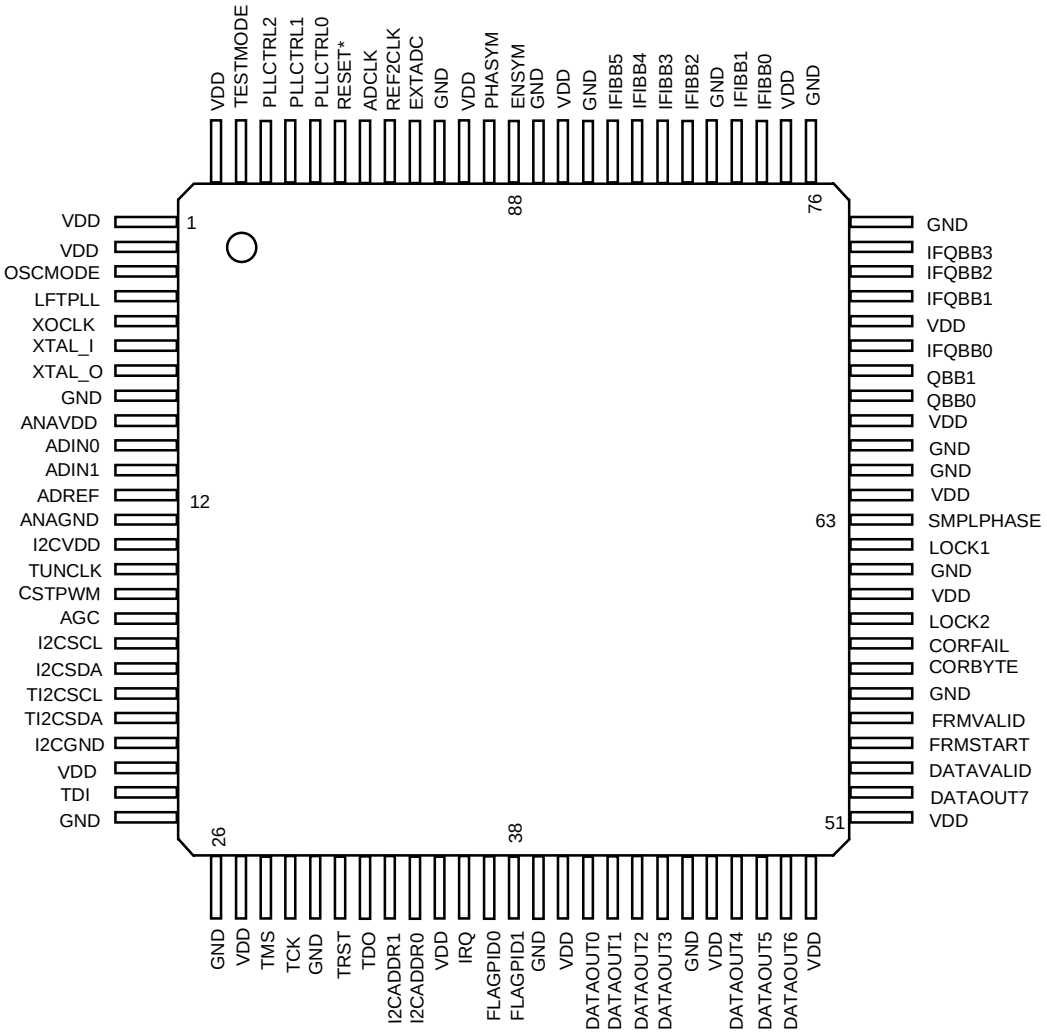
Packaging Information

100-pin TQFP package.

Commercial temperatures: 0 to 70 °C.

Thermal resistance of the package: 40°C/W.

Figure 8. Package Outline



Note: The I/Os located between pins I2CVDD (14) and I2CGND (22) must use VDD5 voltage. All other I/Os must use VDD3 voltage.

Figure 9. 100-pin TQFP Package

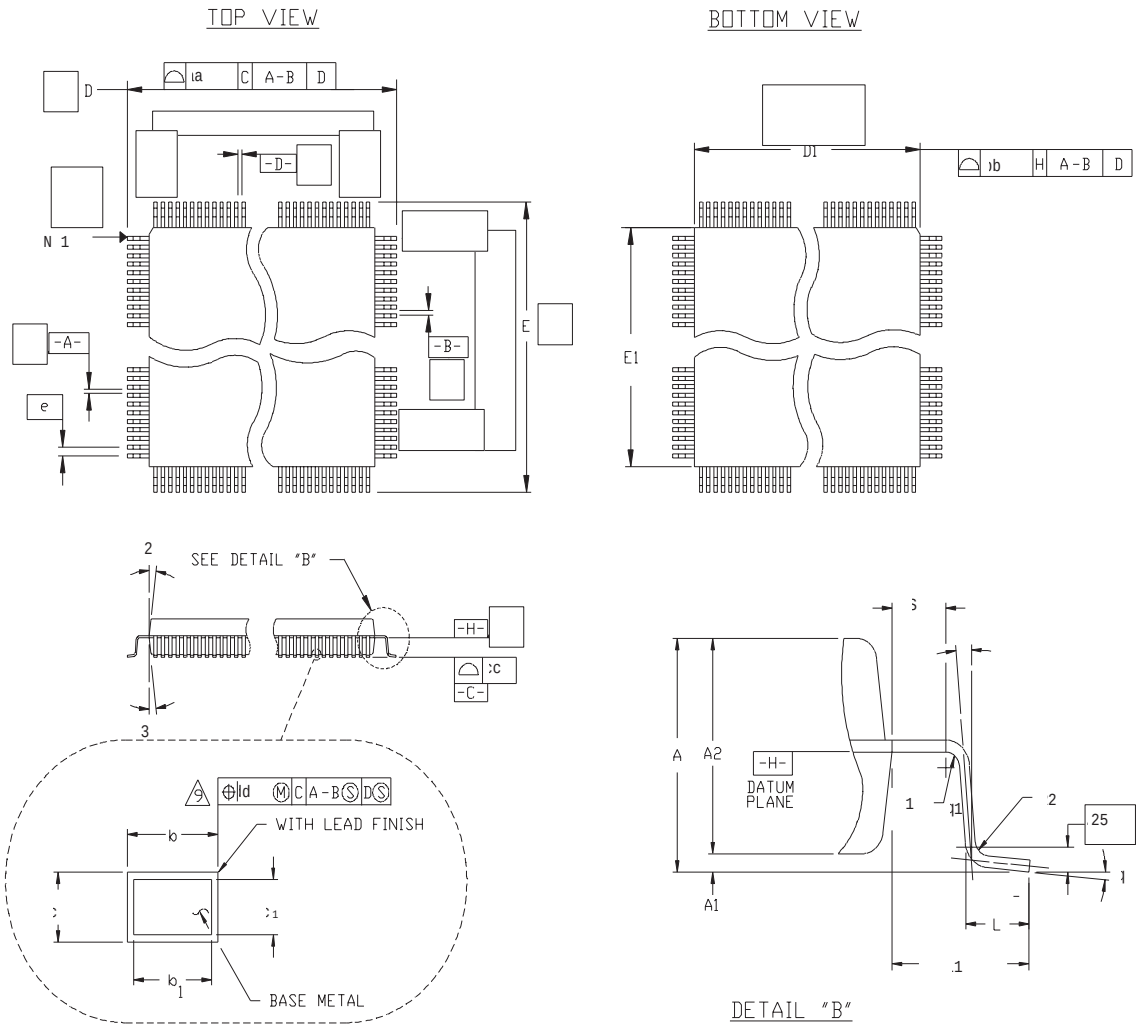


Table 12. Lead Count Dimensions

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
100	16.0	14.0	0.17	0.22	0.27	0.17	0.2	0.23	0.50	0.10	0.06

Table 13. Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.09		0.2
c1	0.09		0.16
L	0.45	0.6	0.75
L1		1.00 REF	
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of form and position			
aaa		0.2	
bbb		0.2	

Appendix

Bit Error Rate Measurements (uncoded)

Figure 10. QAM-64

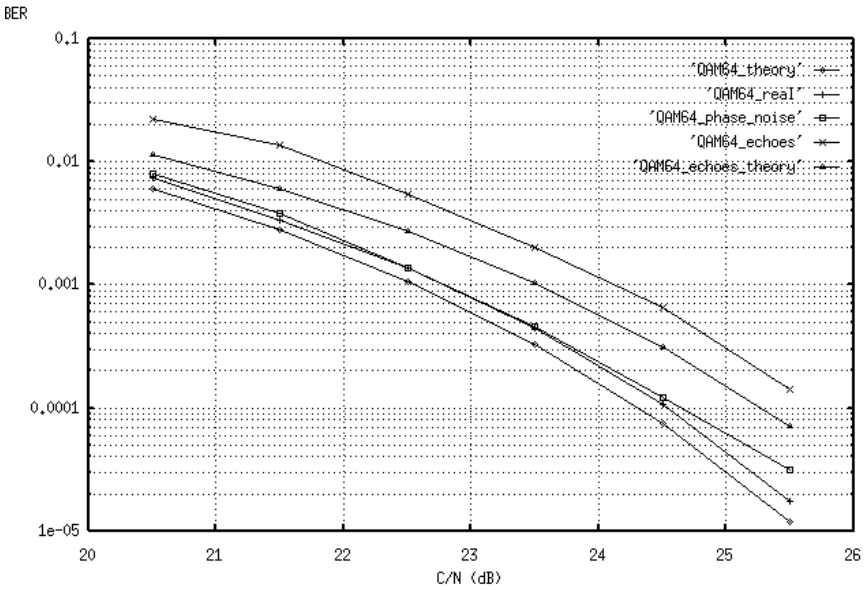


Figure 11. QAM-256

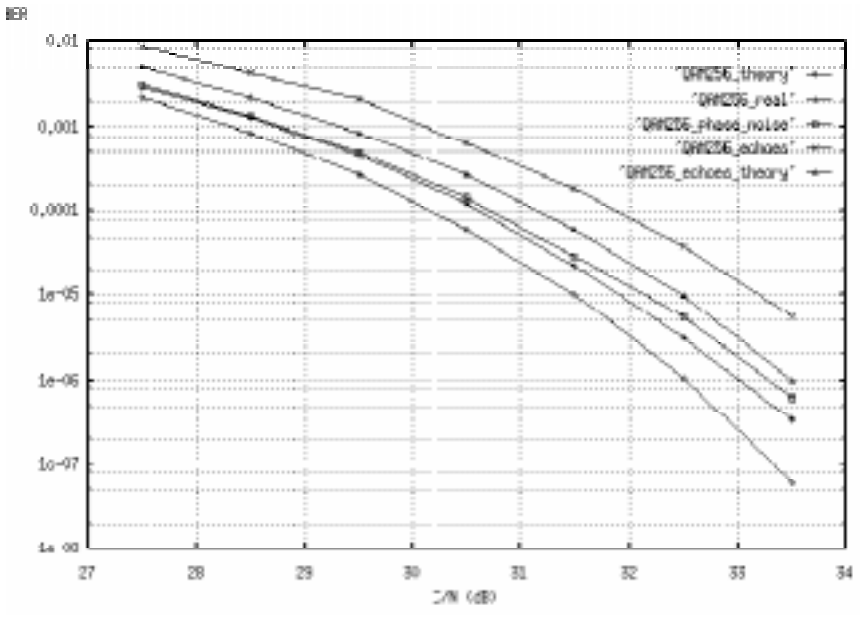
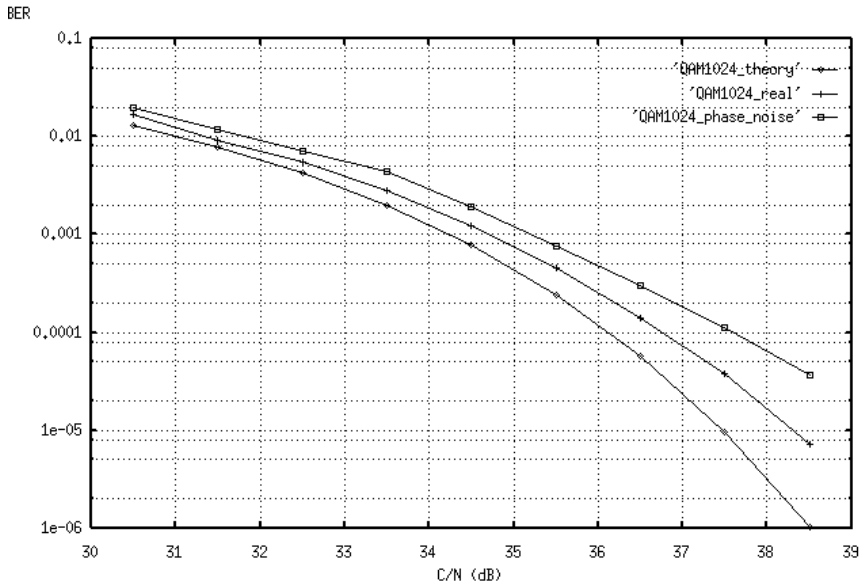


Figure 12. QAM-1024



Configuration and Monitoring Registers

Description

The AT76C651 device is controlled by an I2C interface. Most internal registers are in read/write mode (configuration registers). However, monitoring registers are in read-only mode. Note also that two special registers are write-only, SETAUTOCFG and RESTART. In most applications, very few of these registers need to be configured since the SETAUTOCFG can be used. Some registers are not described in this document. They are used internally and should not be written with a different value after SETAUTOCFG, or may lead to performance degradation. This means that no other address than the ones specified in this document should be used in I2C write mode. Also, reserved bits in a register should always be written with the value 0.

General Registers

SYMRATE: 0x00 to 0x02 (read/write)

Transmission symbol rate. These registers give the initial symbol rate of the timing recovery algorithm. A maximum offset of 4000 ppm between the actual symbol rate and this value can be tolerated by the device. The internally compensated frequency offset can be monitored in the register TIMFREQOFF.

The symbol rate is given as a fraction of the REFCLK frequency. The value must be given with a mantissa (21 bits) and an exponent (3 bits).

	b7	b6	b5	b4	b3	b2	b1	b0
0x00	mantissa (20:13)							
0x01	mantissa (12:5)							
0x02	mantissa (4:0)					exponent (2:0)		

To compute these value the following equations can be used:

$$f_{REF} = \left(\frac{f_{XTAL}}{2}\right) pllctrl \text{ with } pllctrl = 2,4,5,6,7$$

$$exponent = floor\left(\log_2\left(\frac{f_{symbol}}{f_{REF}}\right)\right)$$

$$mantissa = \left(\frac{f_{symbol}}{f_{REF}}\right) 2^{30 - exponent}$$

Example:

For a 30 MHz crystal and pllctrl = 5, $f_{REF} = 75$ *MHz*

A symbol rate of 5 Mbauds gives:

exponent = 6 (0x6) mantissa = 1 118 481(0 x 11 11 11).

So the register value is 0x 88 88 8E

A symbol rate of 6.875 Mbauds gives:

exponent = 6 (0x6) mantissa = 1 537 911(0 x 17 77 77).

So the register value is 0 x BB BB BE (default value)

QAMSEL: 0x03 (read/write)

Specifies the used modulation scheme. This register indicates the number of QAM levels and other parameters such as the used mapping type (DVB or others), whether coherent demodulation or differential demodulation is used for QPSK, and whether Intermediate Frequency (IF) or Baseband (BB) input is used.

	b7	b6	b5	b4	b3	b2	b1	b0
0x03	iforbb	demtyp	maptyp			qamtyp		

- Iforbb : 0 for IF input signal (internal or external A/D), 1 for BB input signal (external A/D only)
- Demtyp : 0 for coherent demodulation, 1 for differential demodulation (in QPSK only)
- Maptyp : 00 for DVB mapping, 10 for DAVIC mapping, other values reserved
- Qamtyp : Number of bits to specify a QAM symbol. Example: 2 for QPSK, 4 for QAM-16, 5 for QAM-32, 6 for QAM-64, 7 for QAM-128, 8 for QAM-256, 9 for QAM-512, 10 for QAM-1024. (0, 1, 3, and greater or equal to 11 are reserved values).

BBFREQ: 0x04 to 0x05 (read/write)

Intermediate Frequency (IF) to Baseband (BB) down conversion frequency. These registers indicate the initial frequency used to downconvert the signal from IF to BB. The value is between 0 and $f_{XTAL}/2$ and is given as a fraction of f_{XTAL}. A maximum offset between the actual IF and this value of 12% of the symbol rate can be tolerated by this device. This offset can be monitored in the DDSFREQOFFSET and CARFREQOFFSET registers.

	b7	b6	b5	b4	b3	b2	b1	b0
0x04	bbfreq1 (15:8)							
0x05	bbfreq0 (7:0)							

The frequency is computed by:

$$f_{IF} = \frac{bbfreq1 \times 256 + bbfreq0}{65536 \times f_{XTAL}}$$

where f_{XTAL} is the frequency of the crystal oscillator.

Example: For a 30 MHz crystal, and a signal at IF frequency f_{IF} = 6 MHz, bbfreq1 = 51 (0x33) and bbfreq0 = 51 (0x33).

Note also that subsampling can be used with this device. This means that the IF can be greater than the sampling frequency of the signal. For example, it is possible to have a sampling frequency f_{XTAL} = 30 MHz, and the IF at f_{IF} = 36 MHz. In that case, an image of the spectrum after sampling is present at f_{IF2} = 36-30= 6MHz , thus the content of BBFREQ should correspond to f_{IF2}.

SETAUTOCFG: 0x06 (write only)

Automatic configuration of the device. This address, when written with the value 0x01, automatically updates all registers of the device except for SYMRATE, QAMSEL, and BBFREQ which remain the same. All values are derived from these 3 non-modified registers, thus offering a very straight forward configuration of the entire device without necessarly understanding the meaning of all other parameters. However, it is possible, if necessary, to modify some register values after having used SETAUTOCFG.

Note also that after hard reset of the chip, all registers are automatically configured with the automatic configuration assuming a symbol rate of 6.875 Mbaud, 64-QAM, and f_{IF} = 0.25 f_{XTAL}. This corresponds to the configuration of most DVB-C channels over cable networks.

RESTART: 0x07 (write only)

Restarts the device without modifying the content of I^2C registers. This address, when written with the value 0x01, restarts the device. All recovery loops (AGC, timing, carrier), and the equalizer restart from their initial value. This should always be done after a SETAUTOCFG or any reconfiguration of I^2C registers.

OUTPUTCFG: 0x08 (read/write)

Data output configuration. This register configures the output format on pins DATAOUT7 to DATAOUT0 of the device.

	b7	b6	b5	b4	b3	b2	b1	b0
0x08	reserved		tundiv		irq pol	outputmode		

- Tundiv specifies the frequency of the clock signal output on TUNCLK pin. The frequency of this clock is given by:

$$f_{TUNCLK} = \frac{1}{p} f_{XTAL} \qquad with \qquad p = 2^{TUNDIV+1}$$

So p can take the values: 2, 4, or 8. When tundiv = 3, there is no output on TUNCLK pin in order to reduce power consumption if not needed.

- Outputmode can take the following binary values:
  - 000: MPEG2-TS parallel (DVB common interface)
  - 001: MPEG2-TS serial
  - 010: Constellation before decision
  - 011: I output after AGC1 and Baseband conversion
  - 100: I output after Timing Recovery
  - 101: I output after A/D sampling
- irqpol configures the polarity of the IRQ output pin
  - 0: IRQ is in high impedence or has value 0 when interruptions occur (see IRQMASK register)
  - 1: IRQ is in high impedence or has value 1 when interruptions occur (see IRQMASK register)

Example: 0x0 configures MPEG2-TS parallel output with IRQ going low when interruptions occur. The default value after SETAUTOCFG is 0x30.

MASKLOCK1: 0x09 (read/write)

Mask for MASKLOCK1 output pin. This register specifies the lock signals that must be monitored on the LOCK1 output pin. If all internal lock signals configured by this mask go high, then LOCK1 goes high.

	b7	b6	b5	b4	b3	b2	b1	b0
0x09	fec	car	equ	tim	agc 1	agc 2	adc	pll

fec : mask on forward error correction lock signal

car : mask on carrier recovery loop lock signal

equ : mask on equalizer lock signal

tim : mask on symbol rate recovery lock signal

agc2 : mask on digital agc lock signal

agc1 : mask on analog agc lock signal

adc : mask on analog agc level lock signal

pll : mask on Phase Lock Loop (pll) lock signal

SETAUTOCFG configures MASKLOCK1 at value 0x80, corresponding to the FEC lock signal only.

MASKLOCK2: 0x0A (read/write)

Mask for MASKLOCK2 output pin. This register specifies the lock signals that must be monitored on the LOCK2 output pin. If all internal lock signals configured by this mask go high, then LOCK2 goes high.

	b7	b6	b5	b4	b3	b2	b1	b0
0x0A	fec	car	equ	tim	agc 1	agc 2	adc	pll

SETAUTOCFG configures MASKLOCK2 at value 0x70, corresponding to the lock signals of the carrier recovery, the equalizer and the timing recovery, that is the full demodulator.

IRQMASK: 0x0B (read/write)

Mask for IRQ output pin. This register specifies the mask on events which should activate the IRQ pin. IRQ goes to the value specified by irqpol (see OUTPUTCFG configuration) when any of the events specified by the mask described below occurs and goes back to high impedence when any I^2C register is written by the microcontroller.

	b7	b6	b5	b4	b3	b2	b1	b0
0x0A	unlck 1	lck 1	unlck 2	lck 2	sat	frm lst	time_win	

- unlck1: IRQ when LOCK1 signal goes from 1 to 0
- lck1: IRQ when LOCK1 signal goes from 0 to 1
- unlck2: IRQ when LOCK2 signal goes from 1 to 0
- lck2: IRQ when LOCK2 signal goes from 0 to 1
- frmlst: IRQ when frame was lost
- sat: IRQ when signal input loss (AGC saturation)
- time_win: (periodic generation of IRQ)
  - 00: IRQ not activated by time delay
  - 01: IRQ activated every 2048 frames
  - 10: IRQ activated every 16384 frames
  - 11: IRQ activated every 10^8 bits

SETAUTOCFG configures the mask on UNLOCK1.

TUNI2CADD: 0x0C (read/write)

Address of tuner connected to I^2C bus of device (pins TI2CSCL and TI2CSDA). This register specifies the I^2C address of the tuner when connected to the device. For more precisions on the tuner I^2C switch principle: see "I^2C Read Mode" on page 9.

	b7	b6	b5	b4	b3	b2	b1	b0
0x0C	Tuner I^2C address							EN

EN enables the switch when set to 1.

Note: EN should be set to 1 when tuner is configured. Then EN must be set back to 0.

CHIPID: 0x0E to 0x0F (read)

Gives information about chip number and version. Value is 0x6510 (AT76C651, version A).

	b7	b6	b5	b4	b3	b2	b1	b0
0x0E	0	0	1	1	0	1	0	1
0x0F	0	0	0	1	0	0	0	0

Baseband Conversion and AGC1

AGC1NMIN: 0x13 (read/write)

Specifies the minimum (or maximum) amplification value of AGC1 given by the PWM output pin, which is between 0 and 255 when BBCFG(4) = 0 (or BBCFG(4) = 1). For more precisions about the BBCFG register, see description below. This value can be used to saturate amplification in case of non-linearities of the amplifier at extreme values.

	b7	b6	b5	b4	b3	b2	b1	b0
0x13	agc1nmin							

Example: 0x00 (for maximum amplifying range).

AGC1NMAX: 0x14 (read/write)

Specifies the maximum (resp. minimum) amplification value of AGC1 given by the PWM output pin, which is between 0 and 255 when BBCFG(4) = 0 (or BBCFG(4) = 1). For more precisions about the BBCFG register, see description below. This value can be used to saturate amplification in case of non-linearities of the amplifier at extreme values.

	b7	b6	b5	b4	b3	b2	b1	b0
0x14	agc1nmax							

Example: 0xFF (for maximum amplifying range).

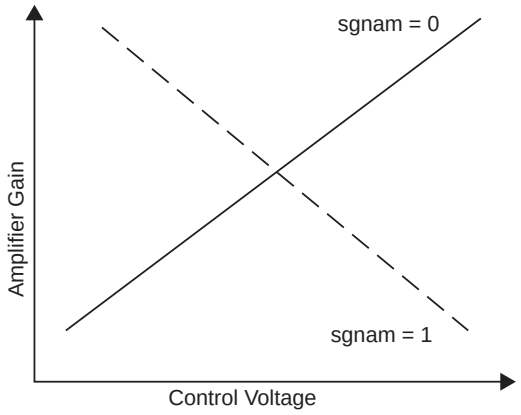
BBCFG: 0x15 (read/write)

General control of IF to BB conversion. This register controls several parameters of the AGC1 control loop, internal DC-offset compensation and AGC output format.

	b7	b6	b5	b4	b3	b2	b1	b0
0x15	res	res	dc con	sgn am	adc con	res	pwm con	res

- Res: reserved (must be configured with 0 when writing register)
- Dccon: DC-offset control. If set to 0, the internal DC-offset compensation is ON. If set to 1, the internal DC-offset control is OFF. The DC-offset should be ON when the input signal is in BB.
- Sgnam: sign of the amplifier control command (see Figure 13).

Figure 13. Sgnam Configuration for Amplifier Gain Control



- Adccon: specifies whether ADCLEVEL must be automatically adapted in the presence of adjacent channels or if it must keep its initial value defined by register AGC1INITADC. Automatic adaptation is configured by 0, no adaptation is configured by 1.
- Pwmcon: specifies output format for AGC and CSTPWM pins. If set to 0, the AGC control is output in PWM format on AGC pin, and a completely configurable value (see CSTPWM register) is output in PWM format on CSTPWM pin. If set to 1, the AGC control is output in differential format on AGC and CSTPWM pins. In this case, differential integration must be performed in the analog domain.

In case of a PWM output, the AGC pin should be connected to an R-C filter with a cutoff frequency of about 5 kHz. Example: R = 1.5 k, C = 22 nF.

Note: The PWM output pin can be power supplied by 5V through the I^2CVDD power supply. This assumes I^2C bus functions at 5V.

CSTPWM: 0x17 (read/write)

Specifies a configurable value between 0 and 255 which is given in PWM format on CSTPWM pin in case BBCFG(1) = 0. The CSTPWM pin should be connected to an R-C filter with a cutoff frequency of about 5 kHz. Example: R = 1.5 k, C = 22 nF. This voltage output can be used to control any other device on the board. Example: other amplifier gain control, variable capacitor, etc.

Note: This pin can output 5V since it is power supplied by the I2CVDD power supply (this assumes I^2C bus functions at 5V).

	b7	b6	b5	b4	b3	b2	b1	b0
0x17	cstpwm							

Example: cstpwm = 0x7F (2.5 V in case 5 V is connected to I2CVDD)

BBTOPCNT: 0x19 (read)

Monitoring register indicating the number of A/D saturations over 16384 successive samples. This register can take values between 0 and 255. 255 indicates that more than 255 A/D saturations have occured during the last 16384 samples.

	b7	b6	b5	b4	b3	b2	b1	b0
0x19	bbtopcnt							

When the demodulator is properly working, this value should indicate 0x00

Timing Recovery

TIMLOOPCFG: 0x23 to 0x24 (read/write)

These two registers configure the loop bandwidth of the timing recovery loop.

	b7	b6	b5	b4	b3	b2	b1	b0
0x23	blmax_mexp				blmin_mexp			
0x24	bltrack_mexp				reserved			

Example: 0x7F for register 0x23 and 0x9 for register 0x24.

The three parameters blmax_mexp , blmin_mexp and bltrack_mexp are 4-bit unsigned numbers that must follow the conditions:

- $7 \leq$ blmax_mexp $\leq$ blmin_mexp ≤ 15
- $7 \leq$ bltrack_mexp ≤ 15

They are related to the bandwidth blmax, blmin and bltrack by the formula: $Blx = 2^{-Blx\_mexp}$

Blmax is the maximal and initial bandwidth value used with robust (Gardner type) comparator. Blmin is the minimal bandwidth value that can be taken by the loop bandwitdh with the same comparator. When Blmax > Blmin, the loop can automatically decrease when the lock indicator is positive, or increase when this signal detects that the timing recovery system is out of lock. This variable bandwidth allows fast convergence and large timing frequency lockin range in initial acquisition phase, and low timing jitter when the system is locked.

Bltrack is the fixed value of the bandwith used with decision base comparator "comp track". Typical values corresponding to the example above are:

Blmax = $2^{-7} \Rightarrow$ Blmax_mexp = 7

Blmin = $2^{-15} \Rightarrow$ Blmin_mexp = 15

Bltrack = $2^{-9} \Rightarrow$ Bltrack_mexp = 9

TIMLOOPMONIT: 0x29 (read)

Monitoring registers indicate the value of the automatically variable loop bandwidth.

	b7	b6	b5	b4	b3	b2	b1	b0
0x29	Bl_mexp				reserved			

Bandwidth Bl which is given by formula: $Bl = 2^{-Bl\_mexp}$

Bl_mexp is a unsigned value taking values from Blmax_mexp to Blmin_mexp (see TIMLOOPCFG).

When timing is well recovered, Bl is equal to Blmin.

Carrier Recovery

CARALPHAACQ/CARBETAACQ: 0x31 / 0x32 (read/write)

These two registers select the carrier loop bandwidth during acquisition phase. Through those two bytes we can control the bandwidth and the damping factor ξ of the loop filter.

	b7	b6	b5	b4	b3	b2	b1	b0
0x31	caralphaacq							
0x32	carbetaacq							

Table 14 depicts some typical values for CARALPHAACQ and CARBETAACQ.

Table 14.

$B_l \bullet f_{symbol}$	ξ	CARALPHAACQ	CARBETAACQ
0.005	0.7	0xAE	0x9C
0.005	1.0	0x98	0x98
0.005	2.0	0x9A	0xBC
0.005	4.0	0x9A	0xDD
0.010	0.7	0x9E	0x7C
0.010	1.0	0x88	0x78
0.010	2.0	0x8A	0x9C
0.010	4.0	0x8A	0xBD
0.030	0.7	0x7A	0x4D
0.030	1.0	0x7C	0x49
0.030	2.0	0x7E	0x6D
0.030	4.0	0x7F	0x8E

In automatic configuration these parameters correspond to Bl f_{symbol} = 0.03 and ξ = 1.0.

CARALPHATRACK/CARBETATRACK: 0x33 / 0x34 (read/write)

These two registers select the carrier loop bandwidth during tracking phase (after acquisition). The same table as given for (0x31/0x32) configures these parameters. The switch between tracking phase and acquisition phase takes place when agc2, equalizer and carrier are locked.

	b7	b6	b5	b4	b3	b2	b1	b0
0x33	caralphatrack							
0x34	carbetatrack							

In automatic configuration these parameters correspond to Bl f_{symbol} = 0.03 and ξ = 4.0.

CARCONST: 0x39/0x3A/0x3B (read)

	b7	b6	b5	b4	b3	b2	b1	b0
0x39	I (11:4)							
0x3A	Q (11:4)							
0x3B	I (3:0)				Q (3:0)			

The constellation points after gain adjustment, timing recovery, equalization and carrier recovery can be collected without breaking down the demodulation and the channel decoding. The two components (I, Q), with 12-bit precision are collected in three bytes:

- byte1 (0x 39): 8 Msb of I
- byte2 (0x 3A): 8 Msb of Q
- byte3 (0x 3B): The 4 Msb of byte 3 are equal to the 4 Lsb of I and the 4 lsb of byte3 are equal to the 4 Lsb of Q.

Byte1 should be collected first. When the address of this byte is detected by the AT76C651, then a constellation point (I: 12 bits , Q: 12 bits) is memorized and only the 8 MSBs of I are sent as data on the I^2C bus. Byte2 and Byte3 can be collected later, their content does not change unless byte1 is collected again.

AGC2

AGC2CFG: 0x42 (Read/write)

	b7	b6	b5	b4	b3	b2	b1	b0
0x42	res		loopbw1			loopbw2		

Two operating modes exist for agc2: boost mode and normal mode. After a reset or a soft clear, the agc2 is in boost mode and unlocked. During this phase equalizer and carrier are inhibited. The switch from boost mode to normal mode happens when agc2 locks. The agc2 loop bandwidth can be controlled through loopbw2 during boost mode and by loopbw1 during normal mode. In both cases the loop bandwidth is proportional to loopbw.

Figure 15 gives the value of AGC2CFG for the different QAM in automatic configuration.

Table 15.

QAM	AGC2CFG
QPSK	0x34
QAM-16	0x35
QAM-32	0x35
QAM-64	0x34

Table 15.

QAM	AGC2CFG
QAM-128	0x33
QAM-256	0x32
QAM-512	0x31
QAM-1024	0x30

AGC2INIT: 0x43 and 0x44 (read/write)

These registers configure the initial agc2 gain.

	b7	b6	b5	b4	b3	b2	b1	b0
0x43	mantissa (10:3)							
0x44	mantissa (2:0)			exponent (4:0)				

AGC2INIT is coded in a floating format with a *mantissa* coded with 11 unsigned bits and an exponent coded with 5 signed bits, defined as follows:

exponent = floor($\log_2$(agc2gain))

mantissa = floor(agc2gain.$2^{-exponent}$x1024)

Exponent must be in the range -6 to 13, and *mantissa* takes its value in the range 1024 to 2047.

Equalizer

EQUCFG: 0x51 (read/write)

This register controls the equalizer operating mode.

	b7	b6	b5	b4	b3	b2	b1	b0
0x51	inh	fre	len	structure		step		

- inh: When set to one this parameter inhibits the equalizer: all equalizer taps are set to zero except central tap which is equal to one (in complex format). In standard configuration it is set to 0.
- fre: When set to one it freezes the equalizer taps adaptation. The equalizer behaves as a complex FIR (Finite Impulse Response). In standard configuration it is set to 0.
- len: The equalizer has 32 taps when this parameter is set to zero and only 16 taps when set to one. The first mode can be selected only if the ratio between fref and fsymbol is higher or equal to 8.(f_{ref} / f_{symbol} ≥ 8). In standard configuration it is set to 1.
- structure: Two equalizer structures are implemented in the AT76C651: LE (Linear Equalizer) and DFE (Decision Feedback Equalizer). When b5 = 1, only LE structure can be selected. In DFE mode two sub-structures, depending on the position of the central tap, can be configured. Figure 16 shows the different possibilities.
- step: This parameter controls the step used to adapt the equalizer taps. The higher the step is, the higher is the adaptation step.

Table 16.

b4b3	Structure
00	LE
10	LE
01	DFE with central tap position between 0 and 7
11	DFE with central tap position between 8 and 15

EQUCENTRAL: 0x52 (read/write)

	b7	b6	b5	b4	b3	b2	b1	b0
0x52	res	adapt		central tap position				

- central tap position: EQUCENTRAL (4:0) gives the position of the equalizer central tap. This position should be set between 0 and 31 when EQUCFG(6)=0 and

between 0 and 15 when EQUCFG(6) = 1. In standard configuration this parameter is set to 7.

- adapt: The central tap adaptation mode can be selected between the following configurations:

Table 17.

b6b5	Real part	Imag part
00	adapted	adapted
01	adapted	fixed to 0
10	fixed to 1	adapted
11	fixed to 1	fixed to 0

In standard configuration it is set to 11.

EQUTAPRORD: 0x53 (read/write)

	b7	b6	b5	b4	b3	b2	b1	b0
0x53	reserved				equalizer tap position			

This parameter selects the position of the equalizer tap that we want to collect (see “EQUTAPREAL: 0x54 / 0x55 (read) and EQUTAPIMAG: 0x56 / 0x57 (read)” on page 26). The number of taps that can be read depends of the equalizer length (see “EQUCFG: 0x51 (read/write)” on page 25).

EQUTAPREAL: 0x54 / 0x55 (read) and EQUTAPIMAG: 0x56 / 0x57 (read)

	b7	b6	b5	b4	b3	b2	b1	b0
0x54 MSB	equtapreal (15:8)							
0x55 LSB	equtapreal (7:0)							
0x56 MSB	equtapimag (15:8)							
0x57 LSB	equtapimag (7:0)							

After selecting the equalizer tap to read (see “EQUTAPRORD: 0x53 (read/write)” on page 26) the real part and the imaginary part of the tap are collected in 4 bytes. The first byte to read must be 0x54. When the AT76C651 detects this address it memorizes the equalizer tap value (4 bytes) and sends the 8 MSBs of the real part as red data. The three other bytes can be collected later. The value of the tap is equal to:

(real+j imag) = (signed (EQUTAPREAL) +
j signed (EQUTAPIMAG)) / 16384 .

FEC

FECIQINV : 0x60 (read/write)

Configuration of I and Q inversion. This register indicates if the I and Q channel must be swapped before demapping. An automatic mode is also provided.

	b7	b6	b5	b4	b3	b2	b1	b0
0x60	reserved					iqinv	iqinvcmd	

- iqinv is a read-only single bit which indicates if I and Q channel are swapped (in manual mode it is equal to b0).
- iqinvcmd is composed of two bits (read/write): the msb (b1) controls the use of the automatic mode (= 0) or the manual mode (= 1), the lsb (b0) is used in manual mode to swap I and Q channel.

Note: The automatic mode use the frame structure to choose the right configuration. If the frame is not recovered, iqinv can change at any time.

FECFLEN: 0x61 (read/write)

Frame length configuration. The size of frame can be configured.

	b7	b6	b5	b4	b3	b2	b1	b0
0x61	flen							

Flen is an 8-bit value which gives the length of the frame. This value should be higher than 50 to guarantee a correct functioning of the FEC decoder.

Example: for DVB MPEG2-TS the frame length is 204, this is the default value.

FECFSW: 0x62 (read/write)

Frame Synchronization Word Configuration.

	b7	b6	b5	b4	b3	b2	b1	b0
0x62	fsw							

Fsw is an 8-bit value which gives the normal value of the first byte in a frame. In DVB, the first byte of the frame is periodically bit-to-bit inverted to synchronize the de-scrambler, this is internally managed.

Example: for DVB MPEG2-TS the frame synchronization word is 0x47, this is also the default value.

FECDILVILEN: 0x63 (read/write)

Number of branches in the de-interleaver.

	b7	b6	b5	b4	b3	b2	b1	b0
0x63	reserved			dilvilen				

Dilvilen is an 5 bits value which give the number of branches in the de-interleaver. See below FECDILVMLEN for constraints.

Example: for standard DVB-C MPEG2-TS dilvilen should be set to 12 (default value).

FECDILVMLEN: 0x64 (read/write)

Memory step size of the deinterleaver.

	b7	b6	b5	b4	b3	b2	b1	b0
0x64	reserved			dilvmlen				

Dilvmlen is a 5-bit value which gives the memory step size of the de-interleaver (described in the DVB standard).

- The first branch has (dilvilen-1) x dilvmlen memory byte.
- The second branch has (dilvilen-2) x dilvmlen memory bytes.
- The third branch has (dilvilen-3) x dilvmlen memory bytes.
- ...
- The Dilvilenth branch has 0 memory bytes.

The first byte of a frame is always routed to the first branch if the de-interleaver. To allow a correct synchronization the following formula must be respected by the user:

fecdilvilen x fecdilvmlen = flen

The internal memory is limited to 2K bytes of ram:

$$\frac{flen(fecdilvilen-1)}{2} + fecdilvilen < 2048$$

Example: for DVB MPEG2-TS dilvilen must be set to 17 (default value). However, it can sometimes be advantageous to use fecdivilen = 17 with fecdilvmlen = 12 (keeping fecflen = 204) to get a better impulsive errors spreading.

FECINH: 0x65 (read/write)

Inhibition of selected parts of the Forward Error correction blocks.

	b7	b6	b5	b4	b3	b2	b1	b0
0x65	res	beind	force	scrm	rs	dilv	frm	diff

Fecinh is a 7-bit value. Each bit set to '1' indicates that the selected function is inhibited. The hardware bloc is then in a transparent mode.

Table 18.

FECINH bits	Functions Inhibited	Comments
b0: diff	differential decoder	useful for non-coherent demodulation
b1: frm	frame synchronization	prevent bit skipping if frames not needed
b2: dilv	de-interleaver	cannot be synchronized without frames
b3: rs	Reed-Solomon decoder	error detection without correction
b4: scrm	Scrambler	need inverted FECFSW for synchro.
b5: force	1st byte forced to FECFSW	cannot be used without frame recovery
b6: beind	Bit Error Indicator (MSB of 2nd byte)	enable external bit error rate measure

Example: for DVB MPEG2-TS, FECINH should be set to 0x00 (default value) but to execute an external Bit Error Rate measure, b3, b5 and b6 should probably be set to '1' (FECINH = 0x68).

For non DVB applications, with FECINH = 0x7E, it is possible to get data after QAM de-mapping and differential decoder in serial mode or in parallel mode (of course bytes are not aligned).

PID Filtering

PID1: 0x70-0x71 (read/write)

First MPEG PID to filter. This function can be disabled.

	b7	b6	b5	b4	b3	b2	b1	b0
0x70	reserved		enpid1	pid1 (12:8)				
0x71	pid1 (7:0)							

PID1 is a 14-bit value which gives the first MPEG PID to flag. This function is provided to make possible the use of simple software MPEG de-multiplexer. Bit 5 of the register 0x70 is an enable. When this function is enabled and if the 13-bit PID of an incoming frame matches PID1, the FLAGPID0 pin takes the value '1'. This filter is more prioritized than PID2 and PID3. The default value is 0x0000 so the function is disabled.

PID2: 0x72-0x73 (read/write)

Second MPEG PID to filter. This function can be disabled.

	b7	b6	b5	b4	b3	b2	b1	b0
0x72	reserved		enpid2	pid2 (12:8)				
0x73	pid2 (7:0)							

PID2 is a 14-bit value which gives the second MPEG PID to flag. This function is provided to make possible the use of simple software MPEG de-multiplexer. Bit 5 of the register 0x72 is an enable. When this function is enabled, if the 13-bit PID of an incoming frame matches PID2 and if PID1 flag is not set, the pin FLAGPID1 take the value '1'. This filter is more prioritized than PID3 but less than PID1. The default value is 0x0000, so the function is disabled.

PID3: 0x74-0x76 (read/write) and PIDMSK3: 0x77-0x79 (read/write)

Third PIDs to filter. This filter is 24-bit length with a mask of the same length.

	b7	b6	b5	b4	b3	b2	b1	b0
0x74	pid3 (23:16)							
0x75	pid3 (15:8)							
0x76	pid3 (7:0)							
0x77	pidmsk3 (23:16)							
0x78	pidmsk3 (15:8)							
0x79	pidmsk3 (7:0)							

PID3 is a 24-bit value which gives the third PID (the 2nd, 3rd and 4th bytes of frame) to flag. This function is provided to make possible the use of simple software MPEG de-multiplexer.

A 24-bit mask is also provided by registers 0x77-0x79. The MPEG header bits are only checked with PID3 if the corresponding bits in PIDMSK3 are set to '1'. If PIDMSK3 is set to 0x000000 the function is disabled.

If PID1 or PID2 get a match for a particular frame, PID3 filter is not performed for this frame. When PID3 gets a match, both pins FLAGPID0 and FLAGPID1 are set to '1'. This filter is less prioritized than PID1 and PID2. The default value is 0x000000 for PID3 and PIDMSK3. This function is disabled.

General Monitoring

LOCK: 0x80 (read)

Monitoring register which indicates the lock status of AGC1, AGC2, Timing Recovery, Carrier Recovery, Equalizer, FEC, and the PLL.

	b7	b6	b5	b4	b3	b2	b1	b0
0x80	fec	equ	car	tim	agc 2	agc 1	adc	pll

- fec: lock signal for FEC
- equ: lock signal for Equalizer
- car: lock signal for Carrier recovery
- tim: lock signal for Timing recovery
- agc2: lock signal for digital AGC (AGC2)
- agc1: lock signal for analog AGC (AGC1)
- adc: lock signal for AGC1 power reference value adaptation
- pll: lock signal for PLL

BER1: 0x81 to 0x83 (read)

Monitoring register which indicates the Bit Error Rate estimate over the last 10^8 bits. This register indicates the number of corrected bit errors in the last 10^8 bits, but does not take into account the frames that are not correctable, i.e., the frames in which more than 8 errors have occured (this value can be monitored in register NPERR).

	b7	b6	b5	b4	b3	b2	b1	b0
0x81	reserved				ber1(20:16)			
0x82	ber1(15:8)							
0x83	ber1(7:0)							

BER2: 0x84 (read)

Monitoring register which indicates another Bit Error Rate estimate based on a counter of false frame sync words. This register is meaningful when the Bit Error Rate is greater than 10^{-3}. The Bit Error Rate is given by *ber2/4096*.

	b7	b6	b5	b4	b3	b2	b1	b0
0x84	ber2							

NPERR: 0x85 (read)

Monitoring register which indicates the number of uncorrectable frames in the last 10^8 bits. The value is saturated at 255 if more than 255 uncorrectable frames have occured.

	b7	b6	b5	b4	b3	b2	b1	b0
0x85	nperr							

TIMFREQOFF: 0x86 to 0x88 (read)

Monitoring register which indicates the value of the recovered symbol rate offset with respect to the configured symbol rate (see “Symbol Rate” on page 12).

	b7	b6	b5	b4	b3	b2	b1	b0
0x86	timfreqoff (23:16)							
0x87	timfreqoff (15:8)							
0x88	timfreqoff (7:0)							

Timfreqoff is a positive integer value directly read in the loop filter memory. This value is scaled by a gain factor Kl inside the chip and added to the configured symbol rate. The result is used to control the timing Numerically Controlled Oscillator, and is the recovered symbol rate.

Therefore, it is possible to compute the real recovered symbol rate offset ΔT (in Hz) with the following formula:

$$\Delta T = \frac{timfreqoff \times K_l}{2^{29}}$$

The scaling factor K_l is internally defined as the approximation of the configured symbol rate given in the following formula:

$K_l = floor\ (mantissa \times 2^{-16})\ 2^{-4} \times 2^{exponent-10}$

where exponent and mantissa are the configured symbol rate exponent plus 10 and symbol rate mantissa (see “Symbol Rate” on page 12).

DDSFREQOFFSET: 0x89 to 0x8A (read)

Monitoring register which indicates the frequency offset recovered by the DDS (at IF to BB downconversion). This value added to the frequency entered in register BBFREQ gives the corrected IF frequency of the input signal.

This value is a fraction of the crystal frequency f_{XTAL}.

	b7	b6	b5	b4	b3	b2	b1	b0
0x89	ddsfreqoffset (15:8)							
0x8A	ddsfreqoffset (7:0)							

The offset frequency is given by:

$$f_{DDSFREQOFFSET} = \frac{ddsfreqoffset \times f_{XTAL}}{2^{20}}$$

CARFREQOFFSET: 0x8B to 0x8C (read)

Monitoring register indicating the frequency offset recovered by the carrier. The collected value is normalized to symbol rate.

	b7	b6	b5	b4	b3	b2	b1	b0
0x8B	carfreqoffset (15:8)							
0x8C	carfreqoffset (7:0)							

Address 0x8B (MSBs) must be read from the device first in order to ensure the correctness of the content of 0x8C (LSBs). The offset frequency is given by:

$$f_{CARFREQOFFSET} = \frac{signed(carfreqoffset) \times f_{symbol}}{2^{17}}$$

The total frequency offset recovered is given by:

$\Delta f = f_{DDSFREQOFFSET} + f_{CARFREQOFFSET}$

PHASENOISE: 0x8D to 0x8E (read)

The residual phase noise (after carrier recovery) is estimated. The collected information contents the phase noise due to oscillators and also the phase noise due to the additive noise integrated by the carrier loop filter. Hereafter follows an explanation how to compute the total residual phase noise and how to extract the phase noise due to additive noise.

	b7	b6	b5	b4	b3	b2	b1	b0
0x8D	phasenoise (15:8)							
0x8E	phasenoise (7:0)							

In:

σ^2_{φ} *(dB) = A (dB) + 10*log10 (phasenoise)*

φ denotes the residual phase noise and σ^2_{φ} the mean of φ square.

The parameter A depends of the QAM format and is given by the table below:

Table 19.

QAM	A (dB)
QPSK	-45.15
QAM-16	-54.69
QAM-32	-54.69

Table 19.

QAM	A (dB)
QAM-64	-62.05
QAM-128	-62.05
QAM-256	-68.67
QAM-512	-68.67
QAM-1024	-74.98

The phase noise portion due to the integration of the additive noise by the loop filter is given by:

$$\sigma^2_{\varphi_n} = B_l \times \sigma^2_n \times \alpha$$

The parameter α depends of the QAM format and is given by the table below, σ^2_{φ} denotes the mean square of the additive noise description (see “ADDITIVENOISE: 0x8F to 0x90 (read)” on page 31), and B_l the selected carrier loop bandwidth for tracking phase..

Table 20.

QAM	α
QPSK	2.53e-2
QAM-16 to QAM-1024	2.83e-2

The residual phase noise due to oscillators impairments is then equal to:

$$\sigma^2_{\varphi_{osc}} = \sigma^2_{\varphi} - \sigma^2_{\varphi_n}$$

Using $\sigma^2_{\varphi osc}$, the configured loop bandwidth, the symbol rate and an assumption about the tuner phase noise shaping, an estimation of the phase noise at a given frequency offset can be obtained.

The example below shows how to make this computation when the tuner phase noise level decreases by 20dB each time frequency offset is multiplied by 10. The result is given by following formula:

$$phasenoise_{spd} = \frac{\sigma^2_{\varphi osc} \times f_{symbol}(Hz)}{(\Delta f)^2 \cdot \alpha}(dBc)/(Hz)$$

phasenoise$_{spd}$ is the phase noise spectral density at frequency offset (Δf) given in Hz. α is a contant that depends on the carrier loop filter (see table below).

Table 21.

Bl	ξ	α
0.005	0.7	1460
0.005	1.0	1250
0.005	2.0	1030
0.005	4.0	980
0.010	0.7	720
0.010	1.0	600
0.010	2.0	510
0.010	4.0	480
0.030	0.7	225
0.030	1.0	180
0.030	2.0	160
0.030	4.0	150

Note: The phase noise information is not relevant if the demodulator is not locked.

ADDITIVENOISE: 0x8F to 0x90 (read)

An estimation of the additive noise level is implemented in the AT76C651. It can be used to compute the S/N (Signal to noise) ratio. Byte 0x8F should be collected first in order to ensure the correctness of 0x90. When the demodulator is not locked this information is not relevant.

	b7	b6	b5	b4	b3	b2	b1	b0
0x8F	additivnoise (15:8)							
0x90	additivnoise 0 (7:0)							

The following formulas give for each QAM format how to compute the S/N (dB) or the Eb/N (dB).In:

$$\sigma_n^2\,(dB) = 10 \times \log 10\left(\frac{additivenoise}{2^{16}}\right)$$

n denotes the additive noise and σ^2_n the mean of n square.

S/N (dB) = 10 x log10(A) - σ^2_n (dB)

Eb/N (dB) = 10 x log10(B) - σ^2_n (dB)

The table below gives for each QAM the values of A and B.

Table 22.

QAM	A	B
QPSK	2	1
QAM-16	10	10/4
QAM-32	20	20/5
QAM-64	42	42/6
QAM-128	82	82/7
QAM-256	170	170/8
QAM-512	330	330/9
QAM-1024	682	682/10

AGC1LEVEL: 0x91 (read)

Monitoring register which indicates the present level of AGC1 which is output in PWM format to AGC output pin. The value is comprised between AGC1NMIN and AGC1NMAX values.

	b7	b6	b5	b4	b3	b2	b1	b0
0x91	agc1level							

Agc1level indicates the control voltage value V applied at the input of the external amplifier through the R-C filter connected to the AGC pin. It is given by:

*V = agc1level / 255 * I2CVDD*

where I2CVDD is the power supply connected to pin I2CVDD (5 or 3.3 V).

AGC2LEVEL: 0x92 to 0x93 (read)

These registers allow the users to monitor the current value of agc2 gain.

	b7	b6	b5	b4	b3	b2	b1	b0
0x92	mantissa (10:3)							
0x93	mantissa (2:0)				exponent (4:0)			

AGC2LEVEL is coded in a floating format with a mantissa coded with 11 unsigned bits and an exponent coded with 5 signed bits, defined as follows:

exponent = floor (log_2(agc2gain))

mantissa = floor (agc2gain x $2^{-exponent}$ x 1024)

Exponent takes its value in the range -6 to 13, and mantissa takes its value in the range 1024 to 2047.

Timing Waveforms

Output Interface

Figure 14. Parallel MPEG2-TS output

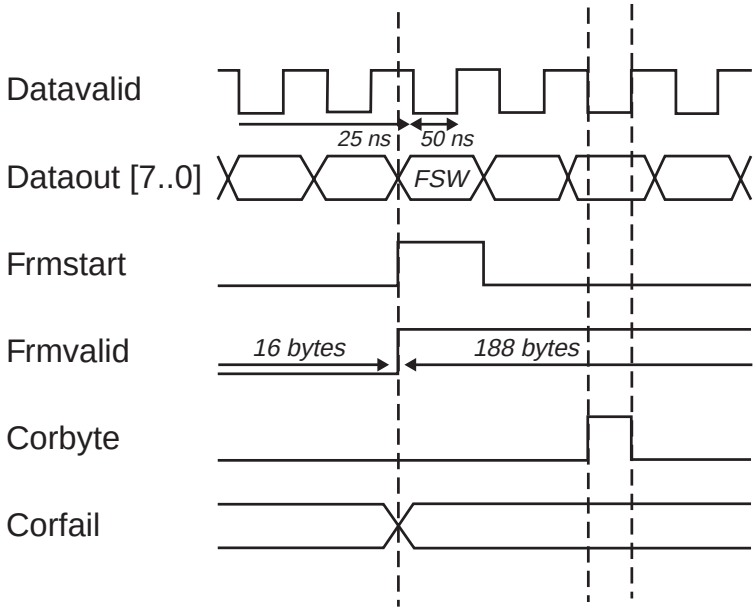


Figure 15. Serial output mode

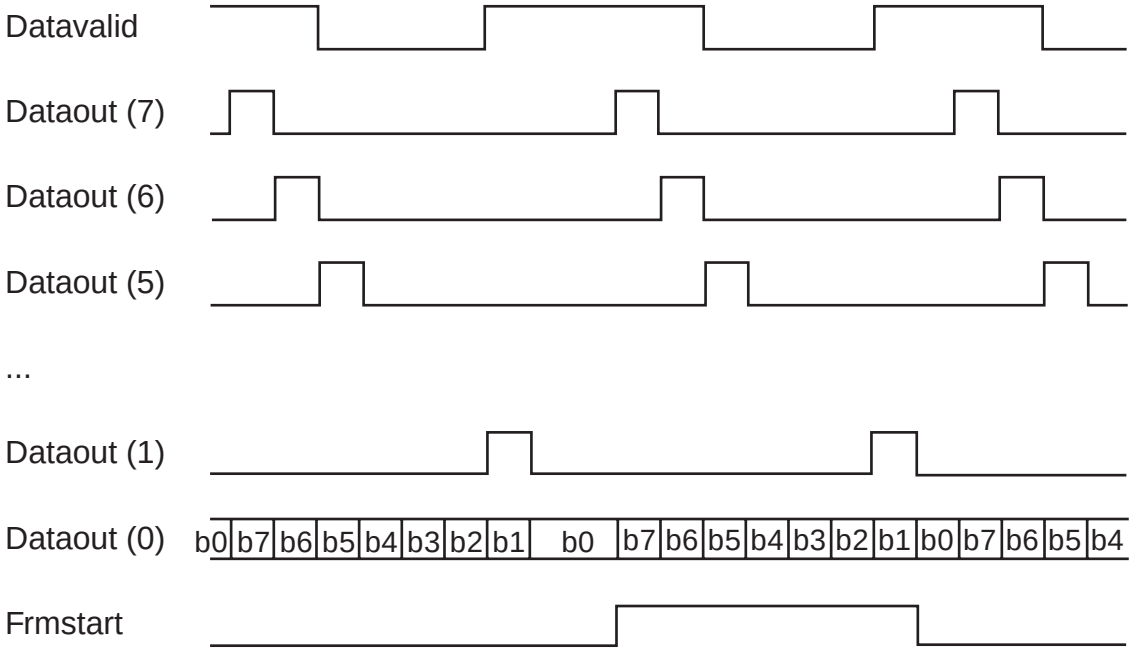
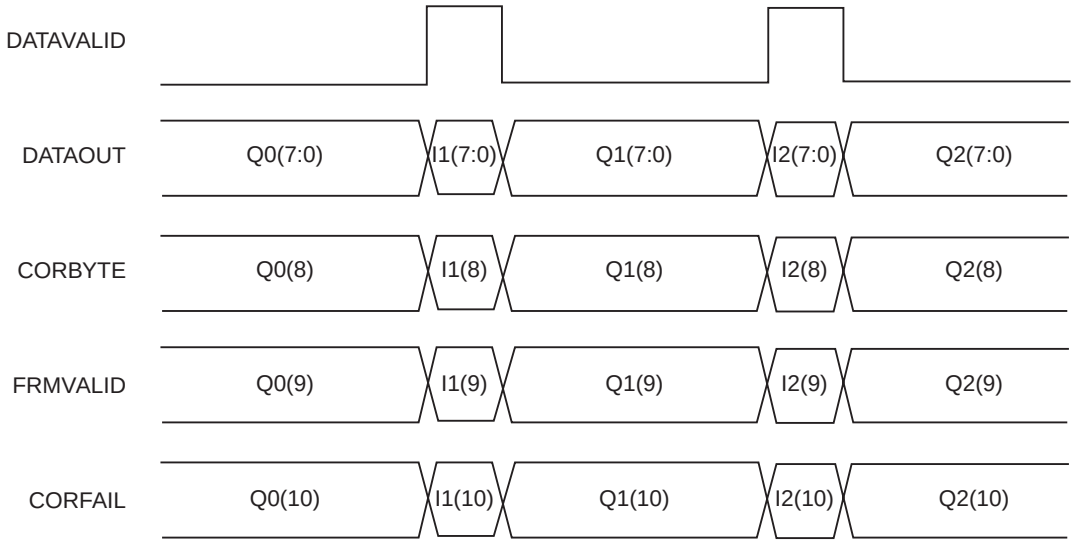
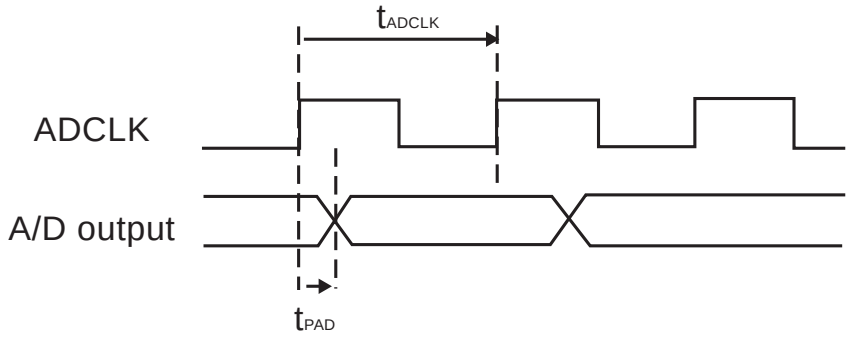


Figure 16. Constellation Output Mode



Input Interface (with external A/D converter)

Figure 17. External A/D converter input



The input pin SAMPLEPHASE must be connected to Ground or VDD, as indicated in the table below (see Figure 17 for the definition of t_{PAD} and t_{ADCLK}).

Table 23.

Samplephase	t_{PAD} Typ
0	$t_{PAD} \le t_{ADCLK}/4$ or $t_{PAD} \ge 3t_{ADCLK}/4$
1	$t_{ADCLK}/4 \le t_{ADCLK} \le 3t_{ADCLK}/4$

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