IC Packaging/Intro

- ICs are at the core of a modern digital system
- Many systems fit entirely on a single IC (SOC)
  - a single $(15\text{-mm})^2$ chip can hold several million gates (1997)
  - a simple 32-bit CPU can be realised in an area of $1mm^2$
- Biggest limitation of a modern digital IC: Large reduction in signal count between on-chip wires and package pins. Typical IC
  - 10^4 wiring tracks on each of four metal layers
  - 10^3 signals can leave the chip (for cheaper packages: 40..200)
  - Chips are often “pad-limited”. Peripheral-bonded chips. Chip area increases as the square of the number of pads

IC Packaging/Intro

- Most ICs are bonded to small IC packages

  Although it is possible to attach chips directly to boards. Method used extensively in low-cost consumer electronics. Placing chips in packages enables independent testing of packaged parts, and eases requirements on board pitch and P&P (pick-and-place) equipment.

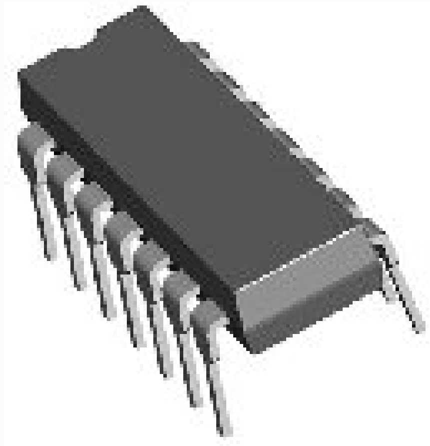
- IC Packages
  - inexpensive plastic packages: <200 pins
  - packages with >1000 pins available

    (e.g. Xilinx FF1704: 1704-ball flip-chip BGA)

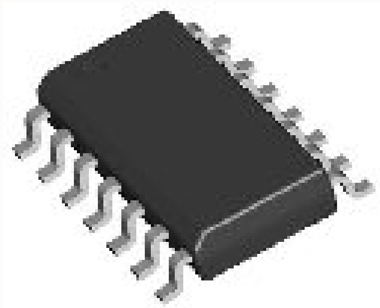
- IC Packaging Materials
  - Plastic, ceramic, laminates (fiberglass, epoxy resin), metal

IC Packaging/Categories

- IC package categories:
  - **PTH** (pin-through-hole)
    Pins are inserted into through-holes in the circuit board and soldered in place from the opposite side of the board
    - » Sockets available
    - » Manual P&P possible

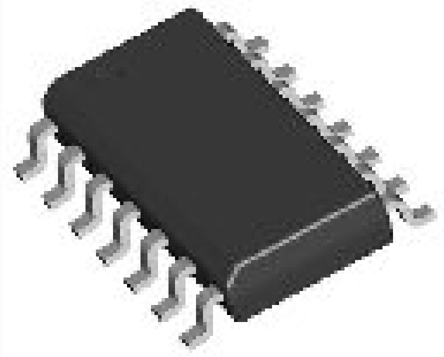


  - **SMT** (surface-mount-technology)
    SMT packages have leads that are soldered directly to corresponding exposed metal lands on the surface of the circuit board
    - » Elimination of holes
    - » Ease of manufacturing (high-speed P&P)
    - » Components on both sides of the PCB
    - » Smaller dimensions
    - » Improved package parasitic components
    - » Increased circuit-board wiring density



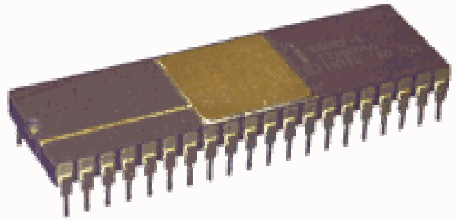
SMT packages offer many benefits and are generally preferred.

IC Packaging/Materials



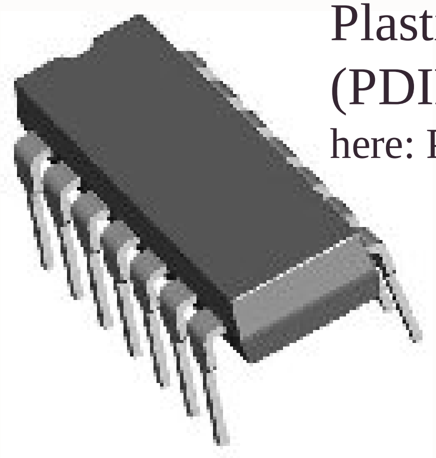
- IC packaging material: Plastic
  - die-bonding and wire-bonding the chip to a metal lead frame
  - encapsulation in injection-molded plastic
  - inexpensive but high thermal resistance
  - **Warning**: Plastic molds are hygroscopic
    - » Absorb moisture
      Storage in low-humidity environment. Observation of factory floor-life
    - » Stored moisture can vapourise during rapid heating
      can lead to hydrostatic pressure during reflow process. Consequences can be: Delamination within the package, and package cracking. Early device failure.

IC Packaging/Materials



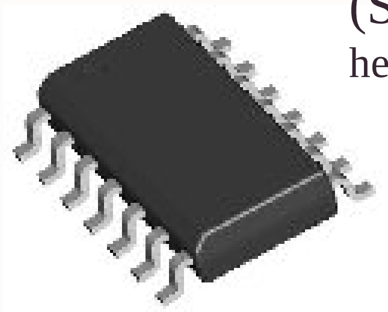
- IC packaging materials: Ceramic
  - » consists of several layers of conductors separated by layers of ceramic (Al_2O_3 “Alumina”)
  - » chip placed in a cavity and bonded to the conductors
    Note: no lead-frame
  - » metal lid soldered on to the package
  - » sealed against the environment
  - » ground layers and direct bypass capacitors possible within a ceramic package
  - » high permittivity of alumina ($\varepsilon r=10$)
    Note: High permittivity leads to higher propagation delay!
  - » expensive

IC Packaging/Popular IC Packages

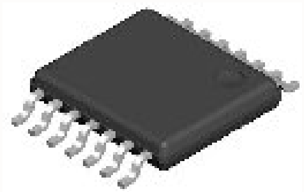


Plastic Dual-In-Line (PDIP)
here: PDIP14

SC70
here: SC70-5

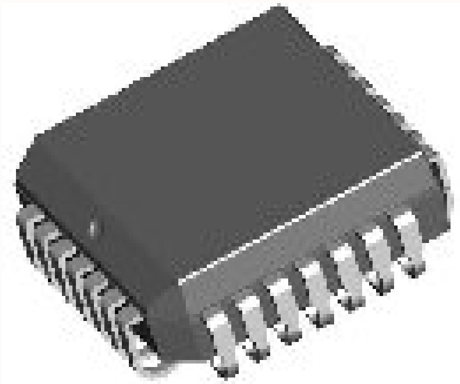


Small Outline Integrated Circuit (SOIC)
here: SO14

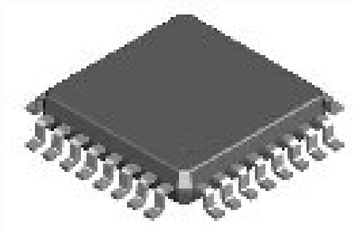


Thin Shrink Small Outline (TSSOP)
here: TSSOP14

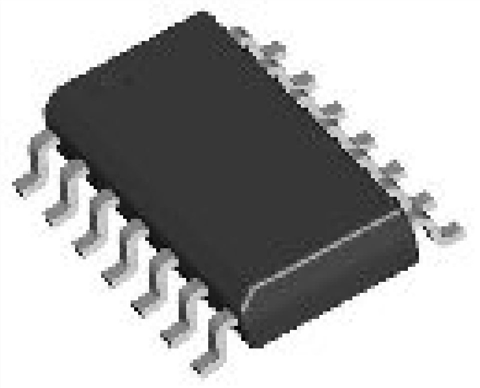
Plastic Lead Chip Carrier (PLCC)
here: PLCC28



Thin Quad Flat Package (TQFP)
here: TQFP32

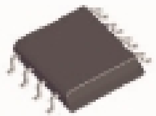


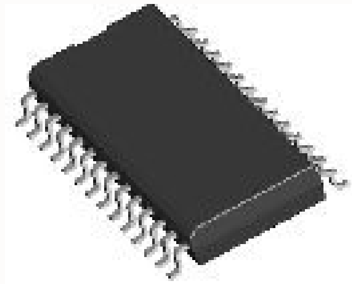
IC Packaging/Popular IC Packages



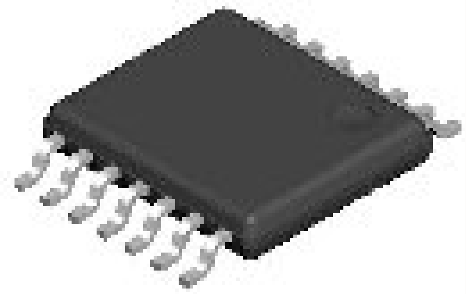
Small Outline Integrated Circuit (SOIC)

- Shown: SO14, but available from SO8..SO28
- Gull-wing leads
- Popular, cost effective, and widely available IC package for low-pin-count ICs
- Dimensions: 8.6mm x 3.9mm x 1.75mm
- Pin-to-pin: 1.27mm (50mil)



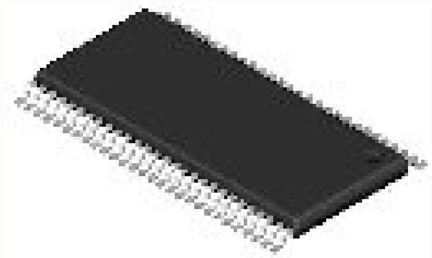


IC Packaging/Popular IC Packages



Thin Shrink Small Outline (TSSOP)

- •Shown: TSSOP14, but available up to TSSOP64
- •Popular, cost effective, and widely available IC package for low-profile applications
- •Dimensions: 5.0mm x 4.4mm x 1.2mm
- •Pin-to-pin: 0.65mm (25mil)



IC Packaging/Popular IC Packages

Ball Grid Arrays (BGA)

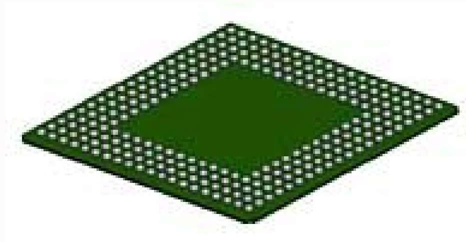
•Shown: BGA54
•Available pin count >1700
•Advanced IC package for high-density low-profile applications
•Chip-scale package (CSP)
•Dimensions: 8.0mm x 5.5mm x 1.4mm
•Pin-to-pin: 0.8mm
•Low lead inductance

Altera Ultra-Fine-Line BGA
•Pin-Count: 169
•Dimensions 11mm x 11mm
•Profile: 1.2mm

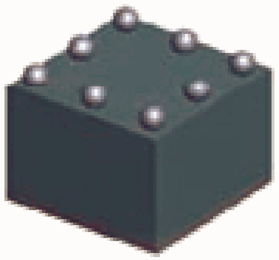
Challenges:
•Integrity of solder joints
•Solder joint inspection (X-ray)
•Availability of 2nd source
•Routing

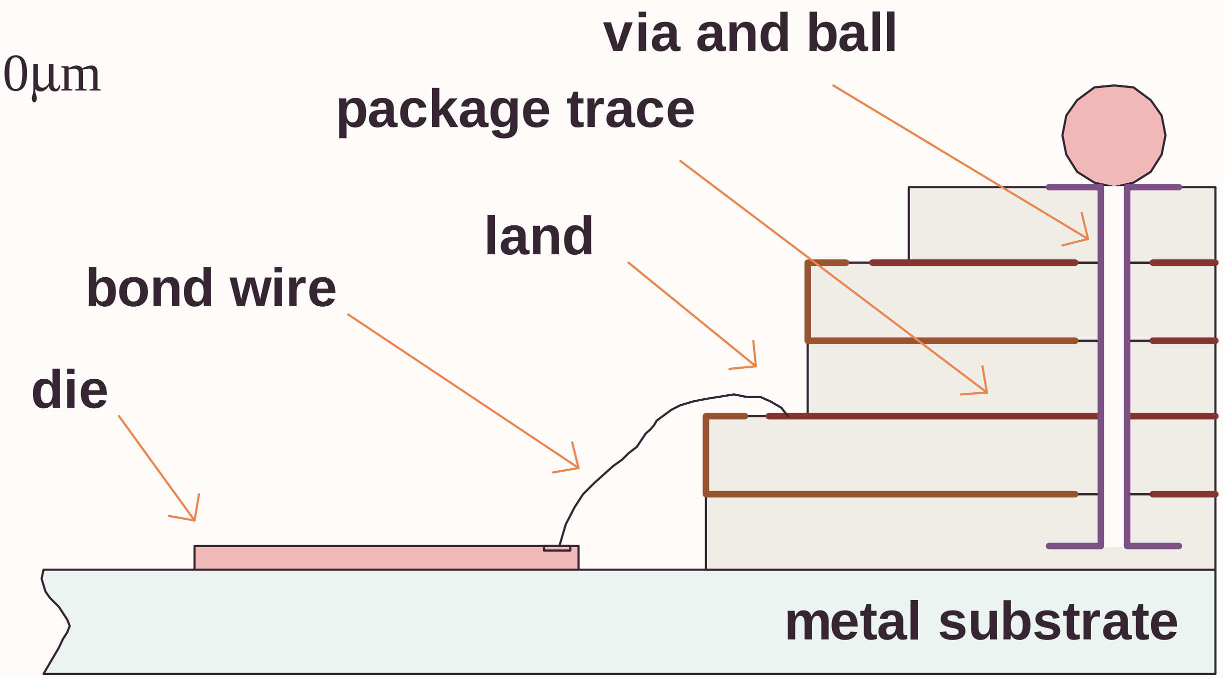
IC Packaging/BGA Physical Construction

Physical construction of a BGA

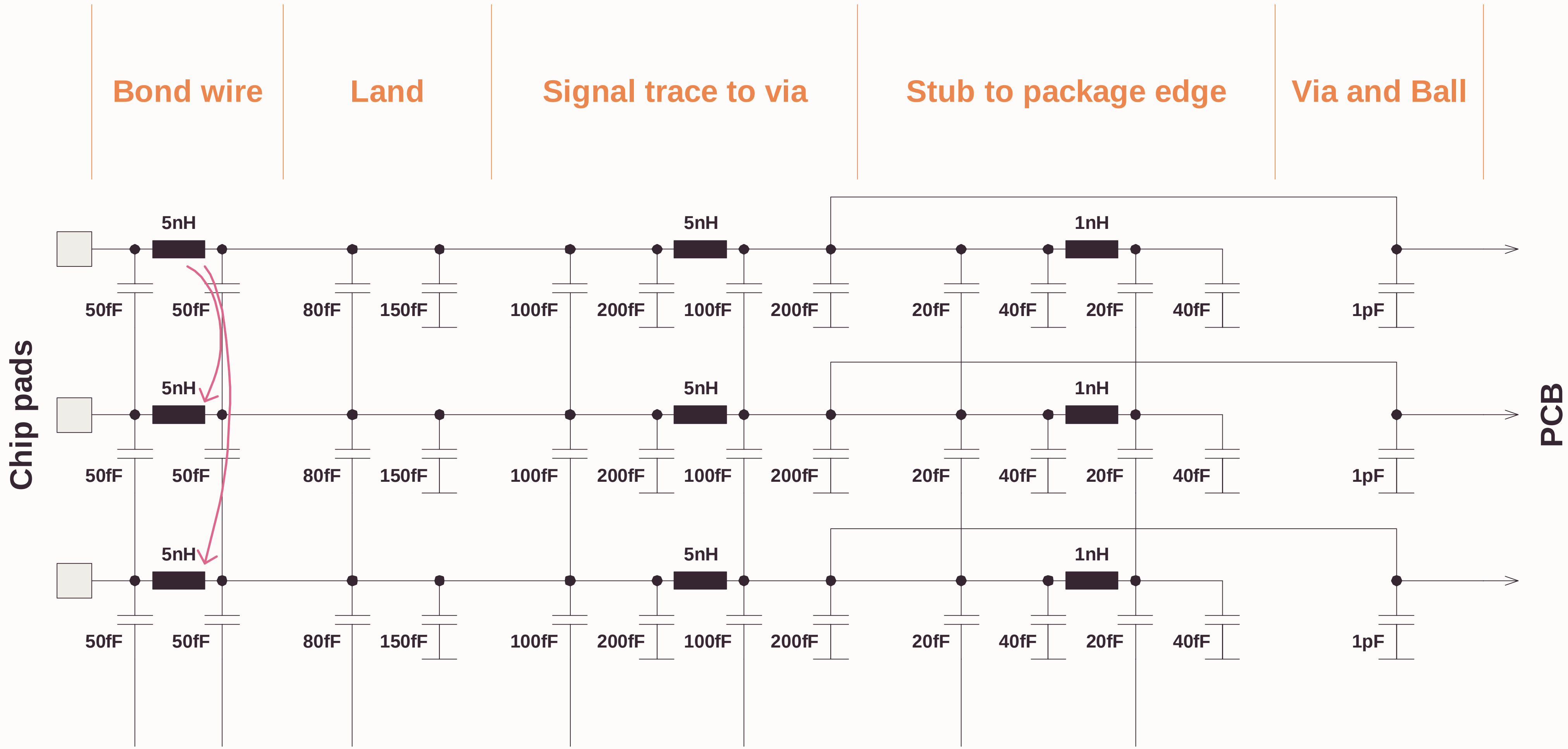


- •Shown: Type-II BGA (cavity-down design)
- •Interconnect: multi-layer laminated construction
- •Die bonded onto a metal heat slug
- •Solder balls make connection to a PC board
- •50µm bond wires
- •Copper conductor thickness 20µm
- •Layer separation 150µm





IC Packaging/BGA Electrical Model



Complexity of a detailed package model! For critical applications many more details are required (e.g. bond wire resistance). Field solver (e.g. LINPAR)!

IC Packaging/Thermal Resistances

- Comparison of thermal resistances

Package	**RthJC** **K/W**	**RthJA (still air) K/W**	**RthJA (0.5m/s) K/W**	**RthJA (2.0m/s) K/W**
DIP16	19	48		
SOIC24	17	77		
PLCC44	10	33	31	27
PQFP44	15	48	46	42
BGA256	13	40	38	33

IC Packaging/Electronic Assembly (1981)

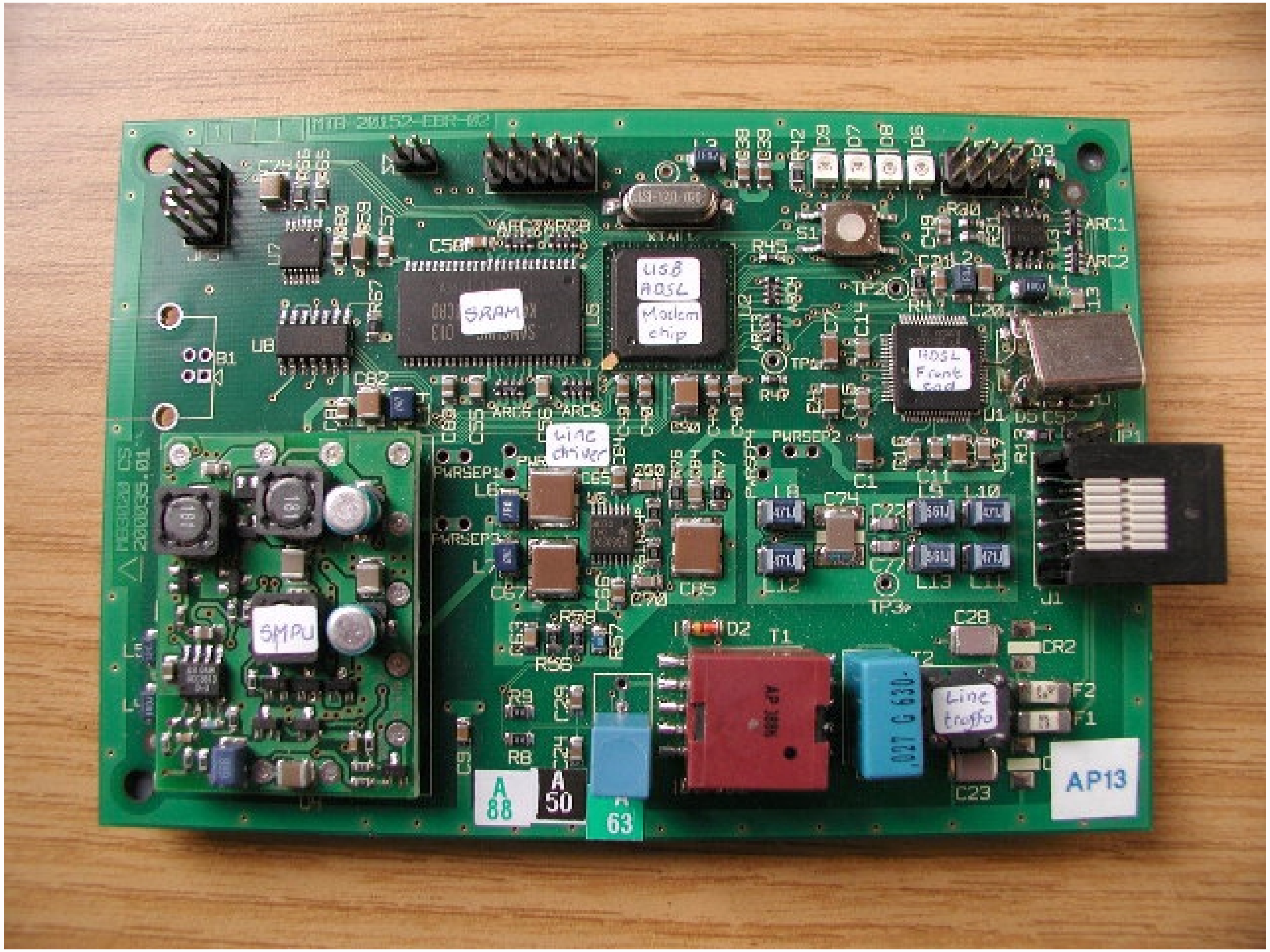
IBM PC 1981

•IC packaging: DIL only!

•Processor: 8088

•Memory: 256kB

IC Packaging/Electronic Assembly (2000)



Low-density electronic assembly with various IC packages

- SO
- TSSOP
- QFP
- BGA

Measurement Techniques

- Primary measurement tool: Oscilloscope
  Other lab tools: Logic Analyser, Gain-Phase Analyser, Spectrum Analyser…
- Visualisation of electrical signals in the time domain
  - Visualisation of voltages through voltage probes (standard)
  - Visualisation of currents through current probes and current amplifiers
- Advanced scopes: Visualisation of signals in the frequency domain (FFT)

Measurement Techniques/DSO

Features of modern scopes

- •Type: Digital Storage Oscilloscope (DSO)
- •Channels: 2 (standard), 4 (better)
- •Bandwidth: 100MHz … >5GHz
- •Sampling rate: 200MS/s …
- •Memory: 1kpts … Mpts
- •Advanced triggering
- •Signal analysis
- •8/10/12 bit vertical resolution with 1% vertical precision
- •Export of data (floppy disk)
- •Remote control (GPIB)

High speed digital design:
Use a DSO with adequate bandwidth!

Digital storage oscilloscopes allow to capture and view events that may only happen once. Note the DSO's relatively poor vertical characteristics.

Measurement Techniques/DSO

Primary Limitations of Scopes

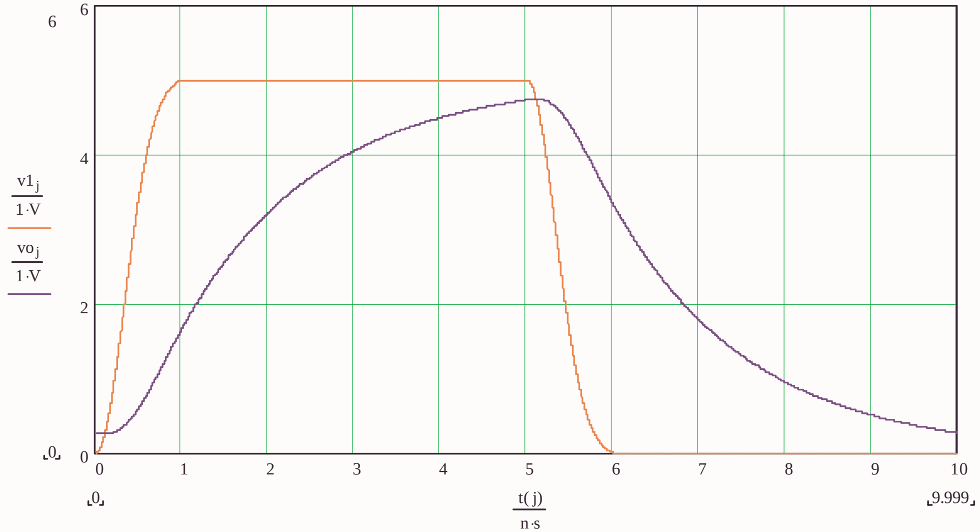
- Vertical sensitivity. Most scopes offer a range of 10mV/div … 10V/div
- Limited bandwidth

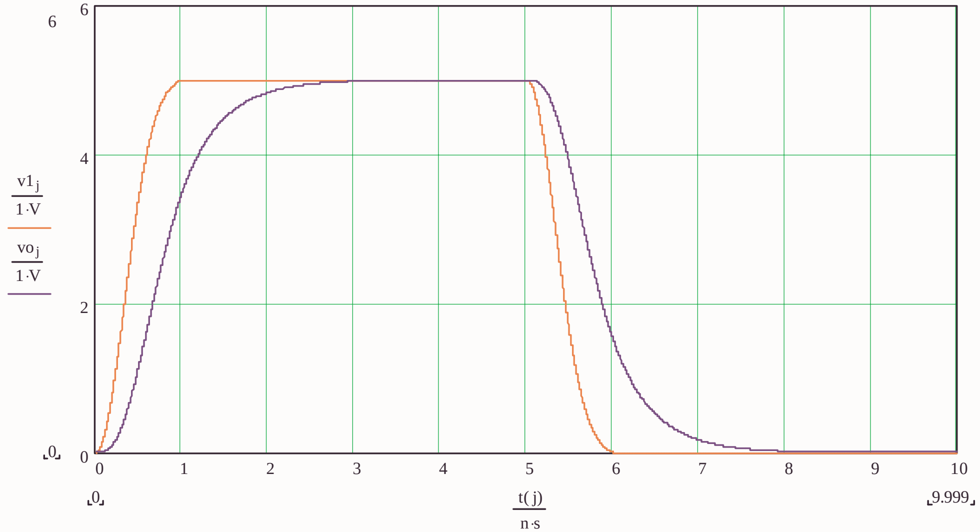
With respect to High-Speed Digital Design

- Vertical sensitivity of DSOs adequate for most digital situations
- Bandwidth!

What do bandwidth numbers mean?
Can you measure a 99MHz signal using a scope with a 100MHz bandwidth?
What exactly do you mean by "a 99MHz signal". Sine wave? Bitrate?

Measurement Techniques/DSO/Bandwidth





Example Parameters

•Signal: fcycle=100MHz with Tr/Tf=1ns
•Top: Scope BW = 100MHz
•Bottom: Scope BW = 350MHz

Signal distortion:

Signal harmonics are attenuated and phase-shifted by different amounts.

remember that $f_{knee} \approx \dfrac{0.35}{Tr_{10\%-90\%}}$

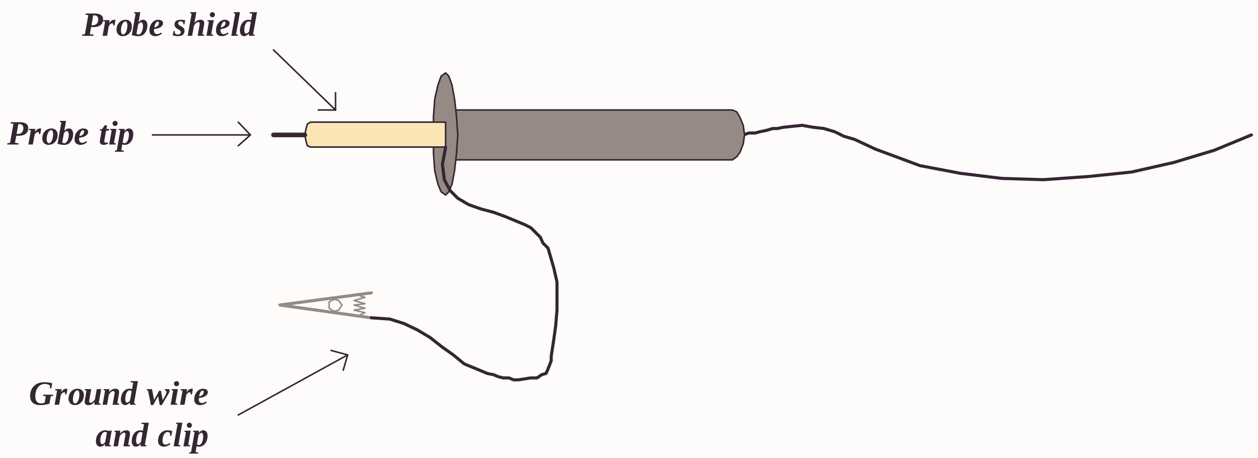
Measurement Techniques/DSO/Probes

Scope probes establish a connection between the circuit under test (CUT) and the scope.

Mission of scope probes: “Extract minimal energy from the CUT and transfer it to a scope with maximum fidelity”.

Scopes can only measure what they can “see” at their input ports. Choosing proper probes is vital for your measurement system.

Measurement Techniques/DSO/Probes

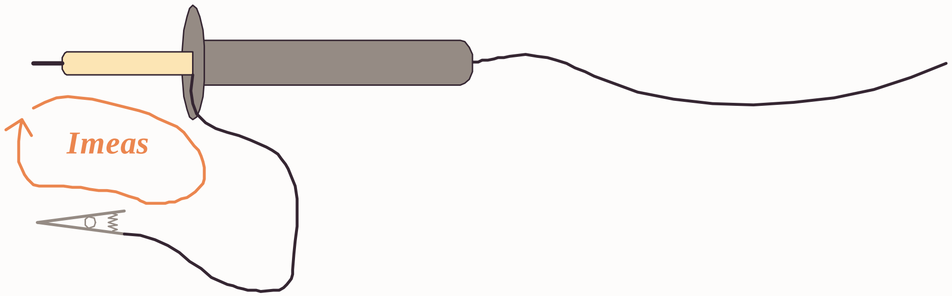


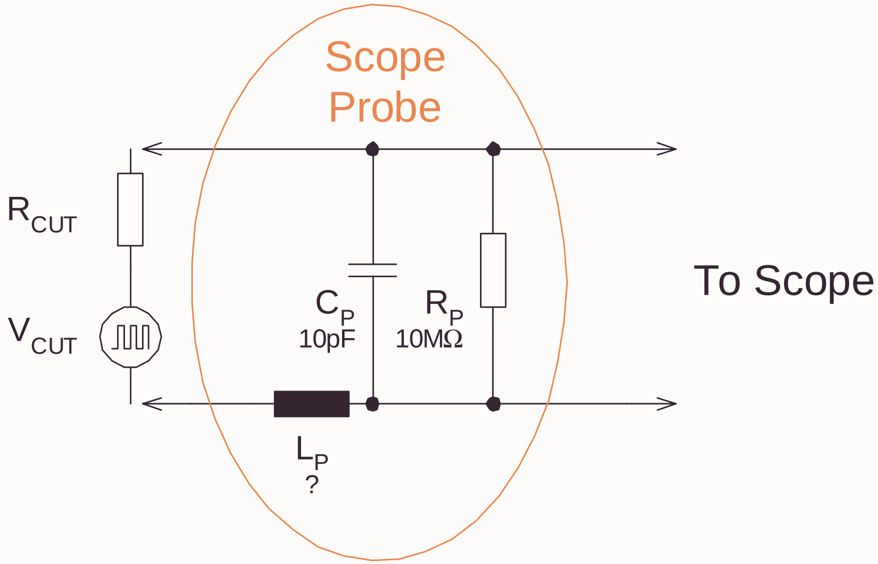
Primary factor degrading the performance of scope probes when used in high-speed digital electronics:

- Inductance of the ground wire

Watch out:
Bandwidth specifications of scope probes do NOT include the ground wire !

Measurement Techniques/DSO/Probes





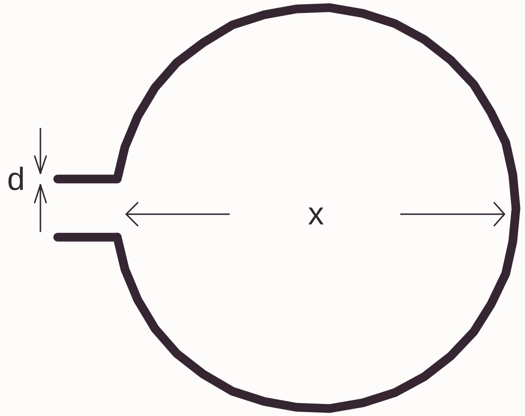
How does the inductance of the ground wire affect measurements?

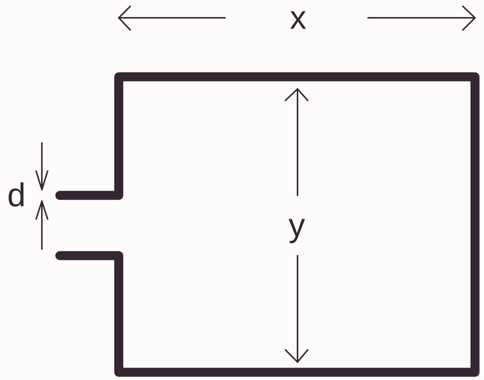
•Estimation of the ground loop inductance of the scope probe…

•Estimation how the ground loop inductance affects the rise time...

Measurement Techniques/Loop inductances

Estimation of self inductance of circular and rectangular loops:





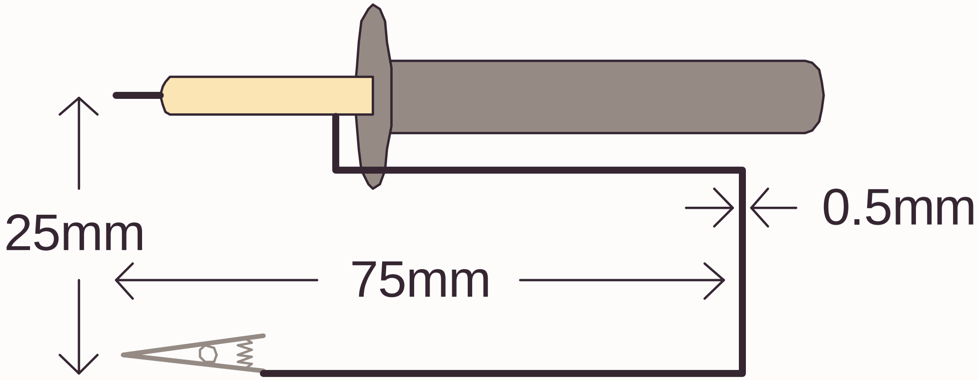
$$L_{circ} \approx 614 \frac{nH}{meter} \cdot x \cdot \left(\ln\left(\frac{8x}{d}\right) - 2 \right)$$

Note:
•valid for x>>d
•small influence of wire diameter

$$L_{rect} \approx 400 \frac{nH}{meter} \cdot \left(x \cdot \ln\left(\frac{2y}{d}\right) + y \cdot \ln\left(\frac{2x}{d}\right) \right)$$

Note:
•valid for x>>d and y>>d
•small influence of wire diameter

Measurement Techniques/Loop inductances



Example Parameters

•500MHz passive probe
•Ground wire 25mm x 75mm x 0.5mm
•Probe capacitance 10pF

•Self inductance of ground wire loop is around 200nH (!)
•Self inductance and capacitance of the probe result in a signal rise time of 4.7ns
•The knee frequency of this signal is around 74MHz. The 500MHz probe has been degraded to a 74MHz probe by the ground wire.

The bandwidth of a passive probe can be substantially reduced by ground wires!

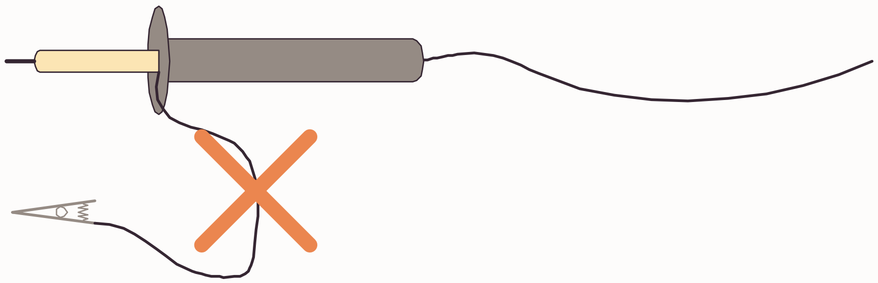
Measurement Techniques/Loop inductances

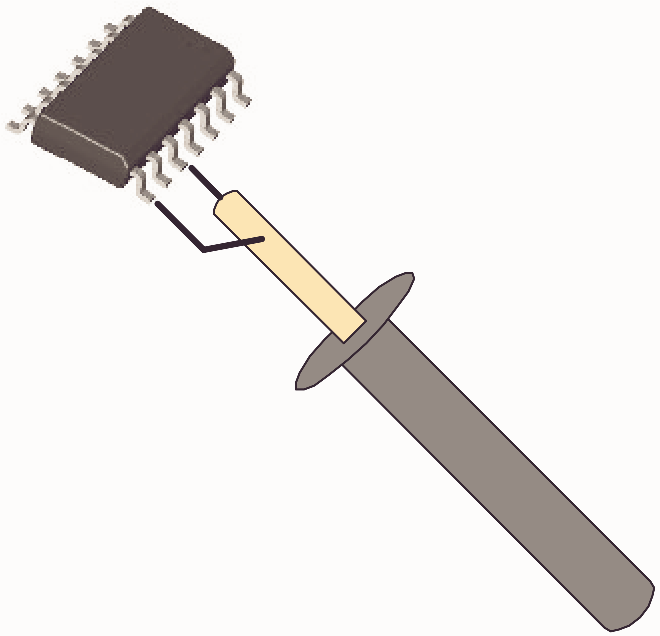
Therefore...

•Don’t use ground wires for measuring high-speed digital signals

•Use special probe tips (bare probe tip with probe collar directly grounded to circuit board)

•In general: Minimise loop areas





Measurement Techniques/DSO Pitfalls

More scope probe pitfalls...

- Capacitive loading of CUT due to scope probe.

Example: A 10pF probe represents an impedance of 136Ω to a signal with Tr=3ns

- Pickup of EM fields
    - For minimum magnetic field pickup: minimise ground loop area
    - Electric field pickup: hardly ever a problem in digital electronics
    - Popular trick of designers: Use scope probe as an EM field sensor
- Noise pickup due to probe shield currents

Remember: Composite rise time of scope probe and scope...

$$Tr_{composite} = \sqrt{\sum_{i=1}^{n} Tr_i^{\ 2}} = \sqrt{T_{probe}^{\ 2} + T_{scope}^{\ 2}}$$

Transmission Lines/Overview

- Transmission Lines (TL)
  - Shortcomings of ordinary point-to-point wiring
    - Distortion, Emi, Crosstalk
  - Modelling and Partial Differential Equations
  - Characteristic Impedance and Propagation Constant
  - Popular Types
  - Classification
  - Infinite Length Uniform Transmission Lines
    - Lossless Transmission Lines
    - Lossy Transmission Lines

TL/Wires

- A few words about wires…
  - Wires are used in digital systems to
    - communicate signals from one place to another
    - distribute power, clocks, etc.
  - Wires dominate a modern digital system in terms of
    - speed (propagation delay)
    - power (driver, termination)
    - cost (use right cost model…. expensive mistakes!)
  - Wires may not be equipotential regions
  - Real wires have distributed parasitics (R, L, C)
  - If not handled properly these parasitics will
    - add delay, cause oscillations, degrade signal quality…

With proper engineering techniques, wires can be easily tamed…

TL/Wiring in Digital Systems

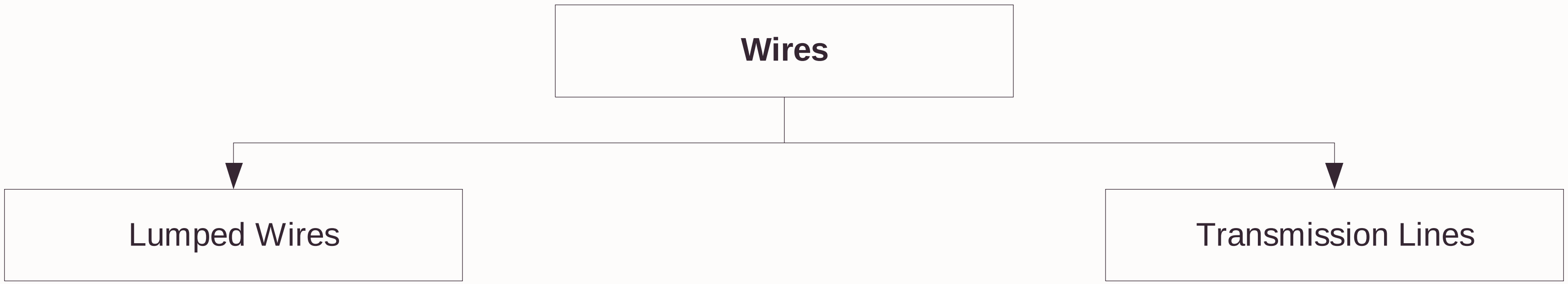
- Wiring Hierarchy in Digital Systems
  - chips (metal layer, poly)
  - carrier (bond wires)
  - circuit boards (PCB)
  - chassis (shared mechanical support for PCBs)
    (connected through backplanes, motherboards, cables)
  - cabinet
- Physical characteristics of wires at each level determines
  - electrical properties
  - cost
  - maximum signal density
    (non-uniform increase in wire density: IC 22%/year vs PCB 7%/year)

TL/Classification of Wires

Remember…

Effective length of rising edge

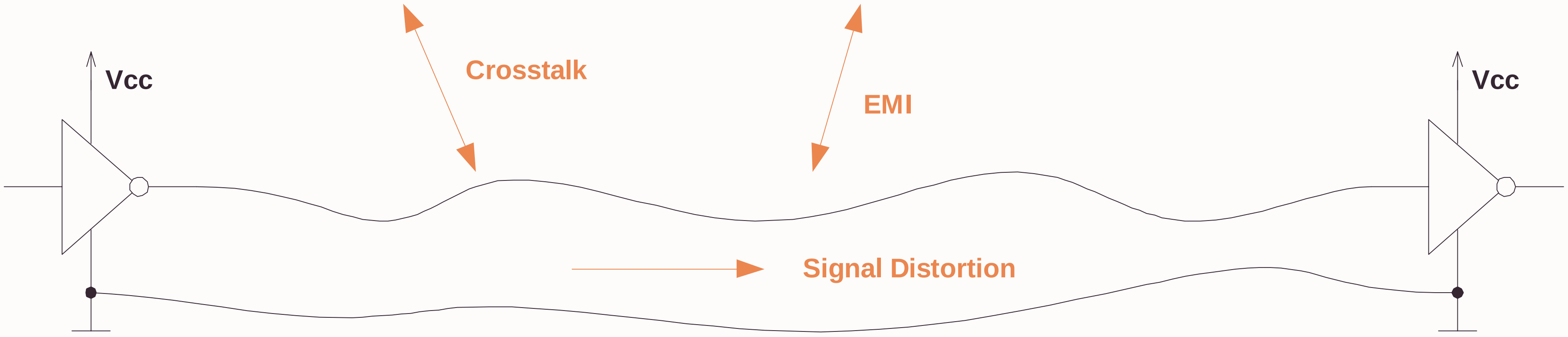
$$lr = Tr \cdot vp$$



- if l < lr/6
  ⇨ System behaves mostly in a lumped fashion

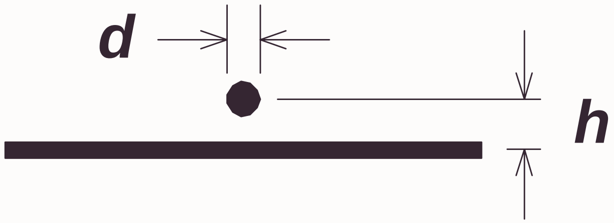
- if l > lr/6
  ⇨ System behaves mostly in a distributed fashion

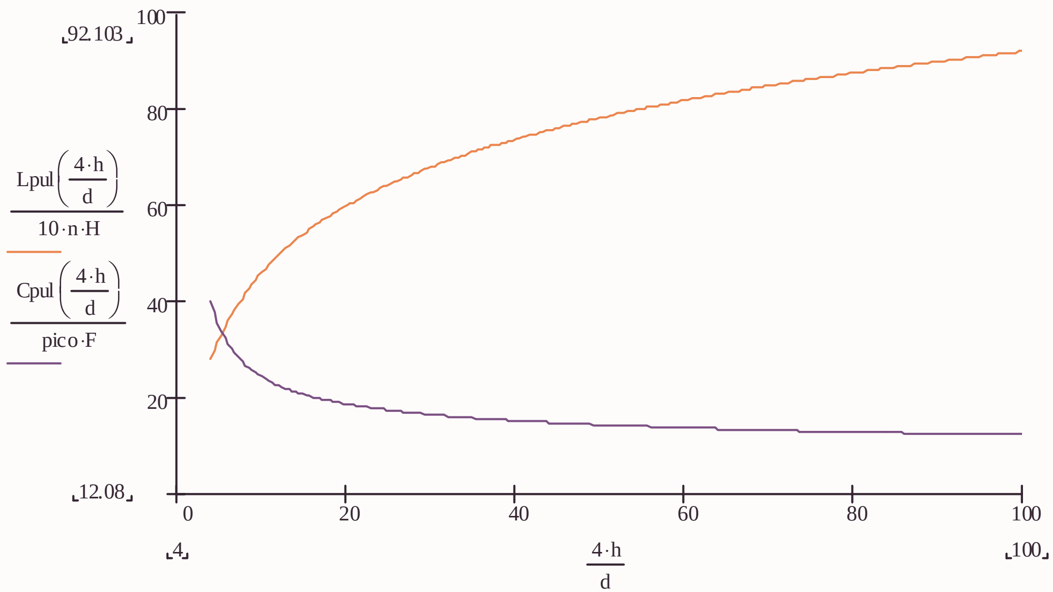
TL/Wiring Problems



- Problems of ordinary point-to-point wiring (example: wire-wrap prototyping)
  - Signal distortion (due to lumped or distributed parasitic wire components)
  - Radiated and conducted noise (EMI). Emission and susceptibility.
  - Crosstalk (inductive, capacitive)
- Common reasons for problems:
  - Large loops: large inductances
  - Vicinity to ground or other circuits: Capacitances

TL/Approximations for Suspended Wire





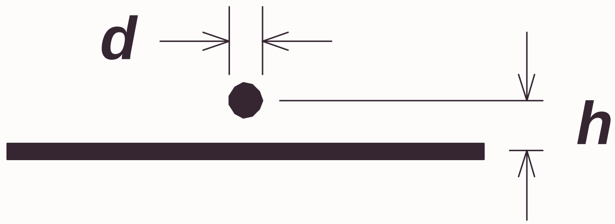
Capacitance and Inductance (per unit length) of round wire suspended above ground plane (valid for h>d):

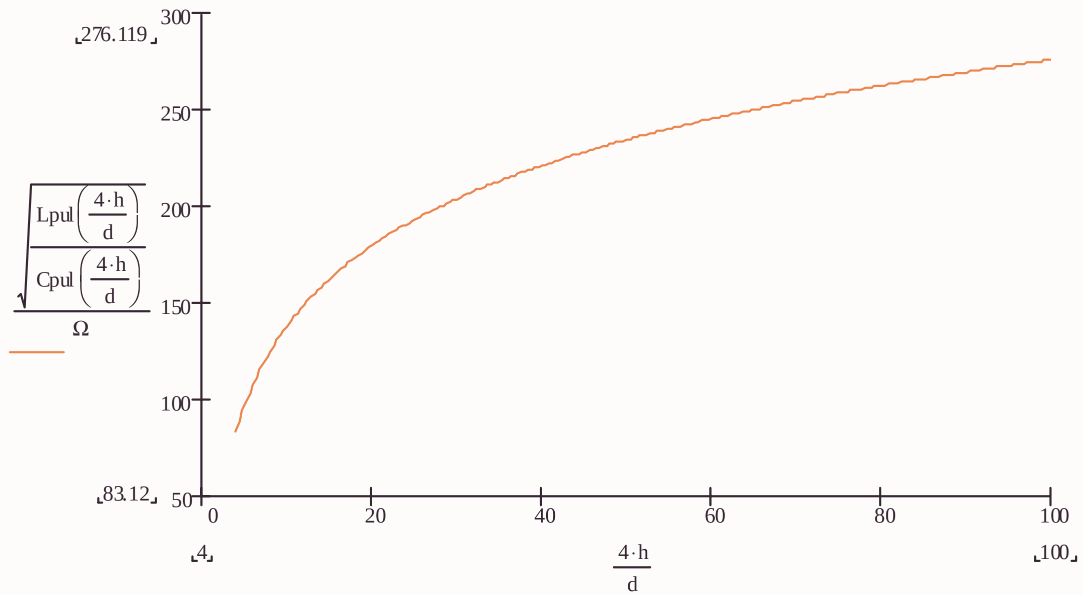
$$C_{rwire\ pul} \approx 2\pi \cdot \varepsilon 0 \cdot \left(\ln\left(\frac{4h}{d} \right) \right)^{-1} \approx 55.6\, {}^{pF}\!\!/\!_{meter} \cdot \left(\ln\left(\frac{4h}{d} \right) \right)^{-1}$$

$$L_{rwire\ pul} \approx \frac{\mu 0}{2\pi} \cdot \ln\left(\frac{4h}{d} \right) \approx 200 \frac{nH}{meter} \cdot \ln\left(\frac{4h}{d} \right)$$

(assumed dielectric: vacuum/air)

TL/Approximations for Suspended Wire





Interestingly:

$$C_{rwire\ pul} \cdot L_{rwire\ pul} \approx const$$

Indicates that propagation delay and propagation velocity is approximately independent of h and d.

$$\frac{L_{rwire\ pul}}{C_{rwire\ pul}} \neq const$$

Indicates that the characteristic impedance is a function of h and d.

TL/Point-to-Point Wiring Example

Example Breadboarding of Prototypes:

•Wire-wrap prototype using AWG30 wire (diameter 250μm)

•Average height above ground: 5mm

•Average wire length: 10cm.

•Resulting average self inductance: L=88nH

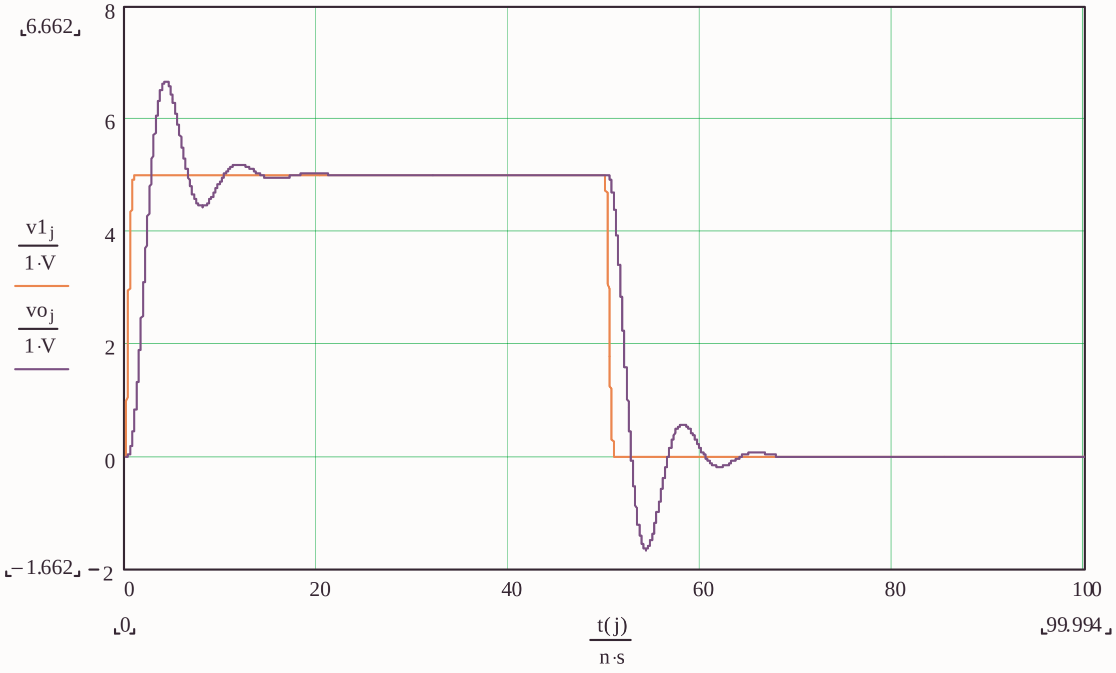
TL/Point-to-Point Wiring Example

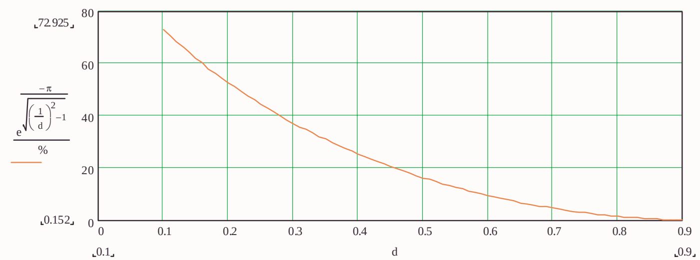
Example (continued):

•Average self inductance: L=88nH

•Typical load capacitance C=15pF. TTL driver with 50Ω output impedance.

•d=0.33. Overshoot 34%





TL/Point-to-Point Wiring Example

Example (continued):

•If height above ground is reduced to 120μm (resembling a ***transmission line on PCB***):

•L=14nH. d=0.82. Overshoot 1%.