In the drivers introduced under [9], [47] and [61] the IGBT/MOSFET dv/dt and di/dt are detected and fed back to the driver (Figure 3.65).

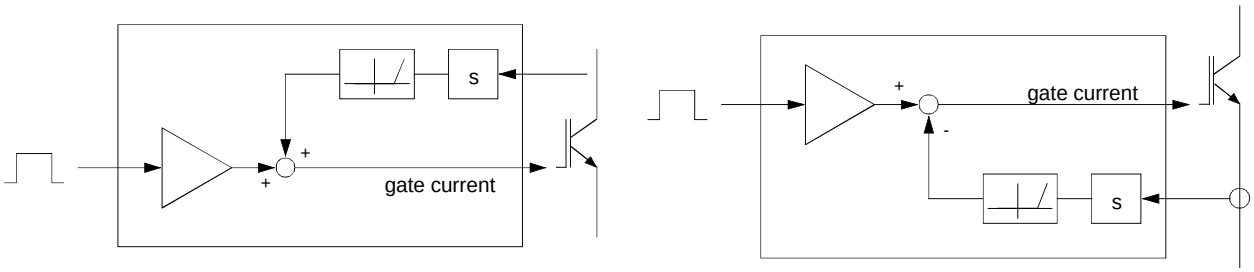


Figure 3.65 Direct dv/dt- and di/dt-detection

Here, the information on di/dt or dv/dt is got by inductance at the emitter or by capacitance at the collector, respectively.

*Overvoltage limitation between control terminals*

Overvoltage limitation between control terminals is required for keeping up the maximum gate-emitter/ gate-source voltage on the one hand, and for limitation of the dynamic short-circuit current amplitude on the other hand.
Figure 3.66 shows a summary of simple circuit variants. For the sake of optimized efficiency the limitation circuits should be laied out for low inductance and be attached as close as possible to the gate.

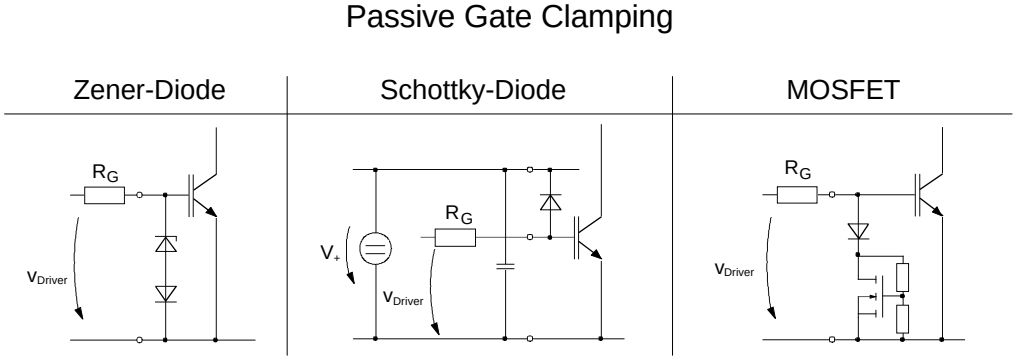


Figure 3.66 Simple gate voltage limitation circuits [194]

### *3.6.3.3 Overtemperature detection*

Direct measurement of the junction temperature is only possible, if the temperature sensor is attached very close to the semiconductor component (e.g. by monolithic integration or by connecting of the temperature sensor and the power semiconductor chip).
Information on temperature can then be got from the evaluation of diode or thyristor blocking currents.
However, technologies of that kind have only been applied in smart-power components so far.

In transistor power module applications temperatures are measured either outside the module from the heatsink or inside the module by temperature-dependent resistors close to the power semiconductor chips (e.g. with SEMIKRON SKiiP/ MiniSKiiP).
Because of the given thermal time constants, only information about the average temperature is given (dynamic temperature measurement is not possible).

If given reference values (which are extremely application-specific) in converters are exceeded, the system can react by immediate turn-off or by operation with reduced power.

## 3.7 Parallel and series connection of MOSFET, IGBT and SKiiPPACK modules

### 3.7.1 Parallel connection

#### *3.7.1.1 Problems of current sharing*

To improve the current capability of power electronic switches, IGBT and MOSFET modules can be connected in parallel.
By paralleling power modules, the transistors and necessary inverse diodes or free-wheeling diodes are also paralleled. As parallel connection of fast diodes had already been dealt with in chapter 1.3.5.2, only special characteristics of IGBTs/ MOSFETs will be discussed to in the following.

Maximum utilization of the switch generated by parallel connection will only be achieved in the case of ideal static (i.e. in the forward operation) and dynamic (i.e. at the moment of switching) symmetrization of the single modules (current sharing).
Therefore, optimal symmetry conditions are of major importance for parallel connections in practice.

Current sharing is mainly effected by the following factors:

| Factor | Influence on | |
|---|---|---|
| | static symmetry | dynamic symmetry |
| <u>IGBT/MOSFET-parameters</u> | | |
| $v_{CEsat} = f(i_C, v_{GE}, T_j)$ or $R_{DSon} = f(v_{GS}, T_j)$ | **x** | |
| $i_C = f(v_{GE}, T_j)$ or $i_D = f(v_{GS}, T_j)$ | | **x** |
| $v_{GE(th)}$ or $v_{GS(th)}$ | | **x** |
| $t_{d(on)}$, $t_{d(off)}$, $t_r$, $t_f$ (in connection with driver parameters) | | **x** |
| <u>Commutation circuit</u> | | |
| Total loop inductance (inside the module + outside the module) | **(x)** | **x** |
| <u>Driver circuit</u> | | |
| Output impedance of driver (including gate series resistances) | | **x** |

| | |
|---|---|
| Total loop inductance<br>(inside the module + outside the module) | **x** |
| Driver circuit inductance carrying collector/ drain current | **x** |

*Influence of saturation voltage and $R_{DS(on)}$ respectively*

The on-state voltage induced during stationary forward on-state is the same for both paralleled transistors. Current distribution is dependent on the tolerances of the output characteristics.
Figure 3.67 shows how the total load current is distributed over two paralleled IGBTs with different output characteristics.

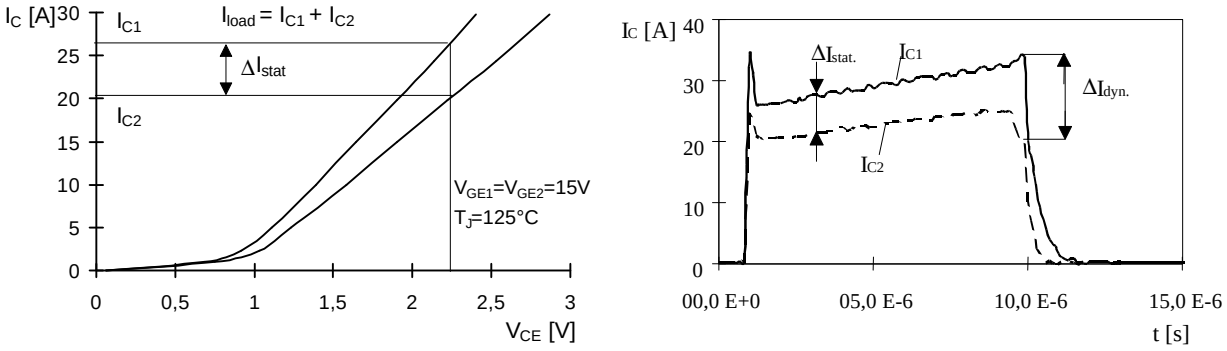


Figure 3.67 Static current distribution over two paralleled IGBTs with different output characteristics

In the beginning, the major current share is conducted by the transistor with the lower saturation characteristic, which is therefore subject to higher forward and switching losses, and, by consequence, the junction temperature will increase rapidly.
In this respect, the temperature coefficient (TC) of the saturation voltage is of decisive importance. If the TC is positive, i.e. if the saturation voltage rises together with the temperature, the current will be shifted to the transistor which had carried the minor current share in the beginning. Finally, the current will (ideally) be evenly distributed over the paralleled transistors.
Therefore, power semiconductors with a positive TC are preferably used for parallel connections.
The TC of NPT IGBTs is positive over almost the whole rated current range. The same goes for the $R_{DSon}$ of MOSFETs, featuring a positive TC by principle.
In contrast to that, the TC of PT IGBTs is negative over almost the whole rated current range. Here, good thermal coupling between paralleled modules is substantial.

*Influence of the transfer characteristic $i_C = f(v_{GE}, T_j)$ and $i_D = f(v_{GS}, T_j)$ respectively*

Deviations in the transfer characteristics, threshold voltages and switching delay times will lead to dynamic asymmetries at the moment of switching and, consequently, to different switching losses, especially during turn-off.

Figure 3.68 shows the example of deviating transfer characteristics of paralleled NPT IGBTs and thereby caused dynamic current asymmetry during turn-off.

Due to the common gate voltage during the Miller process, the IGBT with the steeper transfer characteristic will conduct the major current share during dynamic current distribution and is therefore subject to higher turn-off power dissipation.

While the positive on-state voltage TC of NPT-IGBTs is supporting parallel connections, the steep transfer characteristic and high switching speed will have negative effects on dynamic symmetry.

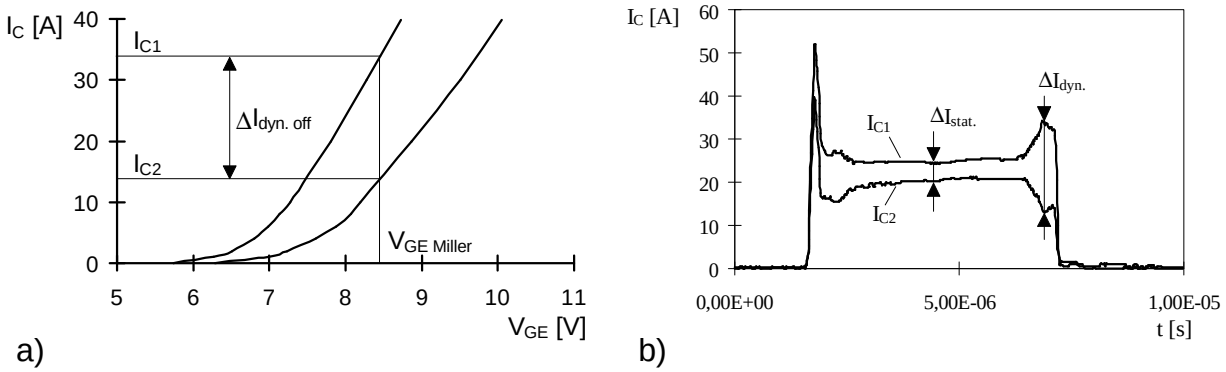


Figure 3.68 a) Transfer characteristics of two paralleled NPT-IGBTs
b) Dynamic current distribution during switching

Furthermore, Figure 3.68 makes it clear that, in addition to the transfer characteristics, the deviations of turn-on losses of IGBTs/ MOSFETs are basically determined by the turn-off behaviour of the free-wheeling diodes.

*Influence of loop inductance in the commutation circuit*

Following the explanations in chapter 3.4.1, turn-on and turn-off power dissipations of power semiconductors are determined by the commutation circuit inductance $L_K$ (loss reduction effect during turn-on, generation of switching overvoltage during turn-off).
Paralleling of switches is always equivalent to paralleling of commutation circuits. If commutation circuits are subject to different loop inductances, the switching speed of fast power semiconductors may be differently, which would cause dynamic asymmetries. Therefore, a strictly symmetrical layout of the commutation circuit should be realized.

*Influence of the driver output impedance (including gate series resistances)*

Impedance deviations of the driver circuits of paralleled transistors have to be minimized. Existing deviations will lead to non-simultaneous switching and will contribute to unbalanced distribution of switching losses.

*Influence of loop inductance of the driver circuit*

In combination with transistor input capacitances, the driver circuit loop inductance can generate heavy oscillations, which might even spread between paralleled transistors (see chapters 3.7.1.2 and 3.4.1).
To avoid such parasitic oscillations, principally any loop inductance in the driver circuit has to be minimized.

*Influence of the collector-/drain-current-carrying inductance of the driver circuit*

Fast alterations of the collector-/ drain-current during switching will induce voltages to the driver circuit inductance, where the main current is conducted; these voltages are counteractive to the gate charge or gate discharge, respectively (emitter-/ source negative feedback). The consequent deceleration of the switching process will increase switching losses.
With respect to paralleling of transistors, different values of these inductances might contribute to asymmetrical distribution of switching losses.

### *3.7.1.2 Module selection, driver circuit, layout*

The following recommendations with reference to module selection, driver and layout for paralleling of IGBTs and MOSFETs can be concluded from chapter 3.7.1.1.

**Module selection**

As for proper handling of dynamic symmetrization, NPT IGBTs are especially suitable for parallel connection because of the positive TC of their saturation voltage. Furthermore, they are outstanding for low tolerances and they are less temperature-dependent in their parameters.

**Driver circuit**

Figure 3.69 shows a proposal for the driver circuit layout for paralleling of IGBTs. The circuit is driven by one common driver unit.
In addition to the common gate series resistances $R_{Gon}$ and $R_{Goff}$ integrated in the driver, the resistances $R_{Gonx}$ and $R_{Goffx}$ damp parasitic oscillations between the gate-emitter/ gate-source circuits. Moreover, they reduce the negative effects of the different transfer characteristics.
$R_{Gonx}$ and $R_{Goffx}$ should be dimensioned with about 0.5 ...2 Ω.

The resistances $R_{Ex}$ will suppress balancing currents via auxiliary emitters. They should be dimensioned with about 0.5 Ω.

The resistances $R_{Cx}$ serve to determine the average actual $v_{CE}$-/$v_{DS}$-value in case overcurrent- and short circuit protection is based on $v_{CEsat}$-/$v_{DS}$ -evaluation.
They should be dimensioned with about 47 Ω.

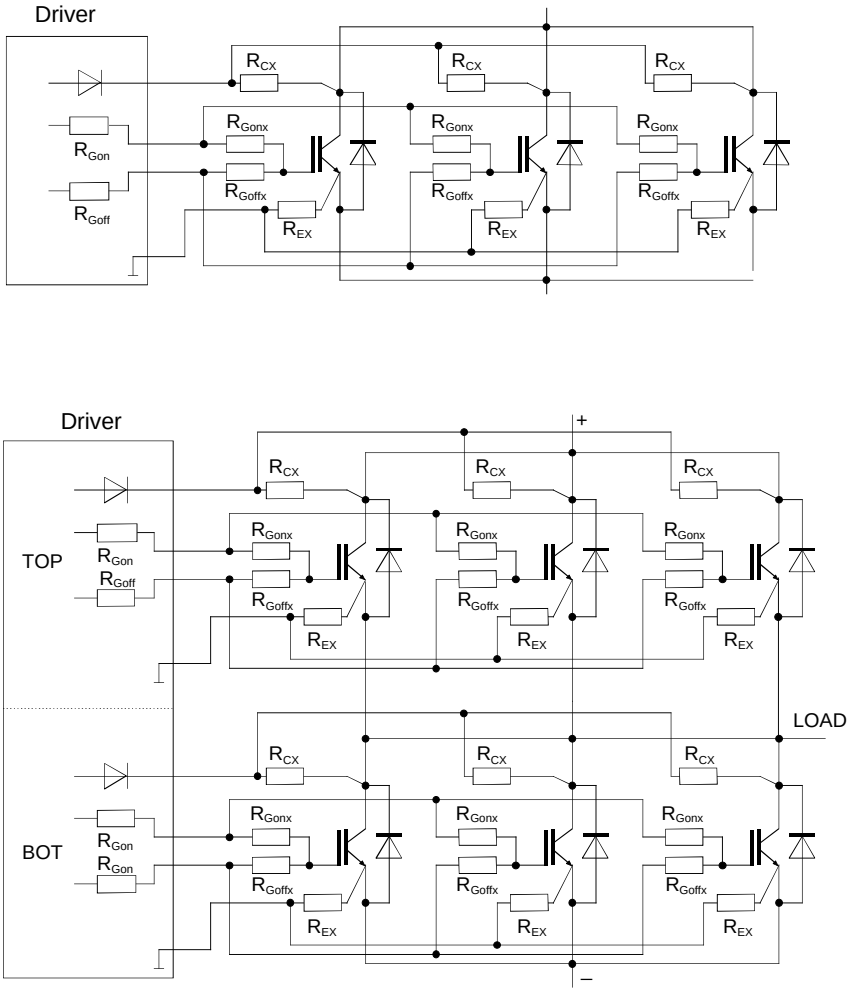


Figure 3.69 Parallel connection of single and dual IGBT modules

If paralleled transistors are to be driven by separate driver units, the driver units should feature identical signal propagation times and output parameters.

**Layout**

All power and driver circuits within the parallel circuit have to be laied out with minimum loop inductance and strictly symmetrical wiring.

Modules have to be mounted to a common heatsink close to each other to guarantee optimal thermal coupling (also because of symmetrization of inverse and free-wheeling diode).

Modern power modules are characterized by minimized internal inductances in the power and driver circuit of only some nH. However, since different module constructions will also show different inductance ratings, only modules of the same construction type should be connected in parallel.

**Derating**

Even if all conditions for optimal module selection, driver circuit and layout design have been fulfilled, an ideal static and dynamic symmetrization will not be achievable.
Therefore, derating has to be considered with respect to the total rated load current of the switches. From practical experiences in different applications a derating of about 15-20 % can be advised.