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CBiCMOS DRIVER FOR SWITCHING POWER MOSFET TRANSISTORS

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Abstract. Original full swing CBiCMOS driver of power MOS transistor is proposed in this paper. Complementary pair of bipolar transistors on circuit output provides low output resistance. Therefore, the driver can operate at frequencies of few MHz and that has been confirmed with simulation. Static transfer characteristic has a shape of the hysteresis curve. High threshold is a function of control voltage. The results are confirmed by SPICE simulation for standard $2\mu m$ technology process.

1. Introduction

MOS transistor increasingly replace bipolar transistors in power circuit [1,2]. Its significant advantage is very high static input resistance in order of magnitude from 10^8 to 10^9 ohms. Thereby, an input current is negligible. Furthermore, since the components are unipolar there is no congestion of minority charge carriers and therefore there is no a delay caused by it when switching off. For that reason the transient period is significantly shorter in comparison to a bipolar transistor. Operating frequency is thereby increased from several tenths of kHz, with bipolar transistors, to a several hundreds kHz with MOS transistors. Furthermore, MOS switches are thermally very stable because drain current has negative temperature coefficient and therefore a possibility of secondary breakthrough is minimized. The main disadvantage of MOS transistors is its higher resistance if being switched on and thereby, higher quasistatic dissipation. Besides, it is to be stressed that excitation current generator must have significant current abilities to be able to charge and discharge parasitic input capacitance of power MOS transistors in dynamic regime.

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In this paper original CBiCMOS driver with hysteresis transfer characteristic, capable of fast charging and discharging of parasite input capacitance of power MOS transistor, is proposed. The circuit has an ability of changing a threshold voltage by outside control voltage. That makes it suitable for application that engage optocouplers.

2. Power MOS switching characteristics

Parasitic interelectrode capacitances have a dominant influence on transient regime of MOS switching circuit. Between gate and source as well as between gate and drain there are parasitic capacitances C_{gs} and C_{gd} respectively, located in area where metal electrodes of drain and source overlap with difused source and drain $n+$ regions. Besides these, there is a capacitance C_{ds} of reverse biased drain–substrate $p-n$ junction. All these capacitances depend on drain–source voltage. Their average values are quite large, typically from hundreds pF to tens nF, because of large transistor area.

A detailed analysis switching characteristics of power MOS transistors with resistive load is shown in [5]. Only characteristic waveforms are shown here when gate excitation is pulsed (Fig.1.)

During delay times t_{dr} and t_{df}, power dissipation on transistor is low. Therefore these times are not critical. However, during t_f and t_r dissipation is significant (Fig.1.). Obviously, the slope of gate–source voltage change has a great influence on transient regime. For that reason excitation generator resistance R_g should be as small as possible. If voltage V_{GS} was changed as step function ($R_g = 0$), delay times (t_{df} and t_{dr}) and time t_f would be negligible. Rise time t_r would be determined by output capacitor $C_{OSS} = C_{ds} + C_{gd}$ discharge time. C_{OSS} is discharged by high drain current in saturated region. Finally, it is to be told that voltage characteristics, shown in Fig.1, illustrate transient regime only qualitatively because Miller effect and interelectrode capacitance dependence on voltage are not taken into account. Nonetheless, they ilustrate the transient process of power MOS transistors.

3. CMOS and optocoupler drivers

According to the conclusion from the previous section, to achieve optimal excitation of power MOS transistor it is necessary that:

- internal resistance of excitation generator is very small,
- excitation generator must have high current capacity to be able to charge and discharge the parasitic capacitance rapidly,
- excitation generator voltage V_g must be high enough to keep transistor fully switched–on (operating point in non saturated region).

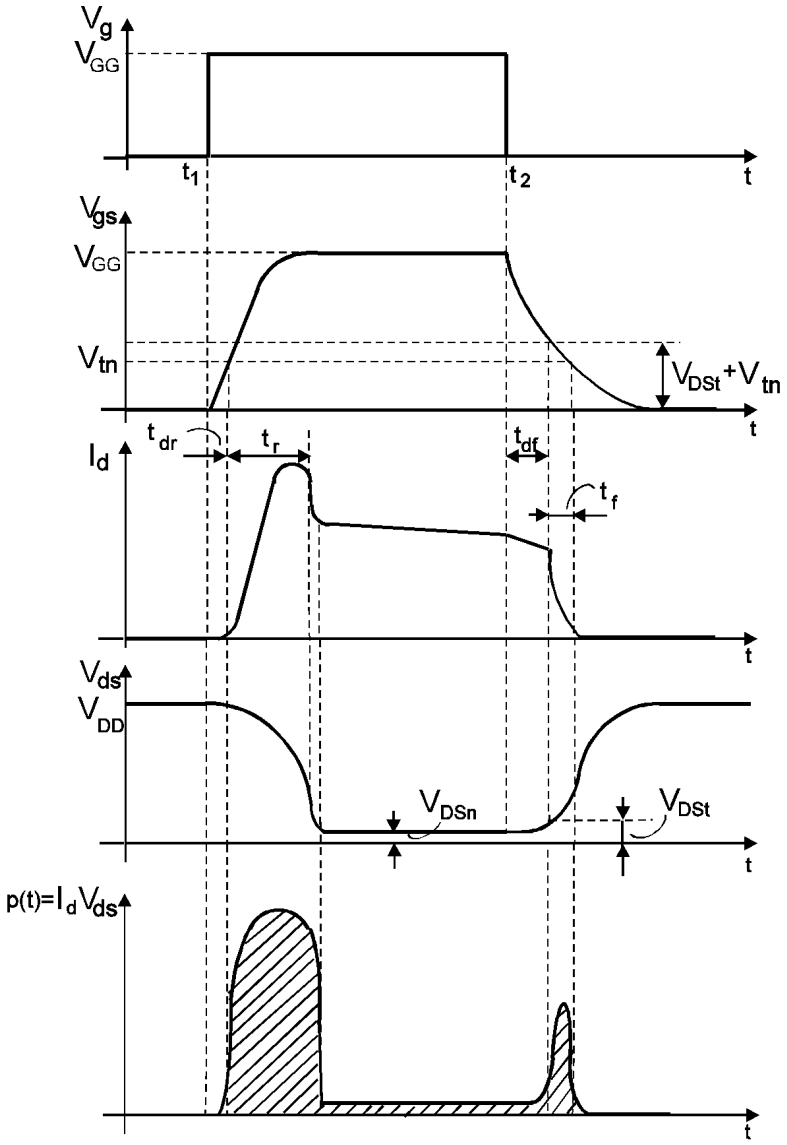

Figure 1. Power MOS switching waveforms.

All these conditions are easily satisfied and for that reason MOS excitation circuits are significantly simpler than their bipolar counterparts. Namely, in static conditions input resistance of MOS transistors is very high so it can be excited directly from output of CMOS logic circuits. It is recommended

for this circuit to have sink and source currents in order to have equal rise and fall times of gate–source voltage of power MOS transistor. Such the circuits, for example are: CD4007, CD4041, CD4069.

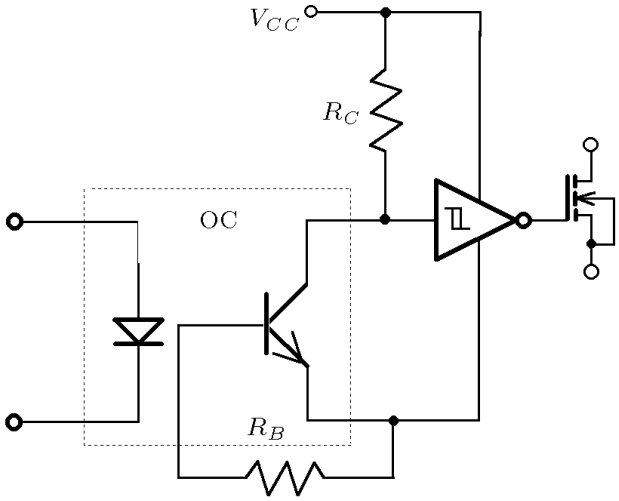

Figure 2. Optocoupler circuit.

In most cases the switching power supply should have input–to–output isolation. For that purpose the optocouplers are typically implemented (Fig.2). Schmitt trigger shapes the pulses from optocoupler output, filters out slow–changing noise and provides current high enough to charge and discharge of the parasitic capacitance of power MOS transistor. Resistor R_C defines operating regime of conducting optocoupler transistor, which can be saturated or in active mode. Since the optocoupler is relatively slow element, it is recommended for its transistor to be in active mode. It is the reason why threshold voltages of Schmitt trigger should be as high as possible (closer to supply voltage V_{CC}).

4. CBiCMOS Schmitt trigger driver

Schmitt trigger with complementary darlington bipolar and MOS transistors which satisfies aforementioned conditions is shown in Fig.3. It contains 3 blocks: input CMOS Schmitt trigger with transistors: $M_{n1}, M_{n2}, M_{p1}, M_{p2}$, M_{p0}, M_{p01}, output pair of complementary darlington bipolar transistors T_1, T_2, T_3, T_4 and CMOS pair of transistors M_{n3} and M_{p3} which provides full logical amplitude. Output bipolar transistors provide low output driver resistance and thereby fast charging and discharging of input capacitance of power MOS transistors. In static conditions M_{n3} or M_{p3} conduct and there-

fore output voltage $V_O = 0$ or $V_O = V_{DD}$. Voltage control of input circuit is achieved through the gate of M_{p01} transistor. Transistors M_{p0} and M_{p01} provide histeresys transfer characteristic of input circuit. When input voltage falls from V_{DD} to zero, before state of circuit change, transistor M_{p0} is switched off because $V_2 = V_{DD}$, therefore M_{p0} and M_{p01} does not influence the low threshold. For that reason, the low threshold is determined by voltage threshold of input pair of transistors M_{n1} and M_{p1}

$$V_{TL} = V_{tn} + \frac{V_{DD} - \mid V_{tp} \mid - V_{tm}}{1 + \sqrt{\frac{\mu_n}{\mu_p} \frac{\frac{W_{n1}}{L_{n1}}}{\frac{W_{p1}}{L_{p1}}}}} \tag{1}$$

where V_{tn} and V_{tp} are threshold voltages of MOS transistors, μ_n and μ_p are electron and hole mobility respectively and W and L are width and length of transistors channels.

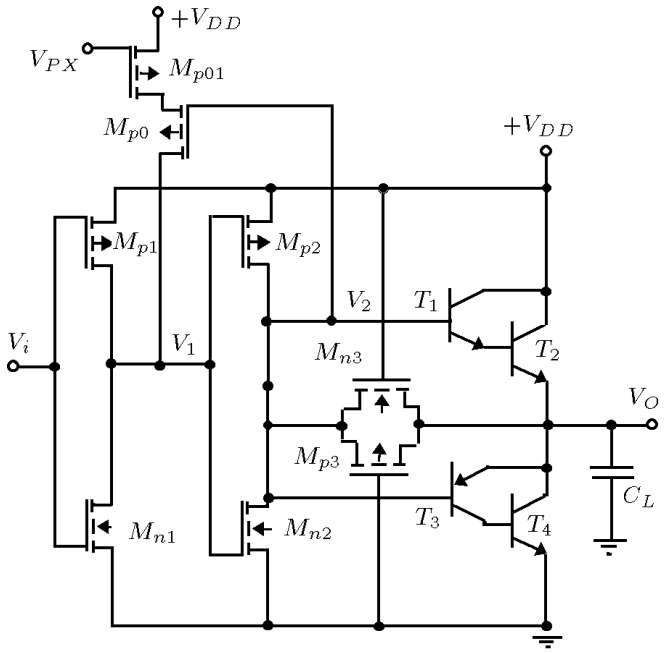

Figure 3. Proposed CBiCMOS Schmitt trigger driver.

When input voltage rise from 0 to V_{DD}, M_{p0} is on until output state change because $V_2 = 0$. Now M_{p0} and M_{p01} behave as a resistor which resistance is a function of the control voltage V_{PX}. Since the resistor is connected

in parallel to transistor M_{p1} it increases the total p–channel transistor current and that is equivalent to increase of transistor M_{p1} channel width W_{p1}. As control voltage V_{PX} decreases, the resistance is reduced and its current is higher and that is equivalent to an increase of channel width W_{p1}.

The analytic procedure described in [8] can shown that the high voltage V_{TH}, is approximately determined by:

$$V_{TH} = \frac{V_{DD}}{2} + \frac{W_{p0}}{2W_{p1}} \left[\left(\frac{V_{DD} - V_t}{V_{DD} - 2V_t} \right)^2 - \frac{1}{3} \right] (V_{DD} - 2V_t) \frac{V_{DD} + V_t - V_{PX}}{2V_{DD} + 2V_t - V_{PX}} \tag{2}$$

Elaborating the equation (2) we taken into account that: threshold voltage of all MOS transistors are equal ($V_{tn} = -V_{tp} = V_t$), constant β of transistors are $\beta_{p0} = \beta_{p01}$, $\beta_{n1} = \beta_{n2} = \beta_{p1} = \beta_{p2}$. According to (2), it means that high voltage threshold of Schmitt trigger would increase with decrease of V_{PX}. Control voltage can be changed in range: $0 \leq V_{PX} \leq V_{DD} + V_{tp}$. For this values of V_{PX} existence of hysteresis is guarantied. For $V_{PX} \geq V_{DD} + V_{tp}$, M_{p01} is permanently switched off so transfer characteristic is unambiguous with voltage threshold determined by (1).

5. SPICE simulation

SPICE simulation of static and dynamic characteristics of proposed driver is accomplished. Simulation is made for $2\mu m$ technology with $V_{DD} = 10V$. Fig.4. shows dependence of the low V_{TL}, and high voltage V_{TH}, on the control voltage V_{PX} for two widths values of channel W_{p1} of the transistors M_{p1}. The other transistors' channel widths are $W_{n1} = 2\mu m$, $W_{p01} = W_{p02} = 2\mu m$, $W_{n2} = 20\mu m$, $W_{p2} = 40\mu m$, $W_{n3} = 2\mu m$ and $W_{p3} = 4\mu m$. Other parameters used for simulation are given in Table 2.

For the purpose of estimation dynamic characteristic of the proposed driver the simulation provided rise and fall times of output voltage of the driver in depending on capacitive output loads. Fig.5. shows the dependence of two values of the channel widths W_{p2} and W_{n2} of the transistors M_{p2} and M_{n2}. With capacitive loads of $5nF$ and channel width W_{n2} and W_{p2} of the transistors M_{n2} and M_{p2} of $100\mu m$ and $200\mu m$, respectively, the rise and fall times are typical $20ns$, whilst with the capacitive loads of $1nF$ the rise and fall times are bellow $10ns$. The diagram in Fig.5. does not show rise and fall time delay of the output voltage, t_{dr} and t_{df}. Those times are $t_{dr} = 7ns$ and $t_{df} = 4ns$ and practicaly independent on capacitive loads.

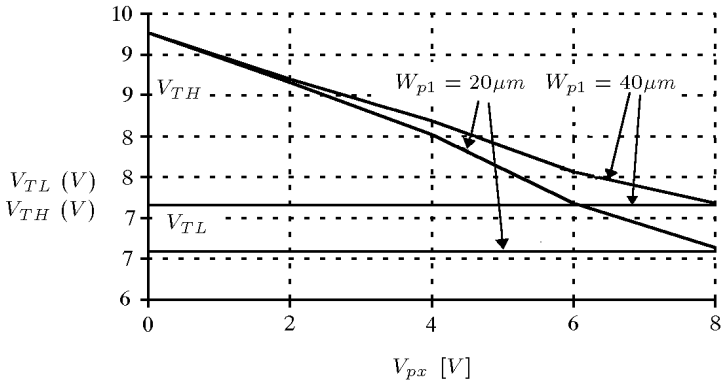

Figure 4. Dependance of high, V_{TH}, and low threshold voltage, V_{TL}, of Schmitt triger on control voltage V_{PX}.

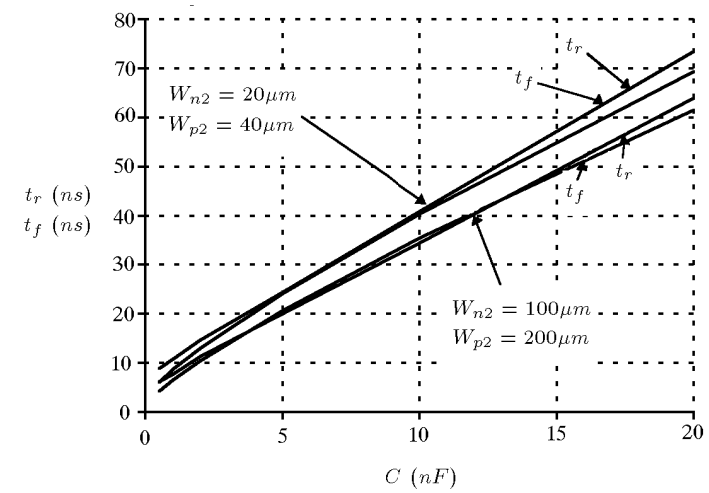

Figure 5. Dependance of rise and fall times of output voltage on capacitive loads.

Table 1. shows delay times, t_{dr} and t_{df}, fall and rise time of output voltage, t_r and t_f, of the proposed driver and some commercially available drivers. The Table 1. shows that fall and rise times are lower than with other drivers for different capacitive loads. Only in the case capacitive loads of

$30nF$, driver UC3710 has a bit shorter times t_r and t_f, but also considerably longer times t_{df} and t_{dr}. Short delay times with the proposed driver is a direct consecvence of its simple structure.

The proposed driver is used to excite power MOS transistor IRF150. The transistor load $R_P = 5\Omega$ is supplied by $V_{DD1} = 50V$, thereby maximum transistor current is $10A$. Parasite inductances of drain and source pins of transistor IRF150, which are $L_D = 5\mu H$ and $L_S = 12.5\mu H$ according to manufacturer specification, are taken into account. Frequency of input trigger pulses is 2 MHz and its amplitude is $10V$. SPICE parameters of transistor IRF150 is given in Table.2. With that excitation, gate voltage of IRF150 and its drain current results as it is shown in Fig.6. Drain current reaches its nominal value of $10A$, meaning that power MOS transistor is in non saturated region with low resistance R_{DSN} when switched on.

Table 1. Characteristic of some commercial drivers compared to the proposed driver.

IC	$C(nF)$	0	1	2.2	30
PROPOSED DRIVER	$t_r(ns)$	5.3	7.7	11.3	99
	$t_f(ns)$	2.5	6.5	11.2	86
	$t_{dr}(ns)$	7	7	7	7
	$t_{df}(ns)$	4	4	4	4
UC3705	$t_r(ns)$	20	40	60	
	$t_f(ns)$	25	45	50	
	$t_{dr}(ns)$	60	60	60	
	$t_{df}(ns)$	60	60	60	
UC3707	$t_r(ns)$	25	40	50	
	$t_f(ns)$	25	40	50	
	$t_{dr}(ns)$	40	50	60	
	$t_{df}(ns)$	30	40	50	
UC3710	$t_r(ns)$	20		25	85
	$t_f(ns)$	15		20	85
	$t_{dr}(ns)$	35		35	35
	$t_{df}(ns)$	35		35	35
SP600	$t_r(ns)$			25	
	$t_f(ns)$			25	
HIP4081	$t_r(ns)$		10		
	$t_f(ns)$		10		

The rise and fall times of the drain current of the transistor IRF150 (Fig.6b) are its own rise and fall times (acc. to manufacturer spec.) and are about $100ns$. By the selection of the faster transistor, IRF450, (specific

time rise and fall times of the drain current is about $50ns$) the frequency trigger pulses can be increased up to 4 MHz. Therefore, due to very short charge and discharge times of greater capacitive loads as well as shorter delay times, it is clear that given driver may be used at relatively high operating frequencies, and that makes it very suitable for excitation of switching elements in different resonant topologies.

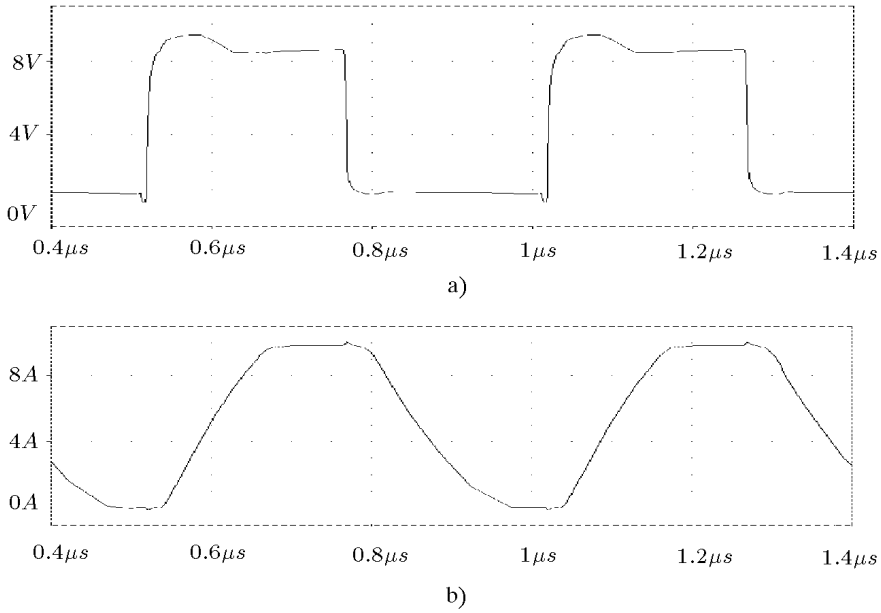

Figure 6. IRF150 (a) gate voltage charachteristic and (b) it's drain current given by SPICE simulation.

5.1 Application of the proposed driver with optocoupler

Due to input hysteric characteristics, the driver is very suitable for application with optocouplers. Simulation of proposed circuit is performed with optocoupler according to the circuit shown in Fig.7a. Optocoupler A4N25, which according to manufacturer specification has $3\mu s$ output voltage typical rise and fall time was used. For that reason, period of trigger generator VG was set on $20\mu s$ and pulse width is $5\mu s$. Resistor R_G in diode circuit is 100Ω, while $R_C = 200\Omega$. For this set of resistors, optocoupler transistors does not get saturated. Because of that, minimum voltage on its collector is about $4.5V$ (Fig.7b). Regardless, correct excitation of Schmitt trigger

can be obtained by setting Schmitt trigger threshold voltages above half of voltage supply level. Trigger voltage V_G and optocoupler output voltage on IRF150 transistor gate are shown in Fig.7b. Delay of rising and falling edge of transistor gate voltage is about $1\mu s$. This delay is less then manufacturer specification because transistor does not get saturated. But anyhow this delay is a limitation factor on use of this circuit at higher frequency what is possible only with faster optocoupler.

Table 2. SPICE model parameters.

Type	*npn*	*pnp*	Type	IRF150	*n*mos	*p*mos
IS	$14.34f$	$14.34f$	LEVEL	3	3	3
XTI	3	3	VTO	2.381	1	-1
EG	1.11	1.11	KP	20.53μ	69μ	34.5μ
VAF	74.03	74.03	GAMMA	0	0.417	0.933
BF	100	50	PHI	0.6	0.65	0.65
NE	1.30	1.30	JS		$1n$	$1n$
ISE	$14.34f$	$14.34f$	CJ		330μ	330μ
IKF	0.2847	0.2847	CJSW		$300p$	$300p$
XTB	1.5	1.5	MJSW		0.5	0.5
BR	6.092	6.092	CGS0	$9.027n$	$350p$	$350p$
NC	2	2	CGD0	$1.679n$	$350p$	$350p$
ISC	0	0	TOX	$100n$	$25n$	$25n$
IKR	0	0	XJ	0	$40n$	$20n$
RC	1	1	UO	600	500	250
CJC	$7.306p$	$7.306p$	NEFF		0.45	0.45
MJC	0.3416	0.3416	RD	$1.031m$		
VJC	0.75	0.75	RDS	$444.4k$		
FC	0.5	0.5	CBD	$3.229n$		
CJE	$22p$	$22p$	PB	0.8		
MJE	0.377	0.377	MJ	0.5		
VJE	0.75	0.75	FC	0.5		
TR	$46.91n$	$46.91n$				
TF	$411p$	$411p$				
ITF	0.6	0.6				
VTF	1.7	1.7				
XTF	3	3				
RB	10	10				

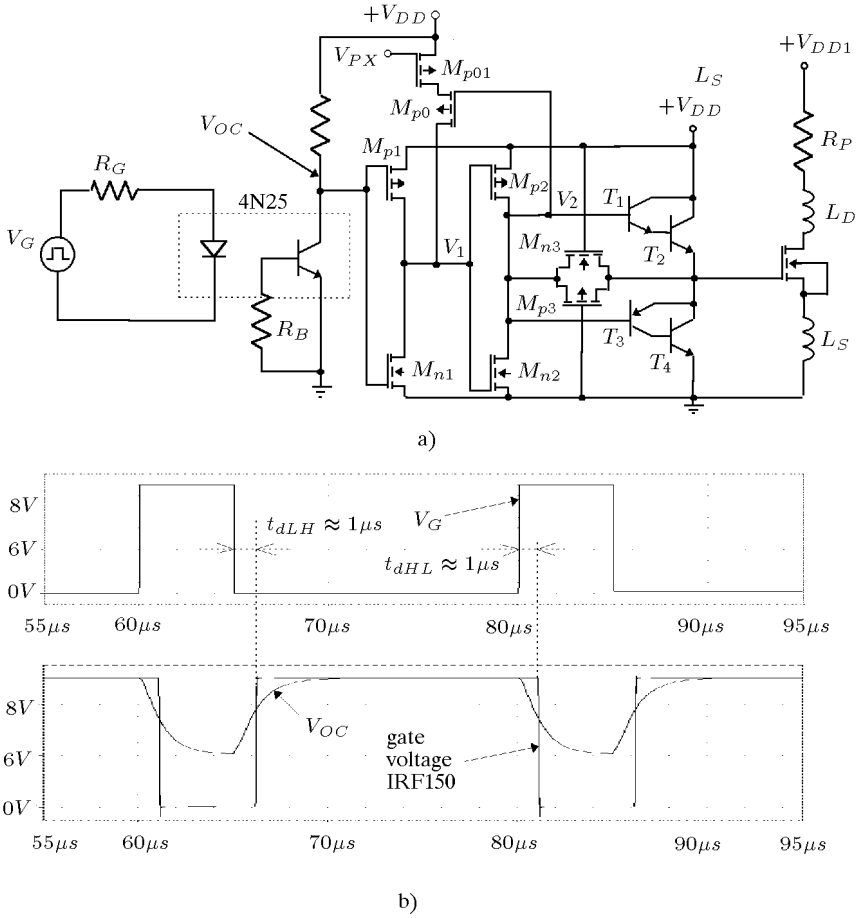

Figure 9. Schema of proposed CBiCMOS driver with optocoupler a) and results of simulation b).

6. Conclusion

Proposed CBiCMOS driver has high performances for driving power MOS transistors. This driver provides small rise and fall times of gate voltage of power MOS transistor. Those times are bellow $10ns$ for capacitive loads of $1nF$, i.e. $20ns$ with capacitive loads of $5nF$. Therefore, short output voltage rise and fall times, t_r and t_f, with very short delay times t_{dr} and t_{df} ($7ns$ and $4ns$ respectively), enable the excitationa power MOSFET transistors at frequencies of several MHz.

Because of hysteresis transfer characteristic, driver is especially suitable when excitation from optocoupler or generally excitation is slow changing. Hysteresis center can be regulated by control voltage V_{PX}, so that it may be adapted to any application.

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