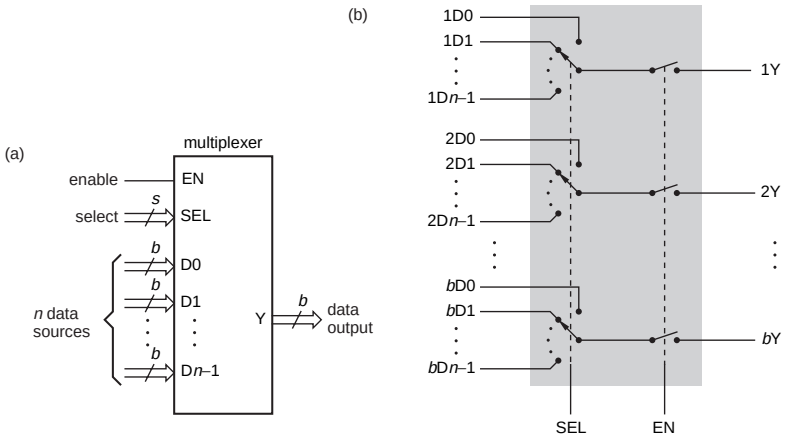
Multiplexers

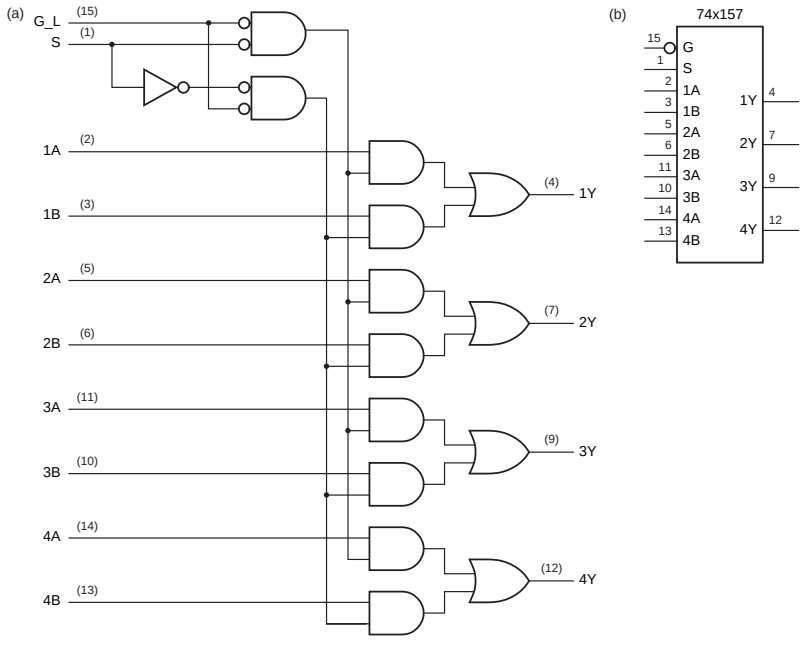
A multiplexer is a (one-directional) digital switch.



Parameters for n-input b-output mux:

- b outputs
- n inputs per output
- $\lceil \log_2 n \rceil$ select signals

74x157 quad 2-to-1 mux



Typical muxes in Xilinx library: `M2_1`, `M8_1E`

Multiplexer truth tables

This is same as truth table for `M2_1E` (except enable active level).

Inputs		Outputs			
G_L	S	1Y	2Y	3Y	4Y
1	x	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

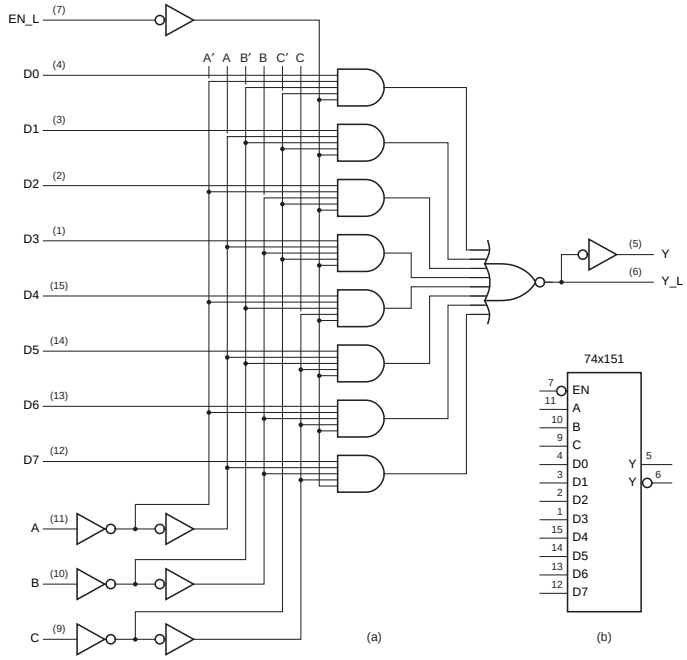
Table 5-35 Truth table for a 74x157 2-input, 4-bit multiplexer.

The 8-input 74x151 corresponds to `M8_1E` with an extra output.

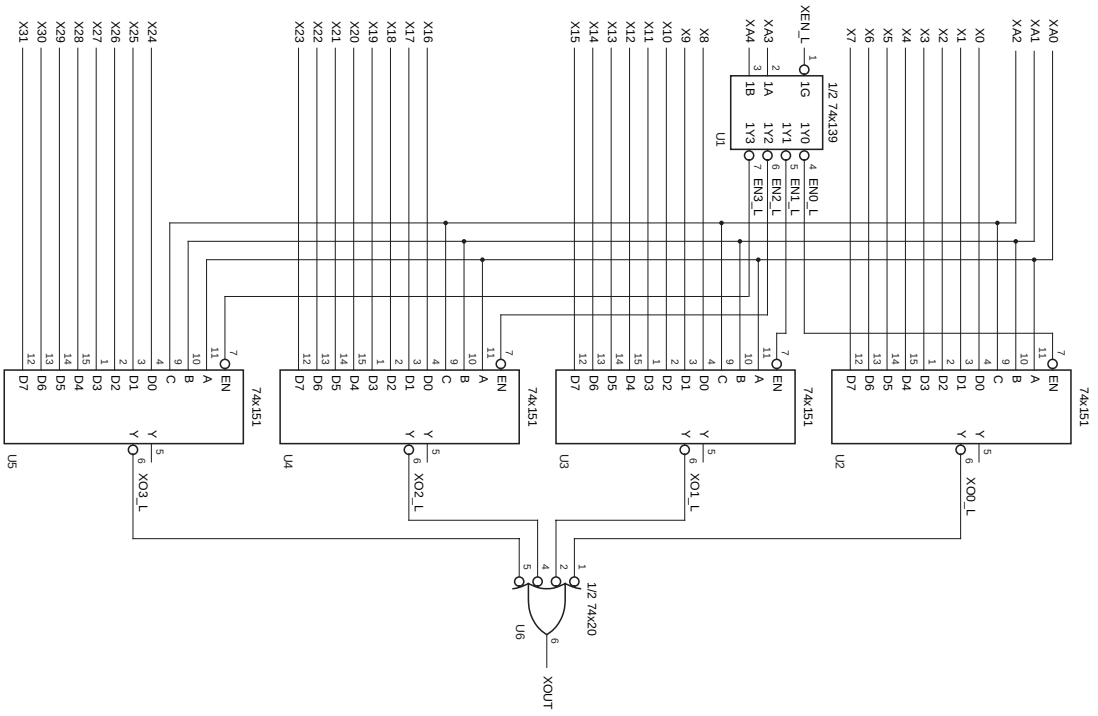
Table 5-34 Truth table for a 74x151 8-input, 1-bit multiplexer.

Inputs				Outputs	
EN_L	C	B	A	Y	Y_L
1	x	x	x	0	1
0	0	0	0	D0	D0′
0	0	0	1	D1	D1′
0	0	1	0	D2	D2′
0	0	1	1	D3	D3′
0	1	0	0	D4	D4′
0	1	0	1	D5	D5′
0	1	1	0	D6	D6′
0	1	1	1	D7	D7′

74x151 8-to-1 mux

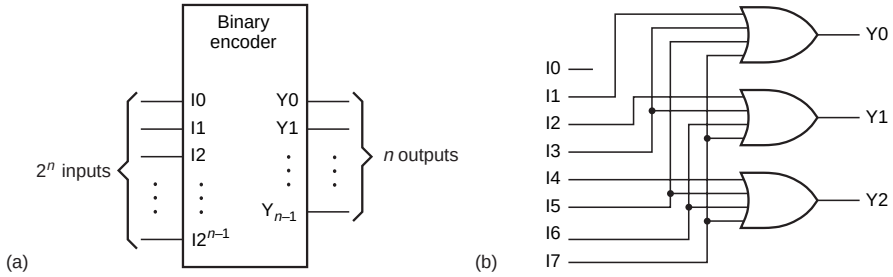


Expanding multiplexers



Encoders

Encoder converts input signals to more useful, usually more compact, representation. Most common encoder is 2^n-to-n binary encoder.



Equations for 8-to-3 encoder:

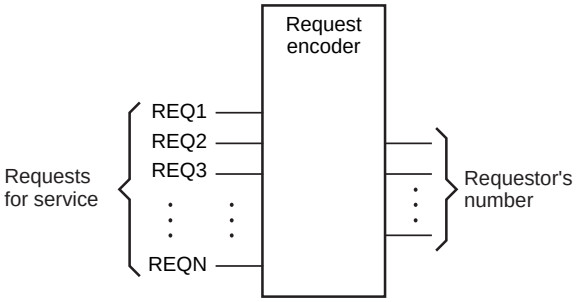
$$Y2 = I4 + I5 + I6 + I7$$

$$Y1 = I2 + I3 + I6 + I7$$

$$Y0 = I1 + I3 + I5 + I7$$

Encoder application

Typical application: produce the index of "the" signal that is active.

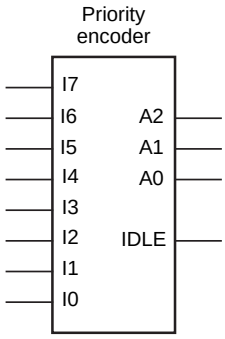


If more than one signal can be active, highest priority signal is selected.

A more advanced encoder might output indexes of highest two active signals.

An even more advanced encoder might remember previous requests and change priorities.

Priority encoder




```
H7 = I7
H6 = I6 * /I7
H5 = I5 * /I6 * /I7
H4 = I4 * /I5 * /I6 * /I7
H3 = I3 * /I4 * /I5 * /I6 * /I7
H2 = I2 * /I3 * /I4 * /I5 * /I6 * /I7
H1 = I1 * /I2 * /I3 * /I4 * /I5 * /I6 * /I7
```

```
A2 = H4 + H5 + H6 + H7
A1 = H2 + H3 + H6 + H7
A0 = H1 + H3 + H5 + H7
IDLE = /(I0 +...+ I7)
```

74x148 priority encoder

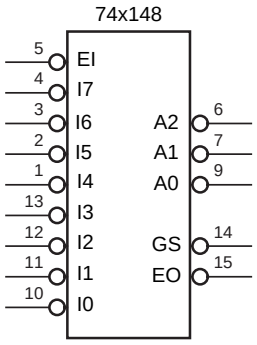
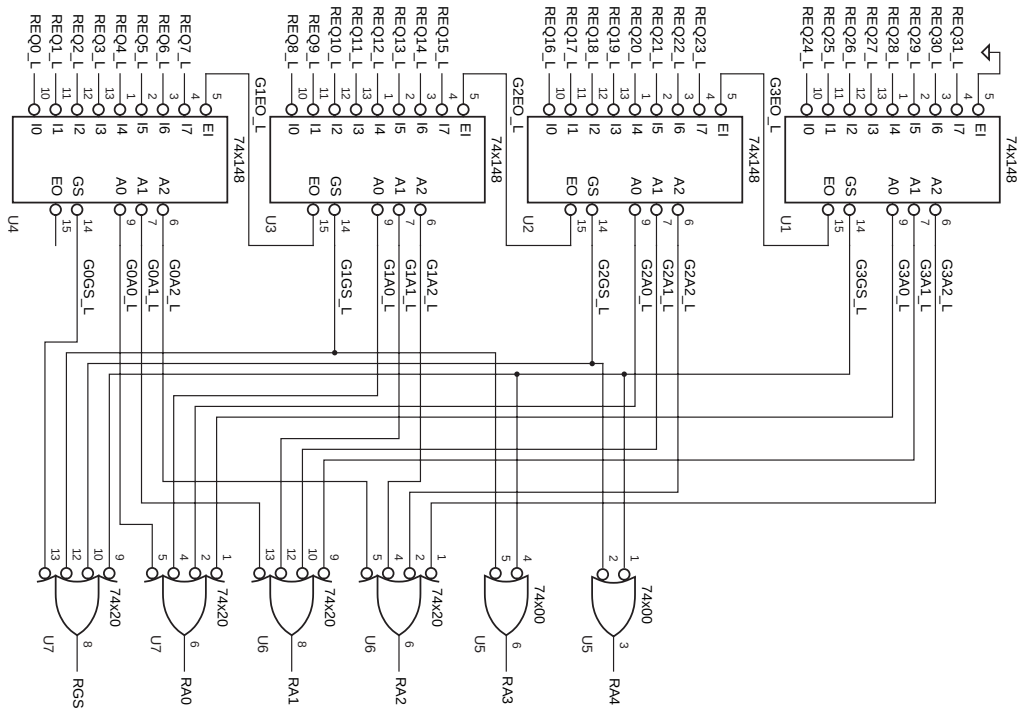


Table 5-23 Truth table for a 74x148 8-input priority encoder.

Inputs									*Outputs*				
EI_L	I0_L	I1_L	I2_L	I3_L	I4_L	I5_L	I6_L	I7_L	A2_L	A1_L	A0_L	GS_L	EO_L
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

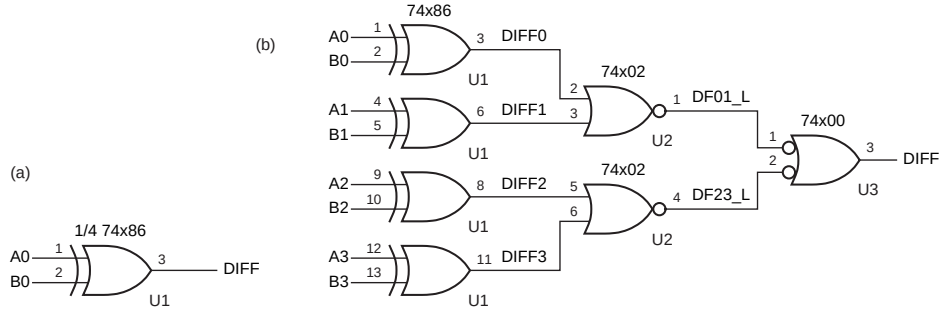
Cascaded priority encoders



Comparators

A one-bit comparator is the same as the XNOR or equivalence function (note that NXOR would be a better name than XNOR):

$$\mathrm{XNOR}(X, Y) = X \cdot Y + X' \cdot Y' = (X \cdot Y' + X' \cdot Y)'$$

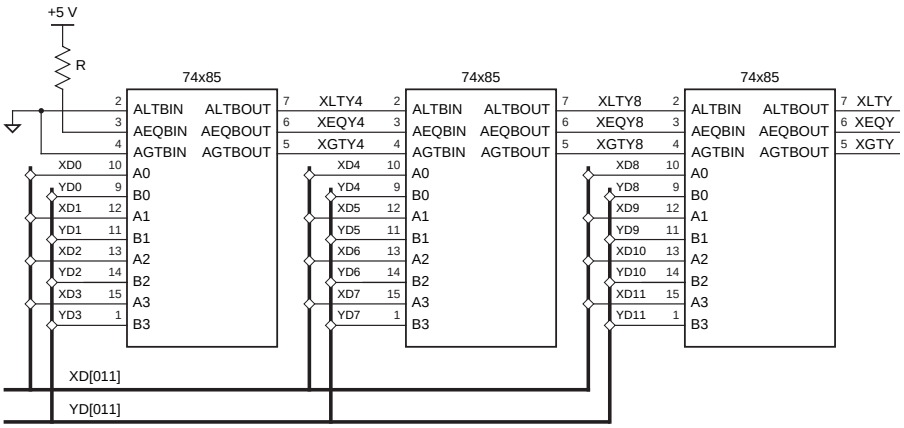


An n-bit comparator determines if two n-bit signal vectors are equal:

$$\mathrm{EQ}(X[1:n], Y[1:n]) = (X1 = Y1) \cdot (X2 = Y2) \cdot \cdots \cdot (Xn = Yn)$$

Magnitude comparators

Comparator components are designed to be cascadable.



Xilinx library includes, among others, `COMP8` (equality comparator) and `COMPM8` and `COMPMC8` (magnitude comparators).