# MULTI-LEVEL SWITCHMODE CLASS D AMPLIFIER

*By*

*TNG CHEE WAN*

Department of Electrical and Computing Engineering
The University of Queensland

Submitted for the Degree of
Bachelor of Engineering (Honours)
in the division of
Electrical and Electronic Engineering

OCTOBER 1998

8/35, The Esplanade,
St. Lucia, QLD(4067)
Tel. (07)33710742

October 14, 1998

The Dean
School of Engineering
University of Queensland
St. Lucia 4072

Dear sir,

In accordance with the requirements of the degree of Bachelor of Engineering (Honours) in the division of Electrical and Electronics Engineering, I present the following thesis entitled “Multi-Level Switchmode Class D Amplifier”. This work was performed under the supervision of Geoff Walker.

I declare that the work submitted in this thesis is my own and have not been previously submitted for a degree at the University of Queesdland or any other insituition.

Yours sincerely,

Tng Chee Wan.

# ACKNOWLEDGEMENT

I wish to thanks a number of people who contributed to this thesis and support me throughout the year. First, my heartfelt thanks to my supervisor, Geoff Walker, whose guidance and advises in formulating and clarifying in this thesis is greatly appreciated.

I wish also to thank my course-mate, Mark and Wong, for their continuous support and helps throughout the proceed of this thesis. Thanks also to Barbara for her encouragement and moral support given to me, not only throughout the year, but also for the friendship in which I always felt happy.

Finally thanks to my family, whose support make it possible for the completion of my thesis and more importantly my undergrad degree.

# Abstract

The theoretical power efficiency of a Class D amplifier is 100% and its theoretical distortion (Harmonic and Intermodulation Distortion) are both zero. In a practical Class D amplifier have a power efficiency in the range of 85% to 95% and distortion level of 1-5%. The Class D amplifier is mostly used in a low frequency(Hz) application as its loss is significantly low in that range.

In this thesis, a high frequency multilevel Class D amplifier is constructed and its output is analysis. The construction of each stage of the amplifier is discussed and the different topology of the PWM techniques and the effect of different design of the output low pass filter are also discussed. Lastly, the efficiency of the implemented amplifier is recorded.

# CONTENT

# LIST OF FIGURES

# LIST OF TABLES

# CHAPTER ONE

# INTRODUCTION

# 1.1 CLASSIC POWER AMPLIFIERS

Many electronic systems are designed to process electrical signals from a transducer. However, the signals provided by transducers are said to be 'weak', i.e. they are in the microvolt (μV) and millivolt (mV) range and posses little energy. These signals are too small for reliable processing. If their magnitude is made larger, the processing will be much easier. Hence, the need for an amplifier arises.

The 3 type of common amplifiers : Class A, Class B and Class AB classified according to the transistor conduction angle θ (*Fig 1.1*). The conduction angle for Class A is 360° (*Fig 1.1b*). The transistor in a Class A amplifier conducts for the entire cycle of the input signal. The conduction angle for Class B is 180° (*Fig 1.1d*). The transistor in a Class B amplifier only conducts for half of the input cycle. Class AB is an intermediate class between Class A and Class B. The conduction angle of a Class AB is between Class A and Class B. However, it must be pointed out that the angle is only slightly greater than 180°but much less than 360° (*Fig 1.1c*). As a result, the transistor conducts for an interval slightly more than half a cycle.

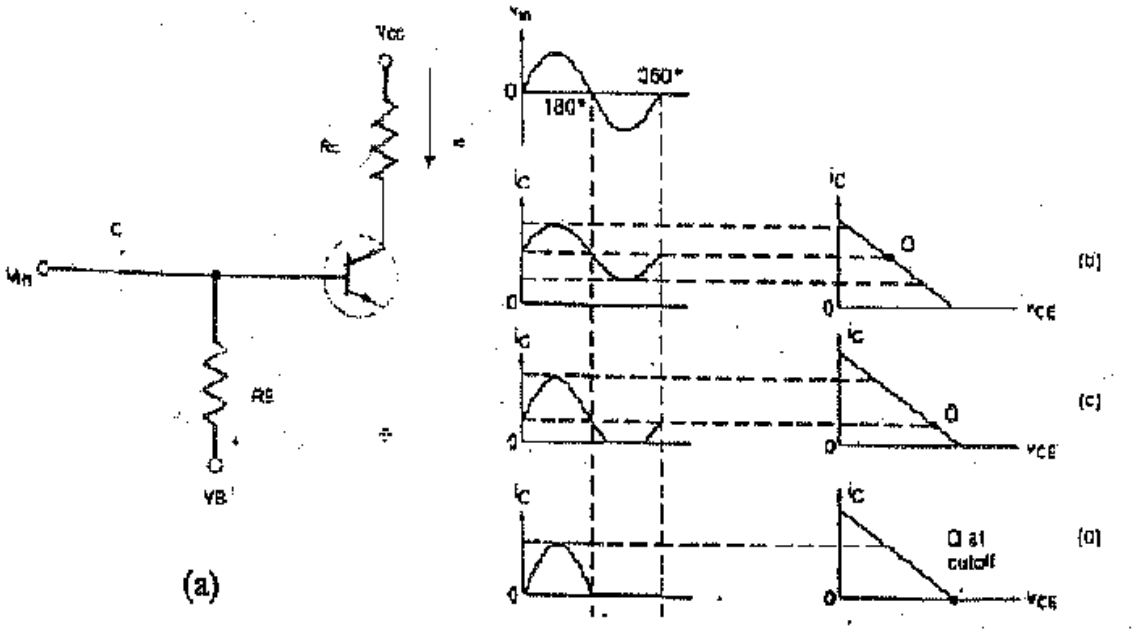



*Fig 1.1 Conduction angle of different classes of amplifier*

Each of the 3 classes of amplifiers has its advantages and disadvantages, as summarised in Table 1.1.

| Class | Advantages | Disadvantages |
|---|---|---|
| A | Low distortion | Low efficiency (25% Max.) |
| B | High efficiency (75% Max.) | High crossover distortion |
| AB | Reduce Class B crossover Distortion | Reduce Class B efficiency |

*Table 1.1 Advantages and Disadvantages of 3 types of common amplifiers*

In the 1990s, many audio products use power supply voltage (below 3V). For instance, Walkman (3 volts), Discman (3 volts) and multimedia (5volts). The lower power supply voltage demands the amplifier to have a very high efficiency (>90%). From *Table 1.1*, it can be seen that none of the 3 classes of classic amplifiers can meet the requirement.

In 1940s, the concept of Class D amplifier was introduced to circumvent the disadvantages of Class A, Class B and Class AB amplifiers. Theoretically, a Class D amplifier has a very high efficiency (100%), very low total harmonic distortion (0%) and intermodulation distortion (0%) [1]. The actual implementation of Class D amplifier was impractical until MOSFETs became available in 1980s.

With the current technology, a Class D amplifier can achieve approximately 94% power efficiency, Total Harmonic Distortion-plus-noise performance ranging from less than 1 to 2.8% in an evaluation circuit [2].

## 1.2 OVERVIEW OF A CLASS D AMPLIFIER

In order to appreciate the advantages of a Class D amplifier, its operation needs to be understood. The operation procedure at the output stage of a typical Class D amplifier is described in this section. Fig 1.2 depicts the block diagram and schematics at the output stage of a typical Class D amplifier respectively.

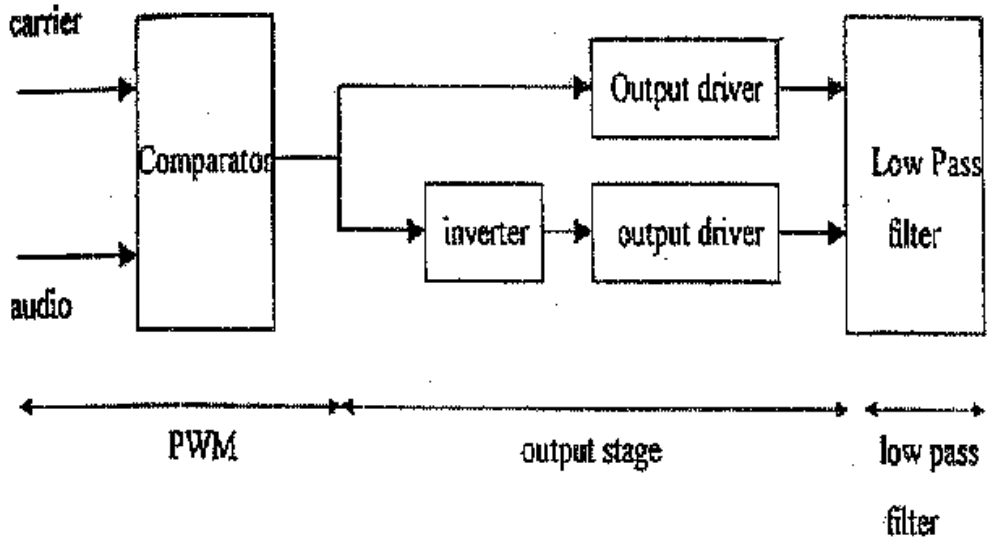



*Fig 1.2 Block diagram of a Class D amplifier*

A Class D amplifier comprises of 3 main function blocks, namely the pulse width modulator (PMW), the output stage and the low pass filter (*Fig 1.2*) [1].

The operation of a Class D amplifier begins with the PWM block. A comparison between an audio signal and the carrier (a triangular wave generated internally) is done via a comparator. The resultant waveform at the output of the comparator is a train of pulse-width modulated pulses, where the width of these pulses are proportional to the instantaneous amplitude of the audio signal.

The PWM signal is fed to the input of the Class D amplifier's output stage. The objective of this stage is to enable the logic level of the PWM pulses to gain adequate driving capability. This is accomplished by making use of the MOSFETs. As MOSFETs have very low turn-on and very high turn-off resistance, this result in very low power dissipation and thus achieving high efficiency.

After passing through the output drivers, the PWM pulses will go through a low pass filter. By designing the low pass filter with an appropriate cut-off frequency, the desired audio signal can be restored at the output.

In general, the Class D amplifier has excellent linearity and noise immunity. In addition, it is free from crossover distortion, which is encountered in other amplifier. Furthermore, being compatible with the digital-oriented MOS fabrication process, the amplifier can be made to be very compact [3].

## 1.3 OBJECTIVE

The overall objective of this thesis is to study the implementation of Class D amplifier operating in high audio frequency. The waveform of each stage of hardware implementation and the different levels of switch-mode Class D amplifier is being investigated here. The results of this thesis should enable circuit designer to better understand the operation of the switching characteristic and the output design of a Class D switching amplifier.

## 1.4 ORGANISATION OF THESIS

This project consists of 2 parts – Theory discussion and Practical simulation.

Chapter 1 gives a summary back ground of this thesis project and describe the overview of a Class D amplifier, specifies the objective of this project, and the organisation of this report. Chapter 2 gives a summary of the theories related to a Class D amplifier incorporate with the literature review on Class D amplifier. Chapter 3 present the practical results obtain from the hardware implementation. In chapter 4, a discussion of the result obtain in chapter 4 is being discussed in detail. Finally, chapter 5 concludes the project.

# CHAPTER TWO

# THEORY AND LITERATURE REVIEW

In this chapter, we are going to look at the theory behind the working principle of a single and multi-level PWM, its losses and the different type of modulation technique. We will also discuss the operation of a Class D amplifier its efficiency and its distortion.

## 2.1 PULSE-WIDTH-MODULATOR (PWM)

The basic principle of a Class D amplifier starts off with the PWM. There are various type of PWM technique. The width of the PWM can be varied to control the output voltage. There are various ways of generating a PWM switching but can be categories into the following 3 area namely:

- Hysteresis control
- Precalculated PWM techniques
- Carrier based PWM

Only the last category will be discuss here as only this will be applied.

### 2.1.1 CARRIER BASE PWM

There are many variation of carrier base PWM but 2 types of carrier base pulse-width modulation, the natural sampling and the uniform sampling method, will be mentioned. In the natural PWM, the switching of the pulse-width are generated at the intersection of the carrier and the input signal. The pulse of he PWM can be varied by using the sinusoidal PWM technique as shown in *Fig 2.1* [4]. The Pulse signal are generated by comparing a sinosoidal signal and a triangular carrier wave of frequency, fc. The frequency of the sine wave determine the output frequency and the number of pulses per half cycle is determine by the carrier frequency which is the triangular wave. The purpose of the PWM is to make sure that the average of the output pulse is proportional to the value of the input signal. This eventually means that the transfer function is linear and distortionless.

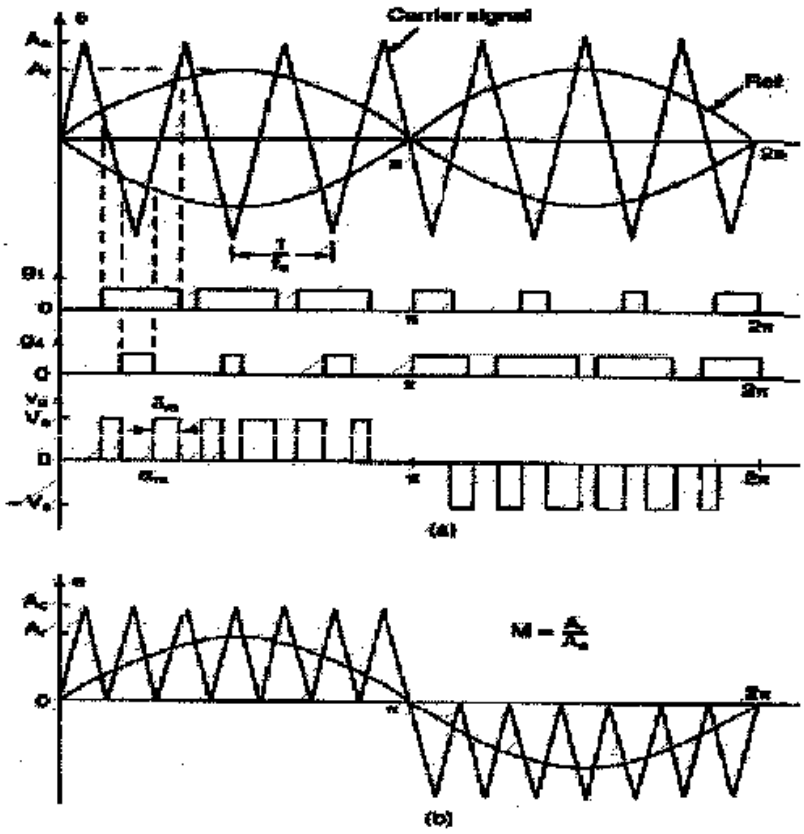



*Fig 2.1 Sinusoidal Pulse-Width-Modulation*

In the uniform sampled PWM, the input signal is regularly sampled and held constant at the beginning of each switch cycle before they are being compared with the triangular carrier. The spectra of the uniform and natural PWM is determine using the same techniques. Since only the natural sampling method will be implemented in the hardware design, we would discuss briefly the hardware implementation next and look at it in more detail in the next chapter.

The natural PWM modulator is can be implemented in the analogue hardware. The triangular carrier can be generated by integrating a square wave generate by a clock, and then pass the carrier signal together with the input signal through a comparator. The

generated square waves will have a representation of the reference signal. This reference signal can be retrieve through filtering out the carrier (triangular wave) signal by using a low pass filter (LPF) which we will discussed in the later part of this report. This type of modulated signal is of single level. By generating a number of synchronised, phase shifted carrier signals, we are creating a multi-level pulse-width modulated signal and subsequently a multi-level switch-mode power supply.

### 2.1.2 MATHEMATICAL ANALYSIS ON THE PULSE WIDTH MODULATION

In order to study the factors that can affect the harmonic distortion levels in a Class D amplifier, a mathematical analysis on PWM waveform essential.

PWM is a modulation of a pulse carrier in which the value of each instantaneous sample of a continuously varying modulating wave is caused to produce a pulse of a proportional duration. The PWM pulses may be obtained by two sampling methods, namely the natural and uniform sampling methods. The different between the natural sampling process is that in natural sampling, the point at which the signal is sampled coincides exactly with the pulse edges. On the other hand, in uniform sampling, each pulse width is proportional to the instantaneous value of a given sample. In addition, for a given signal, the two sampling processes actually produce pulse trains with different spectral characteristic [3]. For instance, the uniform sampling spectra of a sinusoidal signal would contain harmonics of the signal as well as the combination tones centred at about the multiples of its carrier. However, in the case of natural sampling, it does not contain any harmonic components, only the combination tomes with higher magnitude for both single and double sided, natural sampling.

In single sided trailing edge natural sampling, the duty-cycle of the PWM pulse is proportional to the magnitude of the message wave at the trailing edge of the pulse. As for pulses with both edges modulated, they are actually a combination of the leading and

trailing edges modulated pulses. When the time scale is reversed, pulses with the leading edges modulated will become pulses with trailing edges modulated [5]. Thus

$$F_2(t) = F_1(-t)$$

Where $F_2(t)$ is the series representing a train of width modulated pulses with trailing edges modulating and natural sampling and

$$F_1(t) = k + \frac{M}{2}\cos\omega_s t + \sum_{m=1}^{\infty}\frac{\sin m\omega_c t}{m\pi} - \sum_{m=1}^{\infty}\frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k)$$
$$-\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin(m\omega_c t + n\omega_s t - 2m\pi k - \frac{n\pi}{2}) \qquad (2\text{-}1)$$

Where

*$W_c$ : carrier frequency in rad/s*

*$W_s$ : signal frequency (modulating frequency) in rad/s*

*M : modulated index ($0 \le M \le 1$)*

*$J_n$ : Bessel function of the first kind and the nth order*

*K : zero-input duty circle of the PWM signal*

$F_1(t)$ is the series for the width-modulated pulses with the trailing edges modulated by natural sampling of a sinusoidal modulating wave. Therefore,

$$V_{out} = F_1(t) + F_2(t) = F_1(t) + F_1(-t) \qquad (2\text{-}2)$$

Equation 2-1 consists of various terms, including a DC term K, terms proportional to the signal frequency, harmonics of the carrier as well as an inter-modulation term. It is assumed that the pulses of the PWM waveform are either a '1' or '0', which is the ideal case. Except for the input signal term and DC components shall be filtered off by a low pass filter [1].

## 2.2 SWITCHMODE POWER SUPPLY

The main reason of generating a pulse-width modulated signal is to create a switching power supplies and regulator. The switching power supply have come into widespread use in the last decade because of their much higher efficiency, smaller size and weight, and relatively low cost. They are displacing conventional linear power supplies, even at low power.

However, even though high conversion efficiency has been achieved, present switching converter designs possess several undesirable characteristics. Rapid switching of the input or output current can cause severe Electromagnetic Interference (EMI) problems, requiring the addition of appropriate filters that increase both complexity and cost of the circuit. In switchmode power amplifier design, additional problems are imposed by the requirements for dual (bipolar) power supplies, high switching frequencies and complex feedback circuitry.

Switching power supplies are based on the principle that by alternately switching the transistor completely on (in saturation) and off (completely off), its power dissipation can be held to a minimum due to the fact that it is not operating in the linear region (other tan for the unavoidable of transition from conducting to non-conducting state) which will incur an undesirable efficiency loss and power switching loss*(Fig 2.2)* [6].

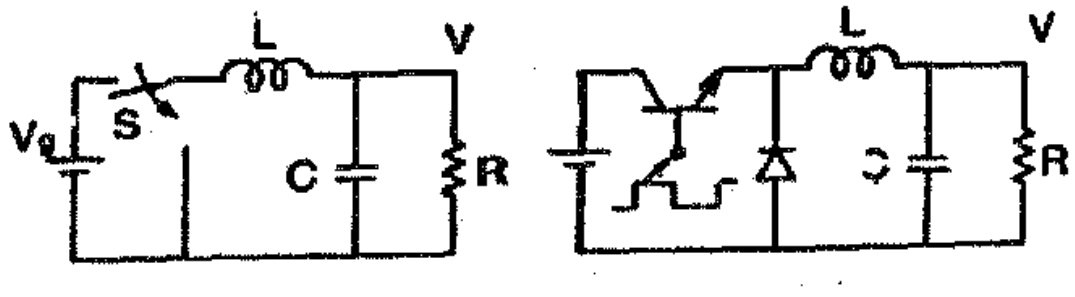



*Fig 2.2 The implementation of the switch using a bipolar transistor*

As the output of the switch-mode power supply is connected to the power output stage, it must be able to satisfy the requirement of the power stage. The power stage of a switching amplifier is that it must be capable of producing an output of either polarity. To apply this dual-polarity power stage in a switching power amplifier, it is necessary to control the duty cycle so that the output voltage varies in proportion to the input signal. When the input signal is positive, duty-cycle (D) greater than 0.5 is generated, producing positive output while for negative input, D is less than 0.5 and negative output is produce. Since the inductor current determines the output voltage, the hardware implementation of the switch must permit bi-directional current flow as shown in *Fig2.3* [6].

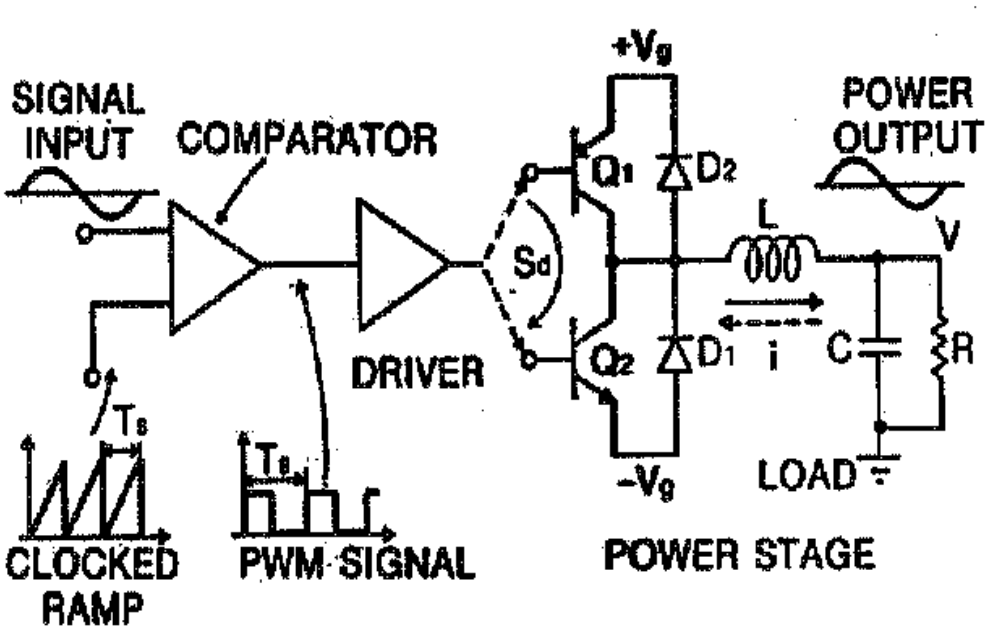



*Fig. 2.3 An open loop switching power amplifier (Buck type)*

This can be readily accomplished by the two transistors with the two diodes. To apply this dual-power stage in a switching power amplifier, it is necessary to control the duty cycle so that the output voltage varies in proportion to the input signal. The linear gain of the buck power stage facilitates this function, and is incorporated into the open–loop amplifier configuration shown in *Fig 2.3.* The design is the same as that of a dc-to-dc

converter operation at constant switching frequency f = 1/Ts, with the only difference that a time varying (sinusoidal, for example) input signal is used at the comparator input, instead of a dc reference voltage.

## 2.3 THE POWER OUTPUT STAGE

The output stage of a Class D amplifier can be describe using the following diagram.

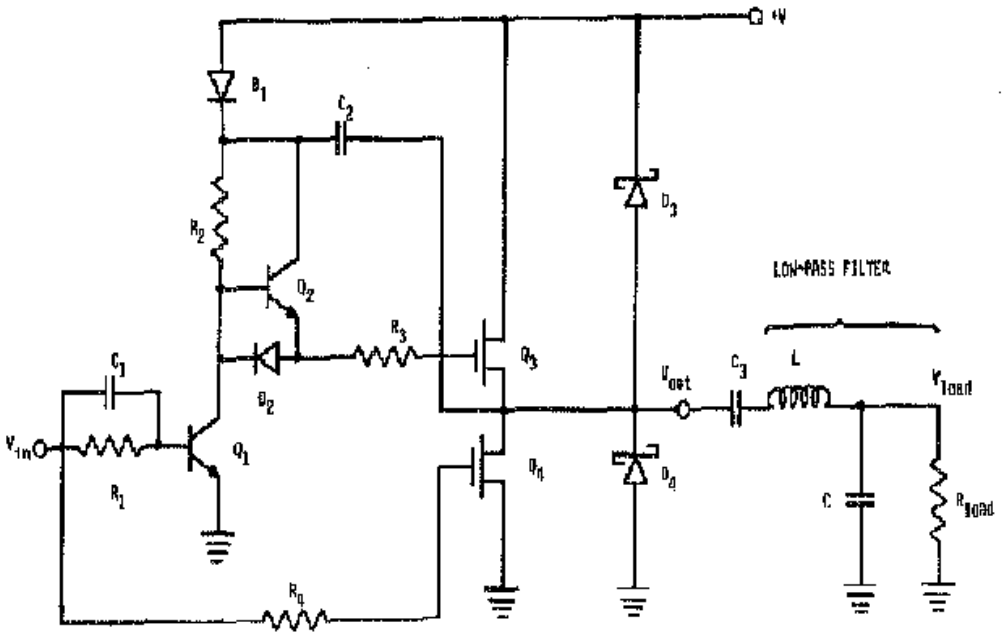



*Fig 2.4 AC-coupled Output stage bipolar driver*

The Class D output stage of the above circuit is operated from a single power supply and is coupled to the load via capacitor C3. A PWM input signal is applied to the gate of the output transistor Q4 and base of driver transistor Q1. The input signal is inverted by Q1 yielding a complimentary drive signal at the gate of output transistor Q3. During operation, a high level input to the stage cause Q4 to conduct, forcing the output to approach ground potential. The corresponding low level signal developed at the gate of

Q3 forces the device into ‘OFF’ state. Conversely, a low level input to the stage produces a high-level signal at the gate of Q3, forcing device to enter the ‘ON’ state. If we assume that Q3 ‘ON’ state resistance is significantly less than the load, the input voltage approaches the positive supply level [7].

The output stage is actually consists of the half bridge configuration. In the half bridge configuration, the controller, the power stage shared the same ground, which simplified the implementation of the controller. However, in reality, the half bridge converter is not suitable for amplifying signal with DC or low frequency. Thus we have to use a full bridge configuration (*Fig 2.5)* for low frequency or DC [8].

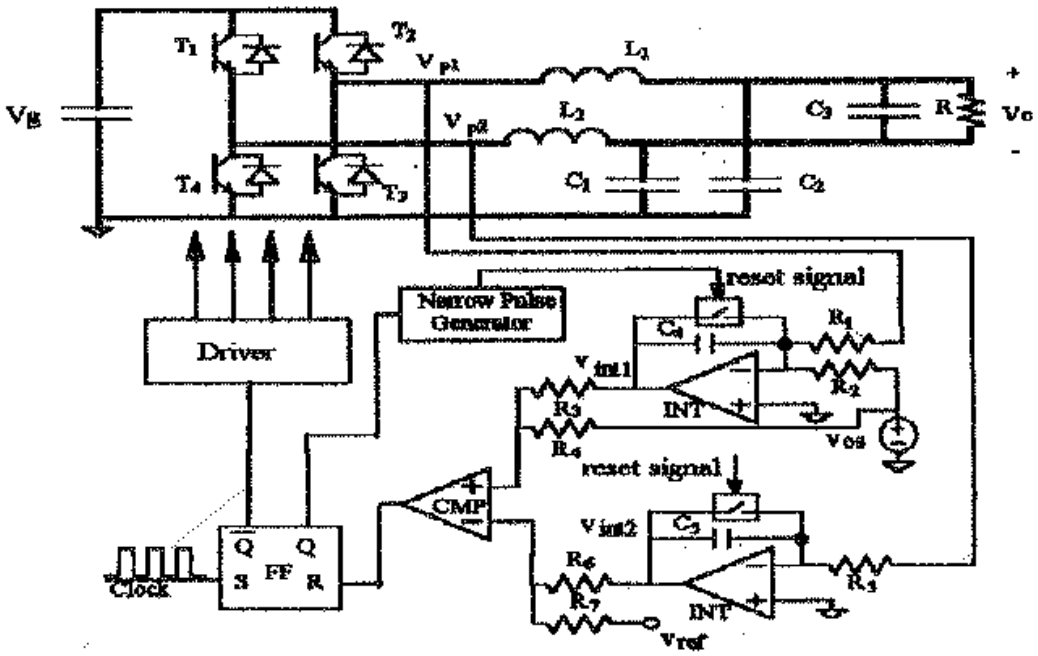



*Fig 2.5 Conception circuit of a full bridge configuration.*

The full bridge converter and its low pass filter network are connected symmetrically to eliminate the switching frequency common mode signal at the output Vo. The output of the bridge Vp (=Vp1-Vp2) is a floating switch variable. In practice, Vp is a large pulse

signal. It will be distorted by the delay and the slew rate limitation of the operational amplifier in the conversion process and therefore the control accuracy is affected [8]. In order to propose the performance of the amplifier, a numerous way can be considered. A feedback can be added as it serves to stabilised the closed loop amplifier gain against parameter variation in the system components and reduce distortion due to the non-linearity in the PWM. A much better LPF can be constructed to reduce the distortion level of the output. The third method that can be considered is to construct a multi-level switch-mode power supply, in this case three-level switch-mode supply.

The principle of the three level switch mode is to generate a 2 triangular carrier, which are 180° out of phase with each other. The two independent carrier signals are then pass through 2 different comparator to be compared with the input signal. Each of them will them produce their own PWM signal which is again out of phase with each other. The purpose of creating the two signals 180° out of phase with each other is so that they can capable of minimising the switching loss by cancellation out each other distortion after we pass through the LPF. By performing the above method, a two level switch-mode are produce. In order to obtain the three levels. We need to combine the output of the two different PWM signals and obtain the third level.

## 2.4 POWER EFFICIENCY OF A CLASS D AMPLIFIER

As mention that one of the advantage of a Class D amplifier is its relatively high efficiency compared to the amplifiers of other classes. In the other amplifier, their low efficiency is due to the higher power dissipation at the output stage. For Class D amplifier, this problem has been minimised through its digitised circuit design at the output.

The three main causes of power dissipation at the output stage of the Class D amplifier are the charging and discharging of the parasitic capacitors, short circuit current dissipation during the transitions of the input signal as well as the resistance of the output transistors [1]. A typical bridge-output Class D amplifier id depicted as in *Fig 2.6.*

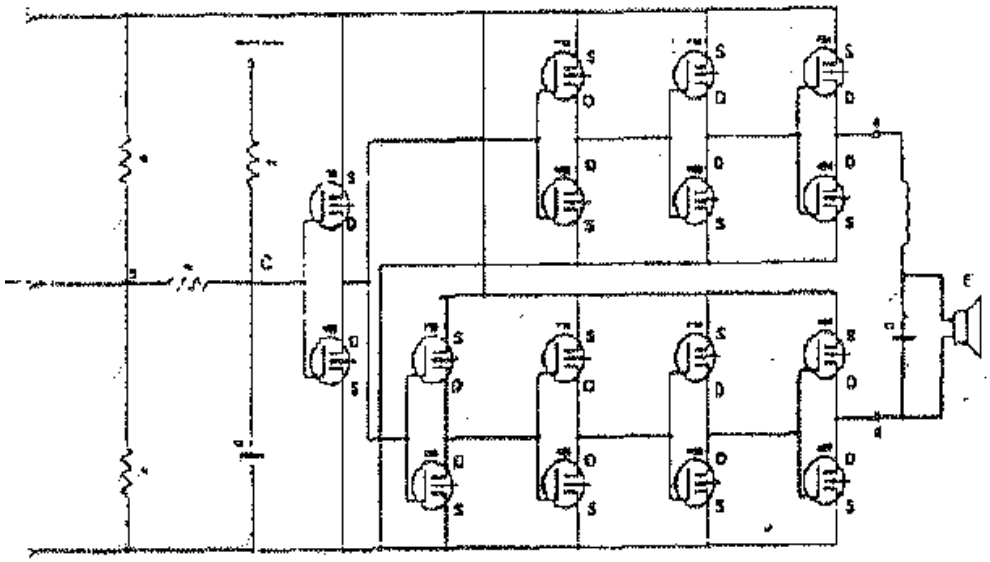


*Fig 2.6 A typical bridge-output Class D amplifier*

In the ideal case of an output stage, the parasitic capacitance as well as its rise and fall time will be zero. In addition, the ideal transistor should have zero on-resistance and indefinite off-resistance. The equivalent circuit of the ideal output stage is redrawn as in *Fig 2.7* and *Fig 2.8*, where current through the load can be expressed as

$I_o(t) = MI_{os}sin(2\pi f_s t)$ where M is the modulation index and $I_o = (V_{DD}/ R_L)$

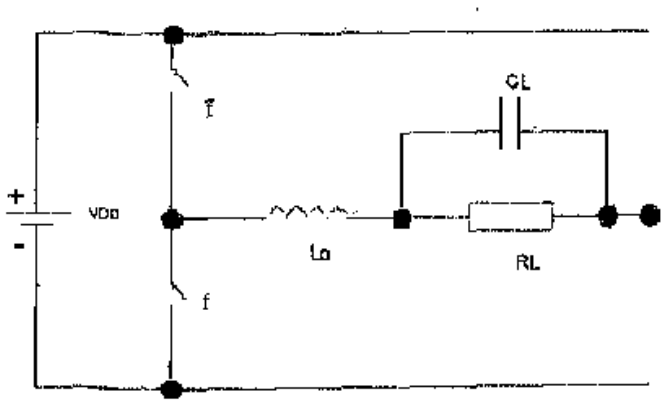



*Fig 2.7 Switches symbolised output stage*

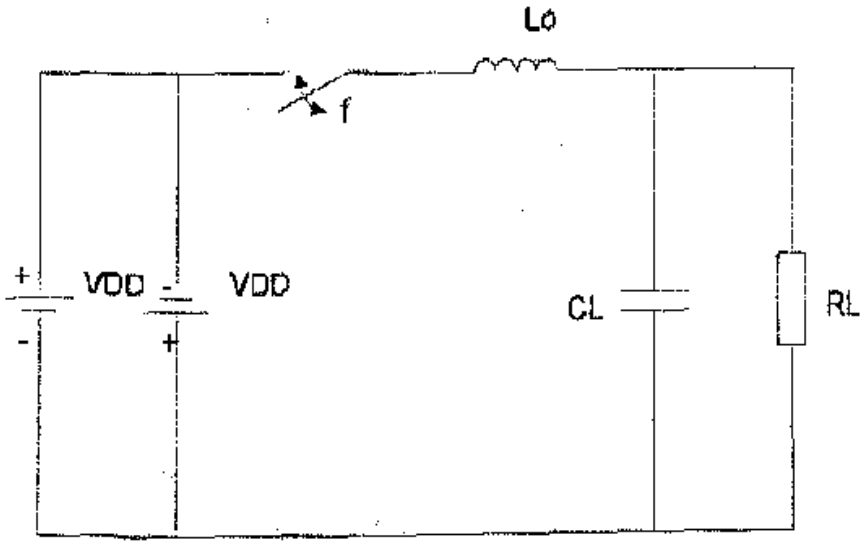



*Fig 2.8 Equivalent circuit of output stage*

Since the output stage is ideal, the output power $P_{out}$ will be equal to the total power $P_E$ and the efficiency will be equal. As mentioned earlier, in an actual Class D amplifier, it also suffers from power dissipation due to transistor's parasitic capacitance, short-circuit current and the on-resistance.

## 2.5 LOSSES IN SWITCHMODE CLASS D AMPLIFER

As mentioned earlier, in contrast to the traditional Class A, B and C amplifier, switch-mode power amplifier such as the Class D amplifier have theoretical efficiency of 100%.

Thus one will assume that the switching devices are ‘ideal’. However such ideal device or component do not exist, so losses in the switching power amplifier must be considered.

## 2.3.1 TURN –ON SWITCHING LOSSES

At the turn-on instant, the device has a high voltage across its output terminals and no current. The voltage starts to fall from its initial value and the current starts to rise toward its final value. If this voltage fall is not an instantaneous, there is a crossover period when both the current and the voltage are non-zero. A significant amount of energy can be dissipated during this time. The power dissipate during this mechanism is proportional to the length of the crossover period. It is also proportional to the switching frequency as the energy loss occurs every switching cycle [9]. This loss is negligible in Class D amplifier circuit as the turn-on occurs at a zero-crossing [9].

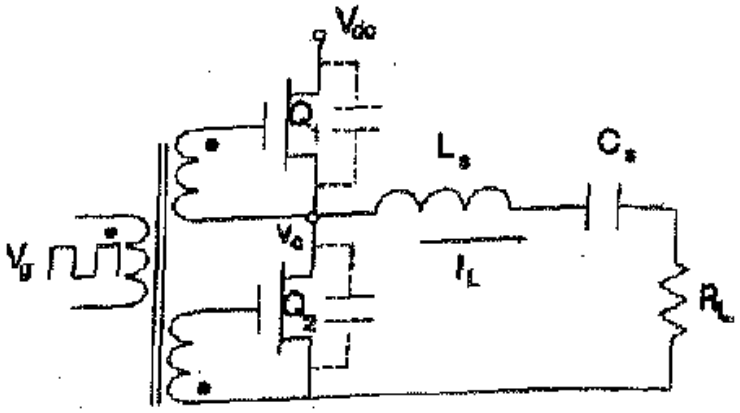



*Fig 2.9 Voltage switching Class D amplifier*

A more important loss mechanism that occurs at the turn-on transition is due to the discharge of the energy stored in the output capacitor of the semi-conductor power devices. This capacitance is intrinsic to the device, a result of the existence of PN junctions. Even an ideal system cannot eliminate this type of losses.
The device capacitances are non-linear and vary with the drain-to-source voltage. In a Class D circuit, (*Fig 2.9*), there are two devices that switch on and off alternately. If the

first device is off, then the voltage across it is equal to the rail voltage $V_{dc}$ and the energy stored in the output capacitor $C_{oss}$ is

$$E_d = \frac{1}{2} C_{oss} V^2_{dc} \qquad (2\text{-}3)$$

This energy is being dissipated once in every cycle of the switching frequency; therefore, the discharge power loss is

$$P_d = \frac{1}{2} C_{oss} V^2_{dc} f_s \qquad (2\text{-}4)$$

Simultaneously, the capacitor of the second device is charged through the resistance of the first device to the rail voltage. As we assume the output capacitances are fixed, then the charging process dissipates an amount of energy equal to the equal amount of energy being stored. Thus, the turn-on loss in a Class D circuit at every switching transition will be twice the loss of $P_d$. As there are two switching transition per cycle, the total turn-on losses in a Class D circuit is four times the loss of $P_d$ [9].

### 2.3.2 TURN-OFF SWITCHING LOSSES

The same type of crossover power loss that occurs at the turn on also occurs at the turnoff. In contrast to the turn-on period, there is no capacitor voltage discharge loss. However, there is a dual type loss caused by the current flowing in the parasitic inductors. At turnoff, the current is flowing through the leads and wire bonds into the device. In general, parasitic inductances are associated with these leads. The energy stored in these inductances is equal to

$$E_L = \frac{1}{2} L I^2 \qquad (2\text{-}5)$$

where L is the parasitic inductance value and I is the flowing at the turnoff instant. The power loss from this discharge is also proportional to the switching frequency is given by

$$P_L = \frac{1}{2} L^2 f_s \qquad (2\text{-}6)$$

In contrast to the capacitive discharge loss, in which the device capacitance are not under the control of the designer, the inductive discharge losses can be reduce by proper design of the circuit [9].

## 2.3.3 GATE DRIVE LOSSES

At low frequency, MOSFET's consume very little drive power, but as the frequency increases, the power dissipation caused by the charging and discharging of the gate capacitance becomes significant. For the sake of simplifying the analysis, the gate circuit is represented by a series RC circuit in *Fig 2.10.*

The gate charge required to turn on a device is the best way to correctly predict the gate drive requirement. The gate drive power requirement is dependent on the type of drive being used: a square-wave drive and a sinusoidal gate drive but only the square-wave drive will be discussed here.

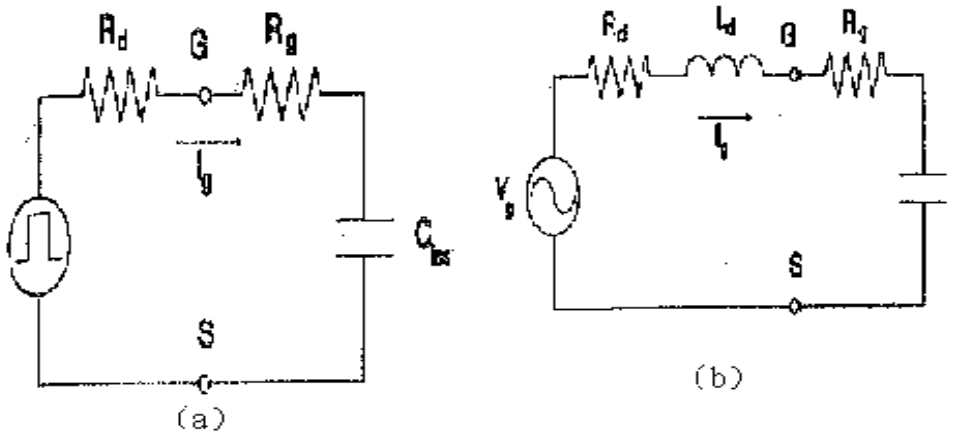



*Fig 2.10 (a) The simplified equivalent circuit of the gate and gate drive circuit. (b) The simplified equivalent circuit of a resonant gate drive circuit.*

In the case of a square-wave drive, the input voltage is the square wave but the input current is a pair of pulses. A gate is being charge through a resistor, the same amount of

energy dissipated in the resistor during the channel process. Similarly, when the gate is discharge, the energy is dissipated resistively. Therefore, the loss associated with the device on and off per cycle is two times of $P_d$ and the power loss is given by

$$P_g = V_{gs} Q_g f_s \qquad (2\text{-}6)$$

Where $Q_g$ is the charge required to raise the gate voltage, $V_{gs}$.

The peak current required to switch an MOSFET is dependent on the desired switching speed. The time constant of the RC network determines the length of time $t_{on}$ it takes the gate capacitance to charge up to $V_{gs}$. Typically, it takes a total time equal to $4\tau$ to fully charge a capacitor. Therefore, for a gate capacitance $C_{iss}$, one can calculate a desired value of gate resistance Rg and gate drive circuit resistance $R_d$ as follows :

$$T_{on} = 4\tau = 4 ( R_d + R_s ) C_{iss} \qquad (2\text{-}7)$$

The value of $C_{iss}$ used here is the value at $V_{ds} = 0$, which gives the worst-case scenario for the gate and drive resistances. The peak current in the gate drive circuit is then given by :

$$I_{gp} = \underline{V_{gs} / (R_d + R_g )} \qquad (2\text{-}8)$$

As we can see that the power requirement for the gate drive with a square-wave voltage is independent of the switching speed, and the switching speed is ultimately by the gate resistance [9].

# CHAPTER 3

# IMPLEMETATION OF DESIGN

In this chapter, the Class D amplifier circuit used in the practical simulation was described. The waveforms of the different stages of the simulation and the description of each stage were discussed.

## 3.1 DESIGN OF THE CARRIER SIGNAL

The first step in implementing a Class D amplifier is to generate a pulse-width modulated signal as shown in *Fig 3.1.*

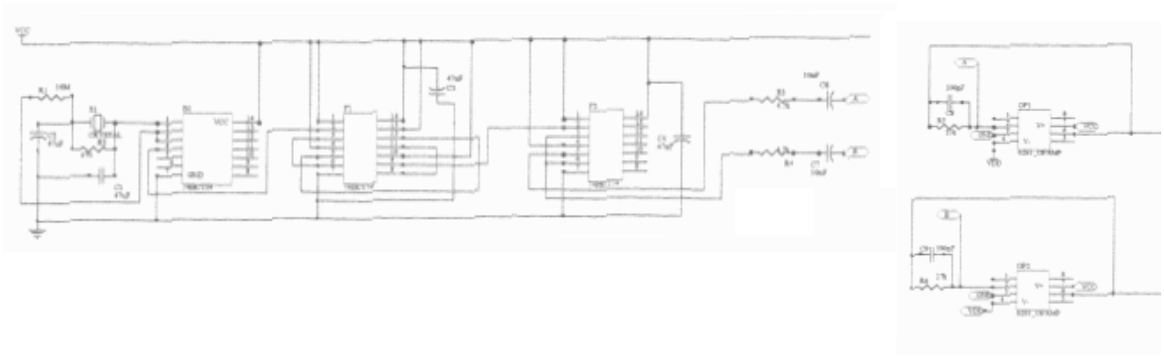


*Fig 3.1 Design of a Pulse-Width Modulator*

### 3.1.1 GENERATION OF SQUARE WAVE

From *Fig 3.1*, we can see that in order to create a PWM signal, a square wave is required so as to produce a triangular wave by integrating this square wave. A crystal of 1MHZ is used to generate this square wave as shown in *Fig 3.2.* The slight overshoot to the switching edge of the clock signal is due to the switching imperfection of the crystal.

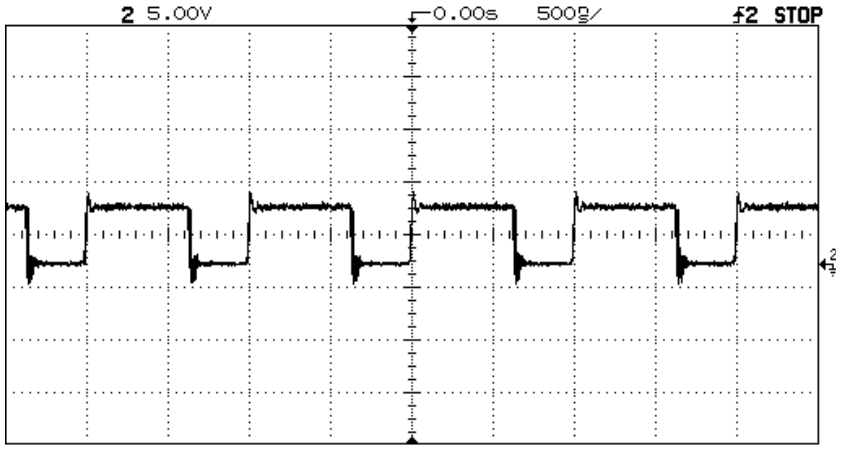



*Fig 3.2 Square wave generated from the 1MHZ crystal*

This generated square wave is the fundamental waveform to generate our carrier waveform as we have to integrate this square wave to obtain a triangular wave, which is the carrier signal. As the required carrier frequency is at about 125KHZ for a suitable comparison with the audio frequency of 20KHZ, we need to reduce the frequency down from 1MHZ by passing through a number of flip-flops (Lm74LS74).

The function of the each flip-flop is to divide its input signal by half, which mean that by passing through one flip-flop the 1MHZ square waves frequency will be reduce to 500KHZ. From the connection in *Fig3.1*, the square pulse generated from the crystal was fed into the clock pin of the first flip-flop. The set and reset pins are tie to high to deactivate them. The inverting output of the first flip-flop is connected to the data input of the flip-flop. The clock would have a constant pulse signal and the data pin would read in the inverting output. Assuming that the initial value of the non-inverting input is low, the non-inverting output would be high, which mean that the data input would be high too. As the clock only passes signal through to the output at every rising edge, it would take one clock cycle to send out high to the non-inverting output. The non-inverting output would then below and was fed into the data pin again, the cycle will be repeated. Thus we need to pass through 3 flip-flops in order to reduce the frequency to the desire level of 125KHZ as shown in *Fig 3.3.*

Another identical square wave was produce at 180° phase different from the original for the purpose of creating the second level switch-mode supply and subsequently the third level. The inverting square wave can be obtained from the inverting output pin of the flip-flop.

In *Fig3.3*, the final square wave of both the inverting and non-inverting output from the flip-flop is shown. The desired frequency is of 125KHz is obtain and the distortion level is reduce because when the as the square wave passes through the flip-flop, some of the noise (distortion) is being attenuated by the flip-flop.

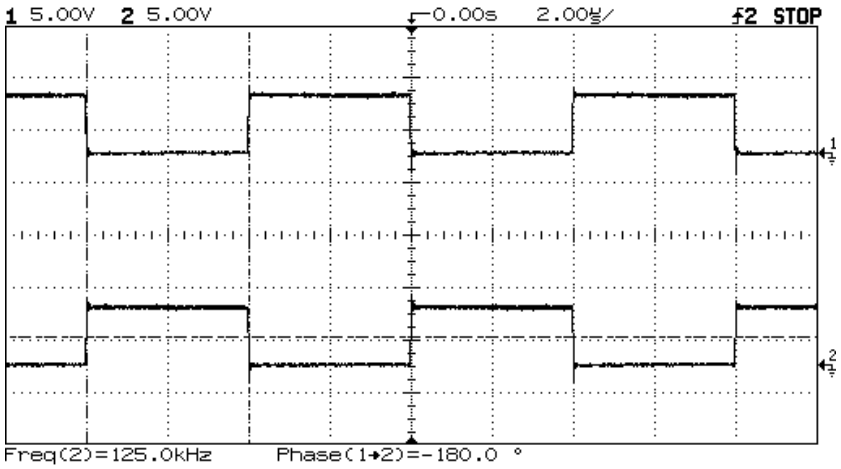



*Fig 3.3 The final waveform of the square wave at 125KHZ.*

## 3.1.2 GENERATING OF THE CARRIER SIGNAL

The next step after generating the square wave is to produce the carrier component by integrating the square wave. Since the square wave is running at a high frequency, a high speed op-amp is required to perform the integration. As such, a Lm6361 is selected due to its high slew rate and high frequency characteristic. As shown in *Fig 3.1*, the output from the flip-flop is pass through a capacitor and resistor before inputting into the op-amp to be compare with the audio signal. The resistors *R3* and *R5* limit the DC gain of the op-amp and the selection of the resistance values are important so that we would not get too high of the DC gain than required. The capacitor *C2* is then chosen for the purpose of

integrating of the square wave together with resistor *R5* and is calculated by the following calculations :

Carrier Frequency, Fc = 125KHZ ; $\tau$ = 8μsec

$\tau_{on}$ = 8 * 2 = 16μsec;

Since $\tau$ = R * C (3-1)

and R is chosen at 27kΩ ,

Therefore *C2* = 16μ / 27 kΩ ≅ 592pF

A preferred value of 350pF is used.

The selection of the capacitor *C2* value is important as it determine the time needed for the capacitor *C2* to charge up to the desired value. If the capacitance was too small, it would had a short charging and discharging time and if the capacitance chosen was too large, the charge up and discharge time will be too long. In both cases, an arc would be produced at the charging and discharging line and a distorted triangular wave would be produced. Thus it is important that the carrier signal be kept as close to a clean triangle as possible as the total harmonic distortion(THD) and the inter-modulation distortion (IMD) will increase dramatically.

By choosing a suitable value, the integration can be done very smoothly with only a slight overshoot at the peak due to the previous effect from the square wave (*Fig 3.4). C1* is included in the circuit as it provides a zero offset to the input waveform of the op-amp by providing a virtual earthing (0V). This step is important as this carrier waveform is to be compared to a sine wave which will has a zero DC offset. By doing so, the output triangular waves are offset to zero DC as shown in *Fig 3.4.* The selection of *C1* is also vital as from the calculation :

Zc = 1 / (2π*f*c) where *f* = 125KHz (3-2)

If C = 100pF, Zc = 12KΩ ;

If C = 100uF, Zc = 0.01Ω

Therefore if the capacitor value chosen was too low, it would perform as a resistor and so no signal would be able to pass through it. On the other hand, if the capacitor was chosen at a range of μF, the capacitor would have very low impedance as well as performing the characteristic of the capacitor.

Similar to the generation the square wave, an identical carrier signal of 180° phase different is also produce by integrating the inverting square wave mentioned in section 3.1.2 with the same method and value.

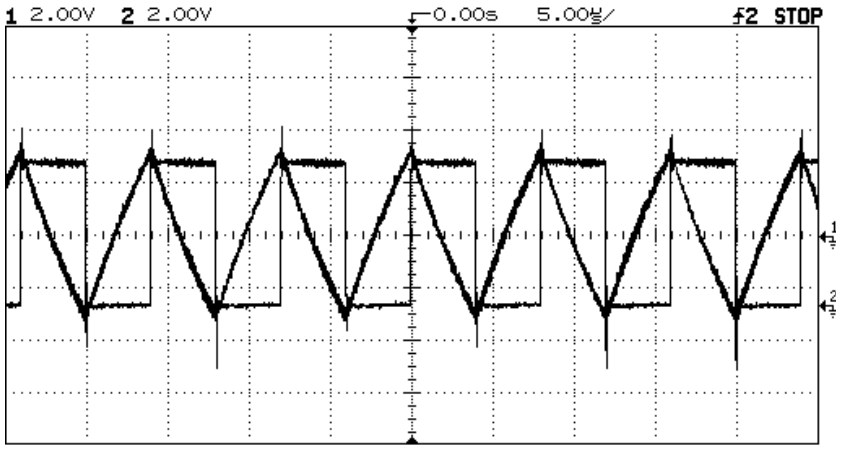
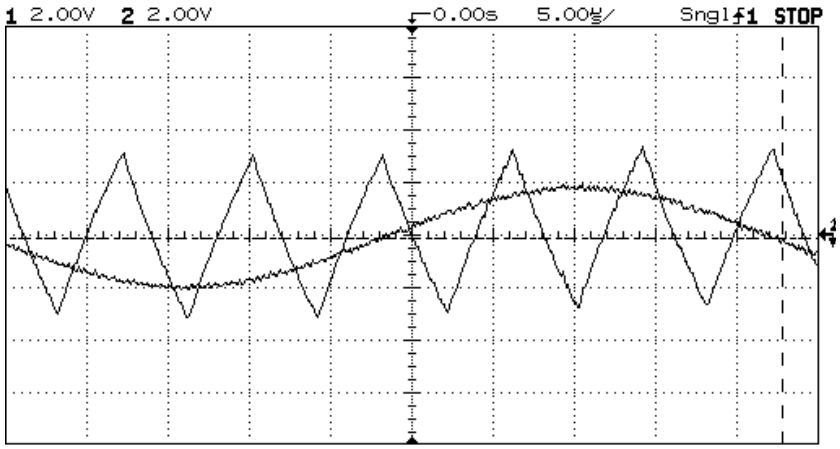



*Fig 3.4 A comparison of the output from the Flip-Flop(2) and the output from the op-amp after the integration(1). Noticing that the square wave rest on the zero voltage line while the carrier signal is offset to zero DC.*

## 3.2 DESIGN OF THE PULSE WIDTH MODULATOR

After producing the carrier signal, the next step was to feed this carrier signal into a comparator together with the input audio signal, which in this design, a sine wave of 20KHZ generated from the signal generator is used for the simulation of audio waveform (*Fig3.5).* A high speed comparator is required for this stage, as a non-ideal comparator

will too increase the distortion level. Thus a LM318 high speed comparator was used in the simulation. The amplitude of the sine wave input is set at $4V_{p-p}$ is design to be less than that of the carrier component in order to produce as accurate results as possible from the simulation. If the input sine wave was larger than the amplitude of the carrier frequency, the comparison may not be accurate as part of the sine wave may be missed out during the comparison. The resultant waveform from the comparator is shown in *Fig3.6.*



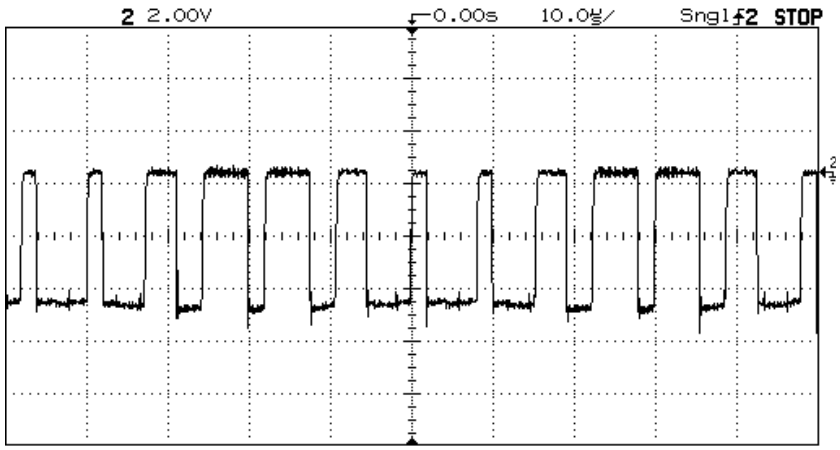




*Fig 3.5 The carrier triangular signal being compare to a sine wave simulation of the Audio signal.*

*Fig 3.6 The resultant PWM wave shape of the comparison in Fig 3.5.*

As shown in *Fig3.6,* the width of the pulse wave changes with the change in the input waveform. When the sine wave goes to negative cycle, the duty-cycles of the pulses will go below 50% and when the sine wave reaches the positive cycle, the PWM will have a duty-cycle of 50% or more. By using the above theory, we can see that the pulse width represented the input signal by varying it pulse width and thus the PWM signalling has been achieved.

After able to achieve a single level of the PWM signal, we can used the inverted carrier signal mention in section 3.1 to generate the second level of the PWM signal. This can be done by using the inverted carrier signal and compared it with the same input sine wave we use for the first level. The same sine wave must be use so that an inverted PWM signal as compared to the first level can be produced. The two level of the PWM signal must have a phase different 180° and it is important in this simulation as they will have an opposite switching characteristic so that they would cancelled each other out in the output stage. The two switching waveform can be seen in *Fig 3.7.*

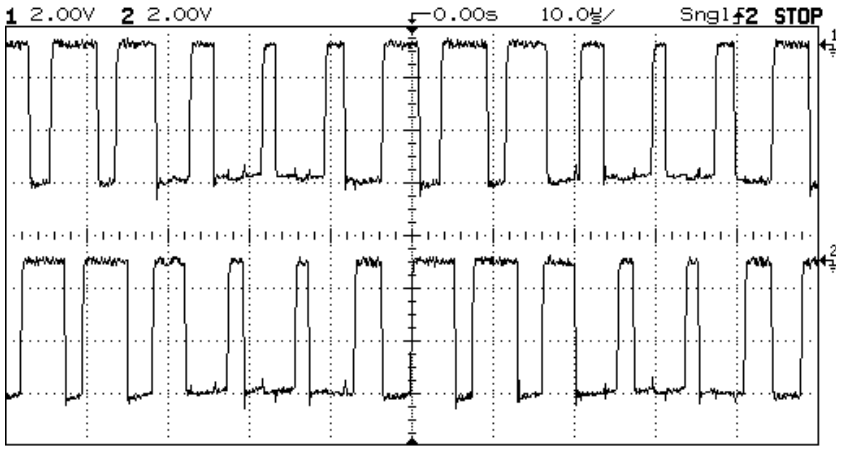



*Fig 3.7 The two switching result from the comparator. A clear inversion of the two signals cannot be seen due to the instability switching of the PWM signal.*

## 3.3 DESIGN OF THE OUTPUT STAGE

The last stage in the designing of the Class D amplifier is the output stage and a schematic of the design is shown in *Fig3.8*. This is the most important design of the Class D amplifier as it will determine the bandwidth and efficiency of the amplifier from its filter design.

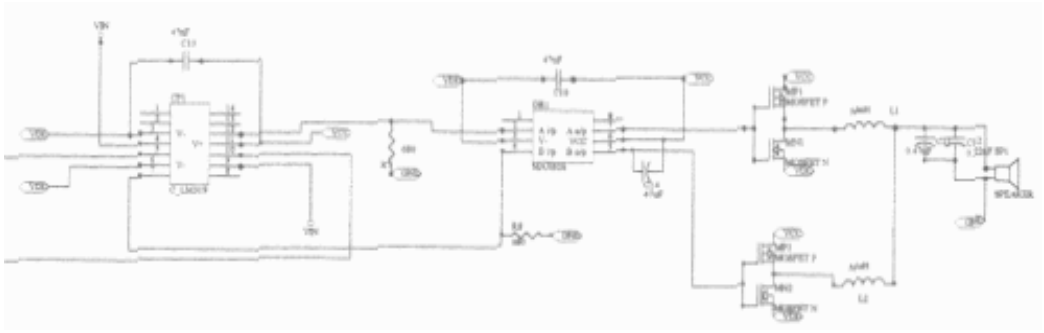


*Fig 3.8 Output stage of the implemented Class D amplifier*

### 3.3.1 MOSFET DRIVER

After generating the PWM signal, we need to pass the PWM signal through a MOSFET driver to boost up its current. It is critical to boost up the signal driven into the MOSFET in order to drive the MOSFET to its saturation point when it is turn-on and have the capability to switch it off completely with minimum distortion. Since the MOSFET driver has a very high peak current output, it is suitable to use at driving the gate of MOS devices. The high current is important since it minimises the time the MOSFET device is in the linear region. The MOSFET will dissipate a significant amount of power if it operate in the linear region for too long. comparison of the PWM signal before and after passing through the inverter driver is shown in *Fig3.9.* The PWM signal after passing the

MOSFET driver was boost up to about $10V_{p-p}$ as compared to the signal of about $4V_{p-p}$ before passing through the driver.

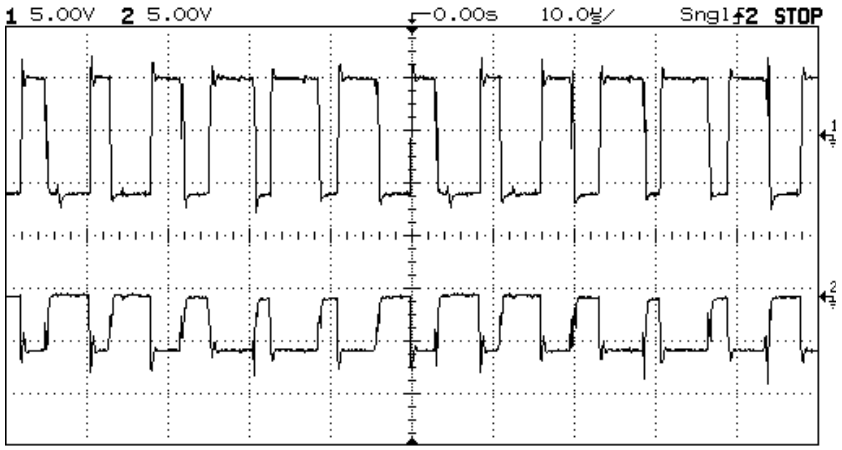



*Fig 3.9 A comparison of the PWM signals before(2) and after(1) passing through the driver. The voltage of the signal before the driver is at about $3V_{p-p}$ and the signal is boost up to about $5V_{p-p}$.*

From *Fig3.9*, it is observe that the distortion of the PWM after passing through the driver is relatively visible but this will not contribute much to the distortion, as the MOSFET will only read the input from the driver as 'on' or 'off' state. An inverting driver is use in this simulation for the purpose of the MOSFET connection as shown in *Fig3.1*.

After boosting up the signal for the MOSFET, the signal from the driver will be fed to the a P-type and a N-type MOSFET connected in series. Since the P-type is connected to the positive 5V supply and the N-type is connected to the negative 5V supply, the output from the half-bridge MOSFET connection will be inverted from the input signal as shown in *Fig3.10.* As we can see that the pulse signal has already been amplified and since the pulse represented the signal waveform, the output signal is expected to amplify too. An identical MOSFET design is implemented for the second level design.

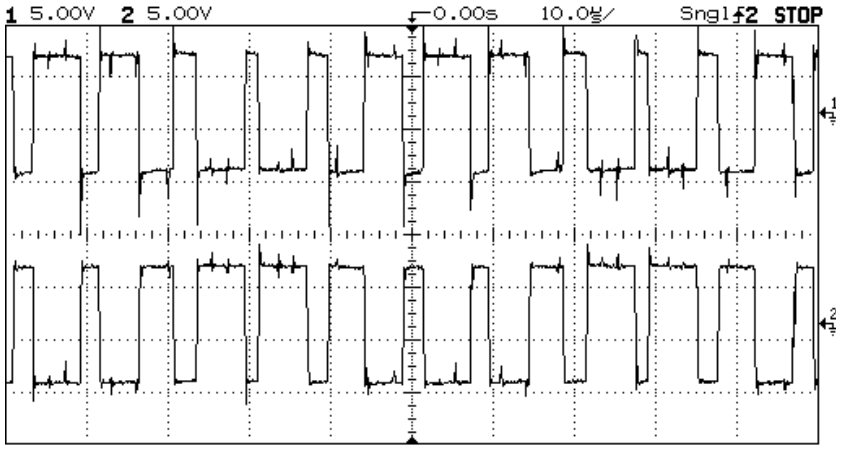



*Fig 3.10 A comparison of the input(1) and the output(2) signal of the MOSFET. A clear inversion of the input signal can be clearly seen*

## 3.3.2 FILTER DESIGN

The last stage of the design is the filter design stage. This stage is very critical as it combines the first and second level to form the third level of the switch-mode supply. A LC low pass filter is best considered here. The –3dB point was set at 30KHZ. The best transient response would be best at critical damping for an 8Ω load. The loaded filter is analysed below.

$X1 = sL$

$X2 = 1 / sC \parallel R = R / ( 1+sCR )$

The transfer function

$H = V_o / V_i = X2 / ( X1+X2 ) = 1 / ( 1 + X1 / X2 )$

$H(s) = 1 / ( 1 + sL ( 1 + sC ) / R )$

$= 1 / ( 1 + sL / R + s^2 LC )$

$D(s) = 1 + s.L / R + s^2 LC$

But $D(s) = 1 + s.2\zeta / \omega + s^2.1 / ( \omega^2 )$ (3-3)

Where $\omega$ = pole frequency in rad/s and

$\zeta$ = damping ratio

Equating these equation for D(s),

$\omega^2 = 1 / LC$ $\zeta^2 = L / R^2 C$

$LC = 1 / \omega^2$ $L / C = R^2\zeta^2$

Choosing $\omega$ = 30KHZ which is 18850 rad/s

$R = 8\Omega$, $\zeta = 1$ (critically damped)

For 3 level design,

Calculating L = 42.4e-6 = 42μH

C = 0.663e-6 = 0.66μF

Choosing a preferred value C = 0.69μF

L would be 41μH but a preferred value of 56μH is chosen and due to the parallel connection of the two inductor, the total inductance will be 28μH.

Therefore,

$\zeta$ = 0.79(under-damped)

Since it is easier to change the value of the capacitor, the inductor value would remain the same and varies the capacitor value in order to obtain a better damping ratio. Using the same assumption of $\zeta = 1$ and keeping the resistor and inductor value the same, the new value for the capacitor, C = 0.44uF. Choosing a prefer value of 0.42uF, the new damping ratio, $\zeta = 1.05$ (slightly over-damped).

The 56μH inductor was chosen to be the type wound on a ferrite rod rather than a gapped core type to prevent saturation problems. The inductor was also chosen to be able to withstand a current of up to 1.5A. Although the power loss through the inductor may be a bit too high for low voltage, but this is the most suitable available.

After passing through the inductor, we then perform the same procedure for the second level by passing through another inductor of the same value. The two signal are then

connect to the 0.42μF capacitor to filter off the high carrier frequency. The output waveform after the filtering is shown in *Fig3.11*.

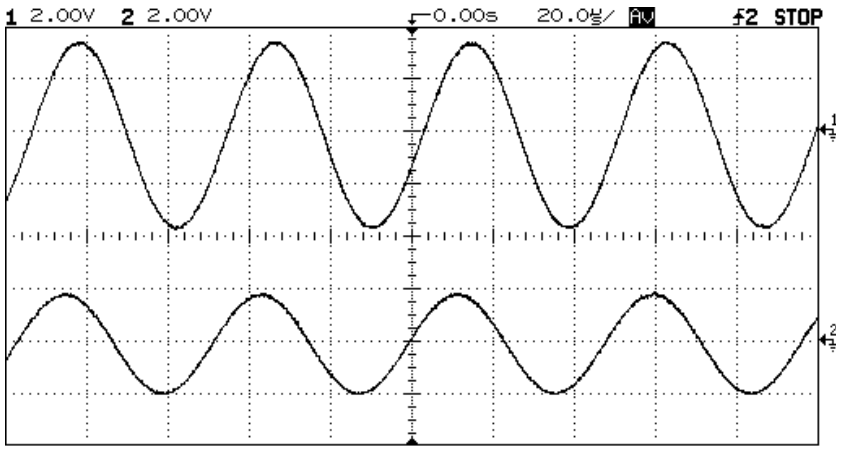



*Fig 3.11 The output signal(1) compare to the input signal(2). Notice the amplifying of the output signal*

From *Fig 3.11*, the gain for the amplifier for a signal of 20KHz can be calculated as :

Gain, $Av = V_o / V_i$ where $V_o = 3.2V_p$ and $V_i = 2V_p$

Therefore, $Av = 1.6$ @ 20KHz.

This is not the peak gain value that the amplifier can achieve. The analysis of the data recorded would be discussed in the next chapter.

# CHAPTER 4

# DISCUSSION

In this chapter, the different results from the hardware implementation would be discussed. The spectrum of the outputs, the bandwidth of the 1 and 3 level Class D amplifier and the effect of different damping ratios of the output stage would be analyst.

# 4.1 RESULTS OF ONE AND THREE LEVELS OUTPUT

## 4.1.1 OUTPUT WAVEFORMS

The output waveform of the one level Class D amplifier can be seen in *Fig4.1*.

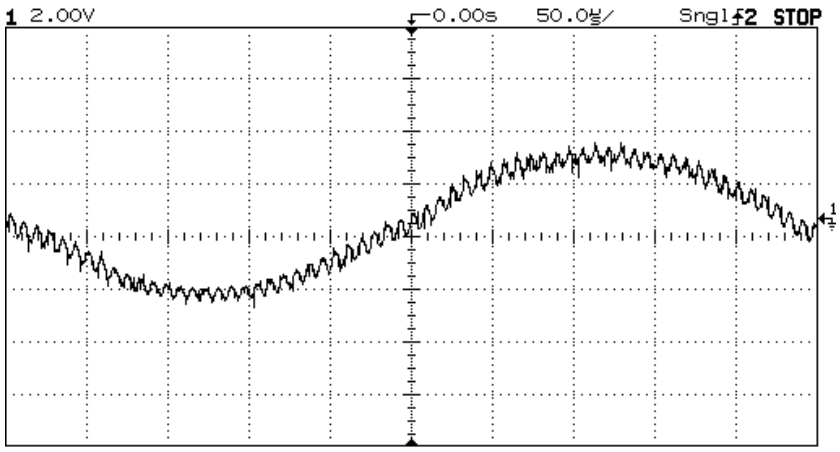


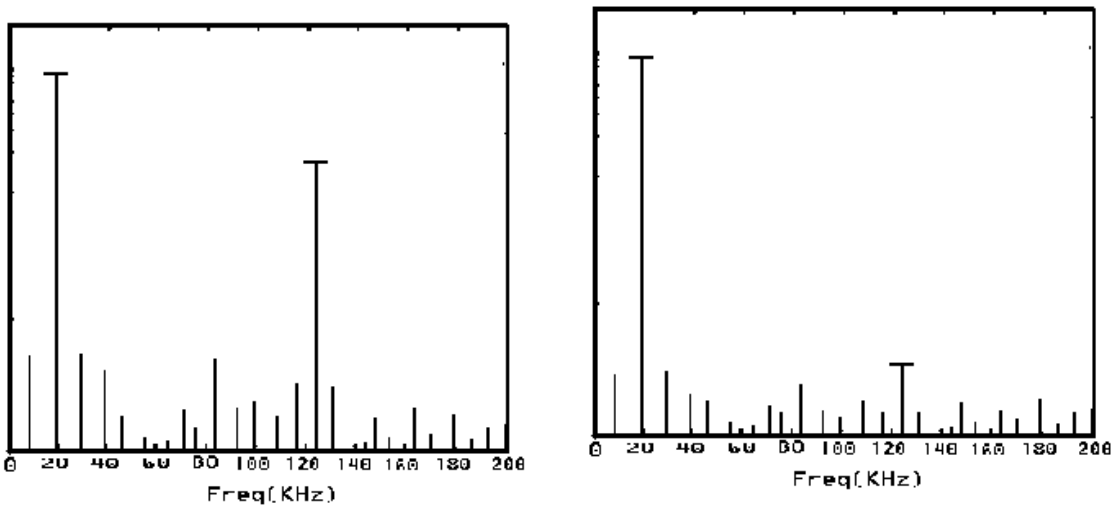

*Fig 4.1 Output waveform of one level Class D amplifier from a signal of 2KHz.*

This result is shown at an input frequency of 2KHz for the purpose of discussion as the switching of the switch-mode supply can be seen more clearly. After the filtering stage, the input signal can be view with the inclusion of the switching signal still present. This is because the LPF (Low Pass Filter) was not able to filter off the carrier frequency completely. From the value of the inductor and capacitor used for the LPF in the simulation, the cut-off frequency can be calculated as follow :

$$W^2 = 1/LC \quad \text{where} \quad L = 28uH \text{ and } C = 0.42uF$$

Therefore W = 291600 rad/s or Frequency = 46KHz

Since the design filter is decaying at a rate of 40dB/decay, the expected stopband frequency should be at 200KHz, therefore the carrier frequency of 125KHz would not be completely eliminated as shown in *Fig4.2*. Although the carrier frequency would not be able to completely attenuated, its magnitude would be scale down because of the filter. With the introduction of the 3 level switch-mode, the carrier frequency would be able to cancelled out since the two carrier frequencies are 180° out of phase from each other. In the hardware simulation, this cancellation may not be able to clear the carrier signal completely because the phase different of the two carriers did not stay constant at 180°. The spectrum of the one and three levels output can be seen in *Fig 4.2.*




(a) (b)

*Fig 4.2 The spectrum analysis of the one(a) and three(b) level output for a signal input of 20KHz.*

From the spectrum diagram, the spectrum of the carrier frequency are visible for the one level but is reduce for the three level output. A small level of the carrier frequency spectrum can still be viewed from the output of the three level output due to the imperfect design of the filter. Although the carrier frequency may still present, its amplitude had already been reduced significantly due to the filtering and cancellation effect. An

improvement of the output wave shape can be done by several methods, for example increasing the number of levels of the switch-mode supply or by improving the design of the LPF. Since the design of a low pass filter with a stop-band frequency before 125KHz were difficult and hard to implement, the use of a multi-levels switchmode to produce a cleaner signal is preferred.

## 4.2 DESIGN OF THE LOW PASS FILTER (LPF)

The design of the LPF is very important as it ultimately determine the bandwidth of the amplifier. The ideal output of the amplifier would be to achieve a LPF, which would attenuate the carrier frequency, a flat pass-band bandwidth for a range of the audio frequency and a damping ratio of 1. In real life, it is hard to achieve the above specification. Thus the best result can be chosen by analysing the different bandwidths of the output by changing the filter design.

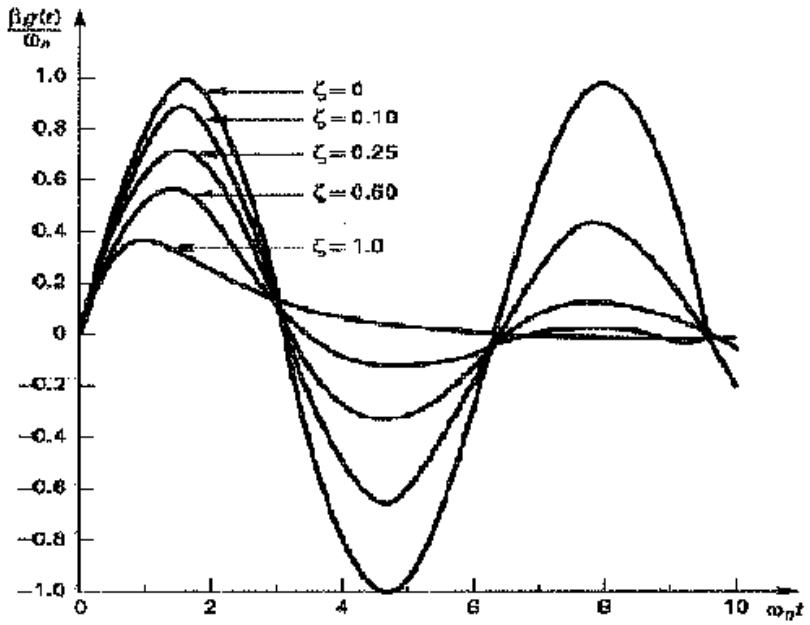



*Fig 4.3 Impulse response of a system with different Damping ratio*

*Table 4.1* is a compilation of result to determine the bandwidth of the amplifier with different damping ratio. Note that if the damping is within the range of $0<\zeta<1$, then the response is a damped sinusoid. For $\zeta = 0$, the sinusoid is undamped, or of substain amplitude. For $\zeta \geq 1$, the oscillations have ceased. It is apparent from *Fig 4.3* that for $\zeta < 0$, the response grows without limit [feedback control]. Thus a reading of the damping ratio of as close to one as possible is taken as it produces the best response. The damping ratio is varying in this case by changing the value of the capacitor while the inductor and resistor values are kept constant [10].

In *table 4.1*, a capacitor of 0.44uF is chosen which will yield a damping ratio of 0.997. As shown from the table the gain of the amplifier remains constant at 4.24dB(1.63) from a low frequency of 20Hz to about 13KHz. The gain started to increase to a maximum peak of 8.3dB due to the damping effect of the filter design. The filter had a cutoff frequency of at about 65KHz which make a bandwidth of about 65KHz.

From *Fig4.5*, a bandwidth of the bandwidth of the Class D amplifier was plotted. A flat pass band from 20Hz to about 13KHz can be seen from the figure. This shows the desired constant gain required for a amplifier to operate with the range of audio frequency. The result of the under-damped effect from the filter can also be seen from the plot.

In this experiment, the percentage overshoot of the amplifier was also studied. In an ideal situation, the percent overshoot can be calculated as below :

$$\text{Percent overshoot} = e^{-[\zeta\pi/(1-\zeta^2)^{1/2}]} * 100\% \qquad (4\text{-}1)$$

Thus the percent overshoot is only a function of $\zeta$ and is plotted versus $\zeta$ in *Fig 4.4*. Therefore with a damping ratio of 0.997, the expected percent overshoot would be almost zero. From the simulation, the recorded overshoot was about 8 to 9% in the operating bandwidth due to the physical implementation of the hardware [10].

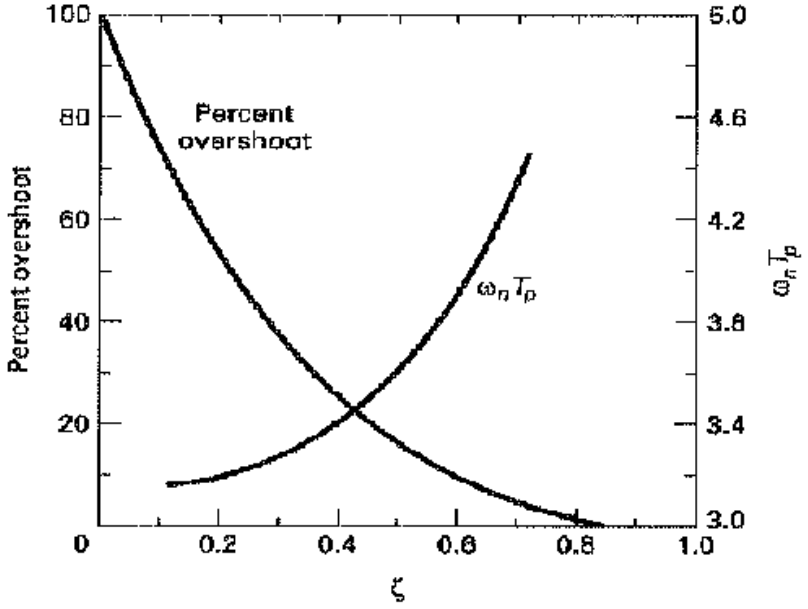



*Fig 4.4 Relationship of percent overshoot against ζ*

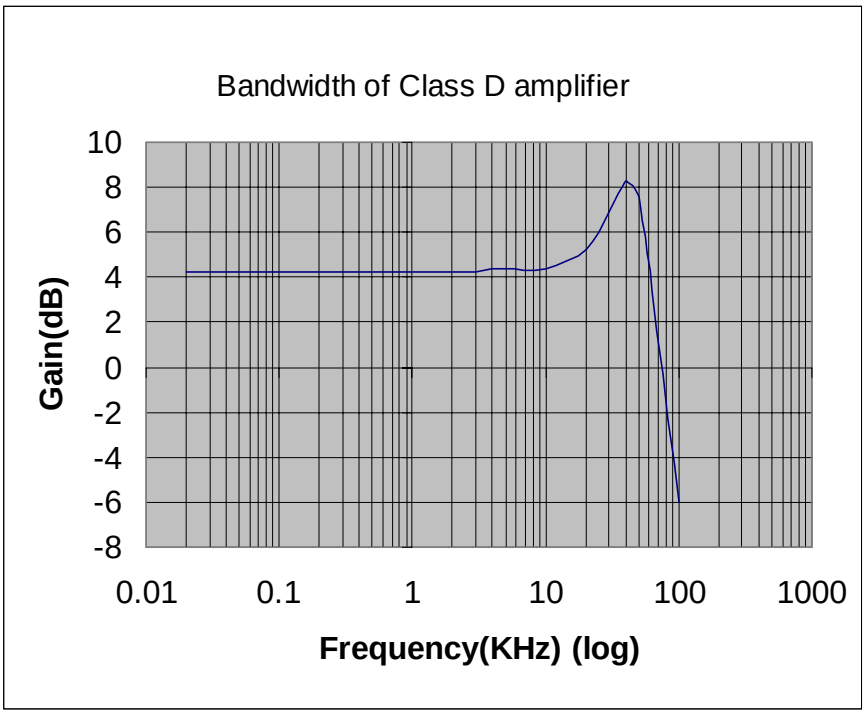



*Fig4.5 Bandwidth vs Frequency plot of Class D amplifier*

**3 level, Vin = 1Vp, Damping ratio = 0.997**

| Freq(Hz) | $V_{op}$ | Gain | Gain(dB) |
|---|---|---|---|
| 0.02 | 1.63 | 1.63 | 4.243752 |
| 0.03 | 1.63 | 1.63 | 4.243752 |
| 0.04 | 1.63 | 1.63 | 4.243752 |
| 0.05 | 1.63 | 1.63 | 4.243752 |
| 0.1 | 1.63 | 1.63 | 4.243752 |
| 0.2 | 1.63 | 1.63 | 4.243752 |
| 0.3 | 1.63 | 1.63 | 4.243752 |
| 0.4 | 1.63 | 1.63 | 4.243752 |
| 0.5 | 1.63 | 1.63 | 4.243752 |
| 1 | 1.63 | 1.63 | 4.243752 |
| 2 | 1.63 | 1.63 | 4.243752 |
| 3 | 1.63 | 1.63 | 4.243752 |
| 4 | 1.66 | 1.66 | 4.402162 |
| 5 | 1.66 | 1.66 | 4.402162 |
| 10 | 1.66 | 1.66 | 4.402162 |
| 20 | 1.83 | 1.83 | 5.249022 |
| 30 | 2.2 | 2.2 | 6.848454 |
| 40 | 2.6 | 2.6 | 8.299467 |
| 50 | 2.4 | 2.4 | 7.604225 |
| 100 | 0.5 | 0.5 | -6.0206 |

*Table 4.1 The compile results of the amplifier output at a dampimg ratio of 0.997*

# 4.3 EFFICIENCY OF CLASS D AMPLIFIER

As mention in chapter 2, the efficiency of the Class D amplifier in a ideal case is 100%. In real life implementation, a efficiency of 100% is impossible due to the varies losses discussed in section 2.5, thus the efficiency of the implemented amplifier was recorded and analysis. The efficiency of a amplifier can be calculated by :

$$\eta = (P_{out} / P_{in}) \times 100\% \qquad (4\text{-}2)$$

where $P_{in}$ = Power input and

$P_{out}$ = Power output

Since power is supply to the internal circuitry of amplifiers from a power supply. The power supply typically delivers current from several dc voltage to the amplifier. The average power supplied to the amplifier by each voltage source is the product of the average current and the voltage. The total power supplied is the sum of the power supplied by each voltage source [11].

$$P_s = (V_{cc} * I_{cc}) + (V_{dd} * I_{dd}) \qquad (4\text{-}3)$$

Where $V_{cc}$ = positive input voltage

$I_{cc}$ = positive input current

$V_{dd}$ = Negative input voltage

$I_{dd}$ = Negative input current

The output power delivered to the load is usually much greater than the power taken from the signal source and this addition power is often taken from the power supply. Not only is this additional power taken from the power supply, the power taken from the supply can also be dissipated as heat in the internal circuitry of the amplifier. Thus the sum of the power entering the amplifier from the signal source $P_i$ and the power from the supply $P_s$ must be equal to the sum of the output power $P_o$ and power dissipated $P_d$:

$$P_i + P_s = P_o + P_d \qquad (4\text{-}3)$$

Usually the input power to the amplifier is insignificant to the other term and so we neglect the effect of $P_i$ in our calculation.

Since the gain of the amplifier is determine by the PWM, therefore the output power can be calculated from the output of the PWM. The calculation can be done by using equation 4-3. *Table 4.2* shows a tabulation of the recorded data and *Fig 4.6* is a log graph plot of the data.

**EFFICIENCY OF CLASS D AMPLIFIER**

| Freq.(KHz $V_{in(p)}$ (v) | $I_{i(p)}$ (mA) | $Vo_{(p)}$ (v) | $I_{o(p)}$ (mA) | $P_i$ (mW) | Po (mW) | Efficiency(%) |
|---|---|---|---|---|---|---|
| 0.02 | 5 | 89 | 5 | 29 | 445 | 145 | 32.58426966 |
| 0.03 | 5 | 89 | 5 | 30 | 445 | 150 | 33.70786517 |
| 0.04 | 5 | 89 | 5 | 30 | 445 | 150 | 33.70786517 |
| 0.05 | 5 | 89 | 5 | 31 | 445 | 155 | 34.83146067 |
| 0.1 | 5 | 89 | 5 | 32 | 445 | 160 | 35.95505618 |
| 0.2 | 5 | 89 | 5 | 32 | 445 | 160 | 35.95505618 |
| 0.3 | 5 | 89 | 5 | 33 | 445 | 165 | 37.07865169 |
| 0.4 | 5 | 89 | 5 | 33 | 445 | 165 | 37.07865169 |
| 0.5 | 5 | 89 | 5 | 34 | 445 | 170 | 38.20224719 |
| 1 | 5 | 89 | 5 | 35 | 445 | 175 | 39.3258427 |
| 2 | 5 | 90 | 5 | 41 | 450 | 205 | 45.55555556 |
| 3 | 5 | 90 | 5 | 41 | 450 | 205 | 45.55555556 |
| 4 | 5 | 90 | 5 | 43 | 450 | 215 | 47.77777778 |
| 5 | 5 | 90 | 5 | 43 | 450 | 215 | 47.77777778 |
| 10 | 5 | 91 | 5 | 58 | 455 | 290 | 63.73626374 |
| 20 | 5 | 92 | 5 | 74 | 460 | 370 | 80.43478261 |
| 30 | 5 | 93 | 5 | 81 | 465 | 405 | 87.09677419 |
| 40 | 5 | 94 | 5 | 89 | 470 | 445 | 94.68085106 |
| 50 | 5 | 89 | 5 | 80.5 | 445 | 402.5 | 90.4494382 |
| 100 | 5 | 79.5 | 5 | 42 | 397.5 | 210 | 52.83018868 |
| 110 | 5 | 79 | 5 | 34 | 395 | 170 | 43.03797468 |
| 120 | 5 | 79 | 5 | 33 | 395 | 165 | 41.7721519 |
| 130 | 5 | 79 | 5 | 33 | 395 | 165 | 41.7721519 |
| 140 | 5 | 78 | 5 | 33 | 390 | 165 | 42.30769231 |

*Table 4.2 Efficiency of a Class D amplifier*

It can be observed that the as the frequency of the amplifier increases, the efficiency of the amplifier increases too until at about to the 40KHz point where it yield the highest efficiency before it started to decrease. As the frequency exceeded the cutoff frequency, the efficiency of the amplifier was observed to have a sharp drop. A maximum efficiency of about 94% was achieved from the amplifier which satisfy the high efficiency characteristic of a Class D amplifier.

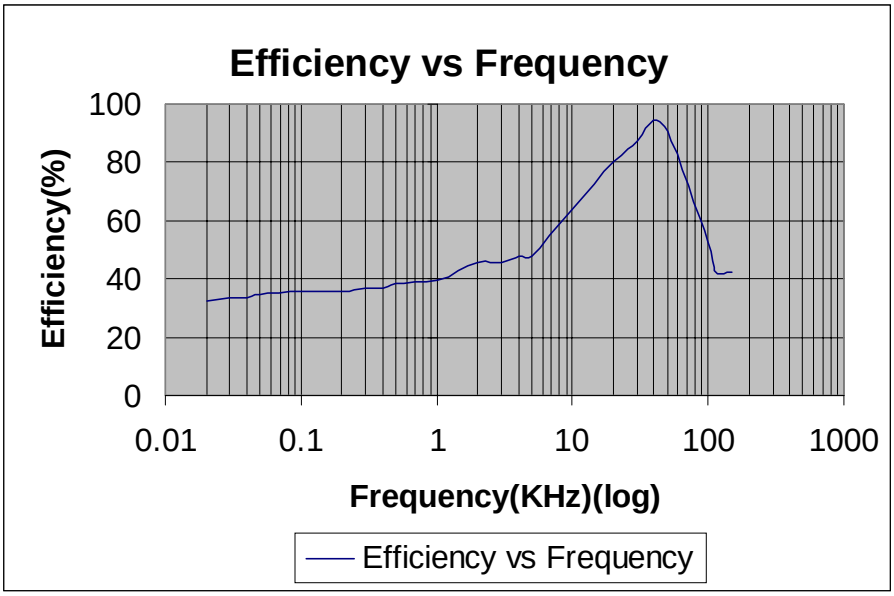



*Fig4.6 Efficiency plot of a Class D amplifier*

The output power from the 8Ω speaker was also recorded and calculated :

$V_{rms}$ (measured) = 1.3V

$I_{orms}$ (measured) = 87mA

R (speaker) = 8Ω

Therefore the power generated at the speaker can be calculated by :

$P = V^2 / R$

$= 0.211W$

This is a reasonably power output for a low power amplifier.

# Chapter 5

# Conclusion

## 5.1 MULTILEVEL SWITCHMODE AMPLIFIER

The use of the multilevel switch-mode supply for amplifiers have been known for many years. It has the advantages of high efficiency and low distortions. In an ideal case, it has an efficiency of 100% and a distortion level of 0 %. It is most commonly use for low frequency application (up to few hundred hertz) as the efficiency level will start to decrease in high frequency application due to the increase in switching losses and the difficulties in implementing a more desirable carrier signal and pulse width modulator.

There are different techniques of constructing the multilevel converter and can be implemented by using the series or parallel connection of individual bridge [3]. Each of the multilevel converter topologies has their own mixture of advantages and disadvantages and each topology will be suitable for a different application.

## 5.1 MULTILEVEL PULSE WIDTH MODUALTION

A multilevel PWM waveform can be regarded as the summation of two separate level of PWM signal. If the two level of waveform are appropriately phase shifted, the amplitude of the voltage and hence the amplitude of the switching harmonic frequency term will be reduce in proportion to the numbers of switching pairs per phase. The output of the PWM will then have a waveform that switches at a value, which is the sum of the two level switching frequencies.

The carrier base PWM technique is most commonly used in the multilevel modulation as compared to the other modulation techniques because of the following advantages :

- it can be easily implemented. As well as the analogue method discussed in chapter 3, software programming with digital circuitry can also be used for the implementation.

- It can be extended to any level of switching required by just creating multiple level of PWM and then summing them together with appropriate phase shifting.

- It has a good dynamic performance, which is suitable for closed loop control.

The understanding of the carrier base modulation application leads to an better understanding of requirements and problems of multilevel modulation of other technique.

## 5.2 LOW PASS FILTER

The design of the output low pass filter has the most substantial effect on the output characteristic of the amplifier. The cut-off frequency is determined by selecting the correct component values. This eventually affects the bandwidth and output wave shape of the amplifier. The damping ratio can also determine the bandwidth characteristic of the amplifier output. The ideal value of damping ration of one is hard to achieve the ratio should be kept as close to 1 as possible to obtain a more constant pass-band gain.

## 5.3 EFFICIENCY

A amplifier can be view as a system that takes power form the dc power supply can converts part of this power into output signal power. For example, a stereo audio system converts part of the power taken from the power supply into signal power that is finally converted to sound by the loud speaker [11]. In the case of the Class D amplifier, the power output is taken from the PWM signal instead of the speaker output because the amplifying was done during the modulation stage. The high efficiency is achieved due to the amplifier not operating in the linear region, thus the losses occur in a linear amplifier is omitted in this case. However, there are still switching losses due to the switching of the transistor. Thus the ideal state of 100% is not obtainable.

Although the Class D amplifier had an ideal efficiency of 100%, but due to losses of the amplifier, an efficiency of about 85% to 95% can be achieved from hardware implementation. In this project, a maximum efficiency of 94% was achieved by measurement and thus accomplished the high efficiency characteristic of a Class D amplifier. It was observed that a high efficiency Class D amplifier was achievable from high frequency signal with a desirable bandwidth although any frequencies higher than KHz may needs a higher level of switchmode amplifier and the efficiency of the amplifier may not be as high as desired.

# REFERENCE

[1] Cheng, Z, *Analysis and design of a micropower low voltage Class D audio amplifier*, Master thesis, Nanyang Technology university, Singapore 1995

[2] Sherman, J.D., *Class D amplifier provide high efficiency for audio system*, EDN, May 1995, pg103 – pg109

[3] Mellor, P.H. & leigh, S.P. & cheetham, BMG, *Reduction of spectral distortion in a Class D amplifiers by an enhanced Pulse width modulation sampling process*, IEE proceedings-G, Vol. 138, No. 4, August 1991

[4] Muhammad H. Rashid, *Power Electronics: Circuits, Devices and Aplications, Prentice Hall*, sydney, 1993

[5] Black, H.S. *Modulation Theory*, Princeton, NJ, Van Nostrand, 1953, pp.261-281

[6] Slobdan Cuk and R.D. Middlebrook, *Advances in switchmode power conversion*, part 1, IEEE transactions on industrial Electronics, vol. 1E-30, No.1, Feb 1983, pg 10- 20

[7] John M.Murray, *Design consideration on Class D MOS power amplifier*, IEEE transcation on electronic and control instrumentation, Vol EECI-26, No 4, Nov 1979

[8] Zheren lai and keyue M. smedley, *A low distortion switching audio power amplifier*, IEEE transcation on industrial Electronics and under control instrument, June 1995, pg174-180

[9] Sayed-amr El-Hamasy, *Design of high efficiency RF Class D power amplifier*, IEEE transcaton on power electroincs, Vol9, No.3, 1994, pg298-301

[10] Charles L. phillips & Royce d. Harbor, *Feedback control systems*(3rd edition), pg 128-129

[11] Allan R. hambley, *Electronics a top-down approach to computer aided circuit design*, Prentice Hall, 1994, pg 34-35