Paralleling Of Power MOSFETs For Higher Power Output

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Abstract - Dynamic current and transition energy unbalance resulting from parameter mismatch between parallel MOSFET branches are mapped over wide operating ranges. Unbalance generator magnitudes are given for HEXFET Power MOSFET data sheet ant typical production batch extremes.

Limit functions are defined for unbalance due to ON resistance, gain and threshold voltage mismatch. Q loci are utilized for mapping dynamic load lines and transition energy. A critical product, average gate current times commutation inductance, and a critical inductance ratio, common source to commutation inductances, are identified.

For worst case parameter mismatch, modest levels of unbalance are predicted through the use of minimum gate decoupling, dynamic load lines with high Q values, common source inductance or high yield screening. Each technique is evaluated in terms of current unbalance, transition energy, peak turn-off voltage and parasitic oscillations, as appropriate, for various pulse duty cycles and frequency ranges.

Results are predicted for a worst case clamped inductive load circuit with an arbitrary number of paralleled IRF150 HEXFET Power MOSFETs.

I. INTRODUCTION

Concepts and design aids are presented for understanding and controlling the steady-state and dynamic current balance between parallel MOSFETs. Dynamic balance is important in power systems employing high frequency, requiring high efficiency or utilizing large pulse currents.

The paper is an extension of earlier work which dealt primarily with the effects of threshold voltage and transconductance (gain) mismatch on current and switching energy unbalance[1, 2, 3]. Current unbalance limit functions are derived herein for threshold voltage, gain and ON resistance mismatches. The latter includes temperature compensation. The effects of MOSFET gate-source and Miller capacitance mismatches and gate decoupling resistance (including parasitics) are evaluated. Non-MOSFET parameter mismatches for drain inductance, common source inductance and gate decoupling resistance are evaluated. Many of the results are generalized for an arbitrary number of parallel devices.

The concept of Q loci is introduced and utilized for mapping dynamic load lines and transition energies. These loci provide a complete generalization that interrelates the MOSFET, its gate driver and the power circuit. The turn-on and turn-off switching loci and corresponding transition energies for a given circuit are easily determined through the use of a simple equation and four graphs.

Unlike other switches[4], parallel MOSFETs do not require additional sharing resistors, dynamic current balancing transformers or active feedback to the driver. It is demonstrated that MOSFET generated unbalance can be held to acceptable levels through appropriate driver design or power circuit design or parameter screening. The degree of control necessary is a function of the application. Most of this work is highly predictable and the paper reviews the relevant factors. A list of recommendations is given at the end of section IV.

I (a) Overview

Section II summarizes the major results and tabulates the primary unbalance resulting from each parameter mismatch considered in the paper.

In Section III, unbalance generators are quantified for International Rectifier HEXFET Power MOSFETs in terms of data sheet extremes and typical production batch extremes. Estimates are used for non-MOSFET parameter mismatch. Maximum current unbalance limits for ON resistance, threshold voltage and gain mismatch are enumerated. Realization of these limits depends on the dynamic load line (Q locus) employed. Current unbalance and transition energy ratios are mapped for various parameter mismatches.

Guidelines are developed in Section IV for reducing unbalance if the predicted limits for given mismatch(es) are considered excessive. Current unbalance and transition energy ratios are evaluated for three different techniques in terms of pulse duty cycle and frequency.

I (b) Analysis Model

The information presented in this paper has been generated for the widely used power circuit in Figure 1 consisting of a voltage source, lead inductance, paralleled switches and a current source with an ideal freewheel diode to represent a clamped inductive load. Transition energies are significant for this configuration.

A worst case representation is used for MOSFET parameter mismatch. N parallel devices are divided into two circuit branches: the first contains a single device with adverse identical parameter mismatch (es); the second contains N-1 devices with identical parameter values.
The MOSFET model used for analysis is given by the following classical equations[5, 6, 7] that describe the switching plane of Figure 2(a):

Active Region —

$$i_D = GF\,(V_{GS} - V_T)^2, \qquad (1)$$
$$V_{DS} \geq V_{GS} - V_T \geq 0$$

Ohmic Region —

$$i_D = GF\,V_{DS}\,\{2(V_{GS} - V_T) - V_{DS}\} \qquad (2)$$
$$V_{GS} - V_T \geq V_{DS} \geq 0$$

where i_D = drain-to-source current
V_{GS} = gate-to-source voltage
V_T = V_{GS} threshold or cut-off value
V_{DS} = drain-to-source voltage
GF = device gain factor (proportional to transconductance, g_{fs})

The applicability of these equations depends on the specific MOSFET being considered. Certain modifications for power MOSFETs have been reported in the literature[6] for the IRF150 used in this paper. A more generalized set of equations would be useful. However, with GF = 1.75 A/V^2, these equations provide a reasonably accurate prediction for the drain current in the active region (equation (1), Figure 2 (b), 25°C and predict the $R_{DS(on)}$ quoted in the data sheet (equation(2), V_{GS} = 10V, i_D = 14A). The main variation from the data sheet occurs in the ohmic region where the IRF150 resistance decreases more rapidly with increasing gate voltage than the equations predict.

Experimental results to support the predictions in this paper are not yet available. An experimental test circuit rated at 5KVA intended for operation in the radio frequency range has been built and tested. Results will be published as they become available.

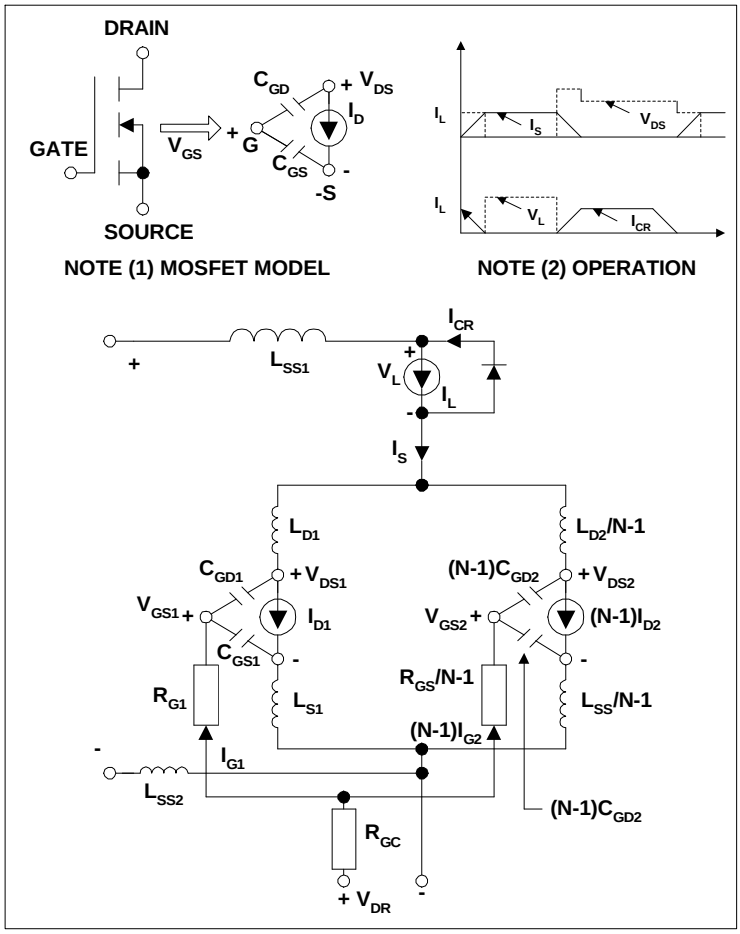


Figure 1 . Clamped Inductive Load MOSFET Power Circuit Containing N Parallel Branches: N-1 Identical; One with Parameter Mismatch (es)

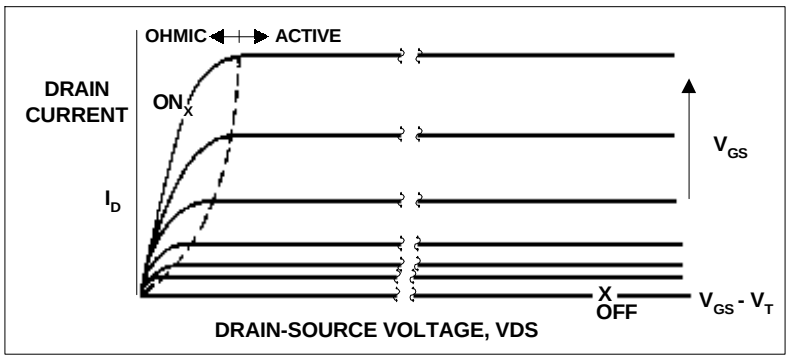


Figure 2(a) : Combined Switching Plane Illustrating Active Region, Equation (1), and Ohmic Region, Equation (2)

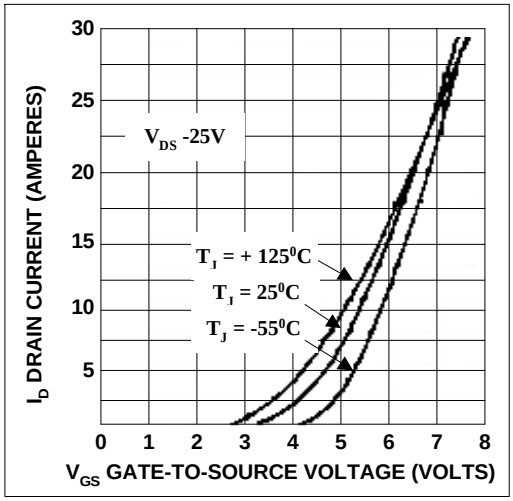


Figure 2(b) : IRF150 Data Sheet Active Region Transfer Characteristics For Deriving Gain Factor (GF) and Threshold Voltage (V_T) in Equation (1)

Figure 2: MOSFET Transfer Characteristics

A Fortran listing of the simulation program used to generate the data in this paper is available upon request.

I (c) Potential Causes of Unbalance

There are several conceivable causes for current unbalance that may result in a particular device exceeding its peak current or continuous thermal ratings. Unbalance may be generated by:

(i) device parameter mismatch
- ON resistance mismatch $R_{DS\ (on)}$
- threshold voltage (V_T)
- gain factor (GF, $\propto g_{fs}$)
- capacitance mismatch (C_{GD}, gate-to-drain (Miller) or C_{GS}, gate-to-source)

(ii) gate driver mismatch
- decoupling resistor (R_G)
- gate loop inductance (L_G)

(iii) power circuit mismatch
- branch inductance (L_D, excluding L_S)
- source inductance common to power and gate circuit (L_S)

Individually or in combination, mismatch between these parameters may produce serious unbalance. For example, consider the circuit of Figure 1 in which eleven IRF150's are sharing a pulse current (I_L) from a clamped inductive load. The first parallel branch contains the mismatched parameters causing the unbalance. The other ten branches are identical and, therefore, equally share load and gate current. Because of the relatively large number of identical parallel branches, typical values are used for the parameters of these branches (refer Table 1).

i_D: maximum 70 A (I_{DM}) continuous 28 A V_T: typical 3 V minimum 2 V g_{fs}: typical 10 A/V minimum 6 A/V C_{GS}: 2650 pf C_{GD}: 350 pf	equivalent to	GF: typical 1.75A/ V^2 minimum 1.05A/ V^2

Table l: IRF150 Data

Consider the unbalance that occurs in branch #1 if its HEXFET Power MOSFET has a V_T of 2.0 volt (2/3 typical) and a GF of 2.45 A/ V^2, (40% more than typical). Remaining parameters are:

V_{DR} = 11V
R_{GC} = 5.2Ω
$R_{G1} = R_{G2}$ = 0
$L_{Dl} = L_{D2}$ = 100 nh
$L_{S1} = L_{S2}$ = 10 nh
$L_{SSl} + L_{SS2}$ = 9.1 nh
V_{SS} = 50V
I_L = 385A

Initially, the 385A load is circulating in the freewheel diode. At t = 0, V_{DR} is stepped from zero to 11V, remains at this value for 700 nsec and then is reset to zero volt. The resulting current distribution and switching energy are illustrated in Figure 3. For this example, the peak current in #1 HEXFET Power MOSFET is 61A or 75% greater than the balance current of 35A. The transition energy dissipated in #l is more than 100% greater due to unbalance. This example illustrates several important factors. First, even though the 61A peak current represents a large unbalance current in #1 HEXFET Power MOSFET, it is still within the device SOA which allows a 70A peak current. Secondly, it is the differential current established during turn-on that sets the initial unbalance for the constant current portion of the pulse. Unbalance losses due to turn-on differentials will be significant in applications where conduction losses dominate the thermal design (e.g. high duty cycle pulses). Thirdly, the current differentials established during turn-off generates energy differentials that will be significant in high frequency applications where switching or transition losses dominate the thermal design. Note also that for threshold voltage or gain mismatch, the differential current development during turn-off is a continuation of the process generating the differential during turn-on. Generally, maximum differentials are established in the active region.

The extensive list of interacting unbalance generators given above illustrates that the evaluation of the effects may be a complex task. To clarify the response of parallel MOSFETs to ON resistance, gain, and threshold voltage mismatch, unbalance limit functions are derived. Although the following analyses concentrate on MOSFET generated unbalance, other parameters must be included. The Q-locus mapping technique simplifies the quantification of current and transition energy unbalance by identifying key parameter products and ratios.

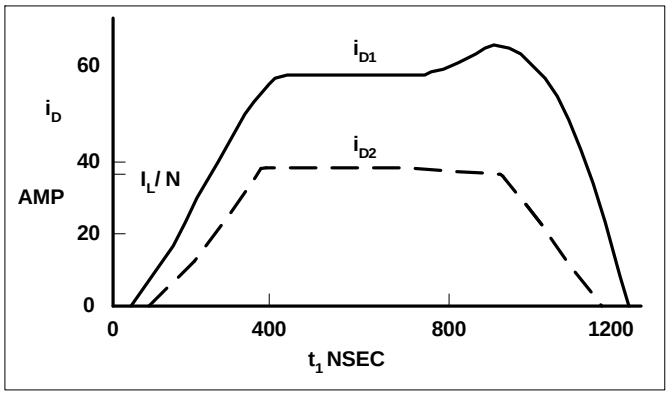


Figure 3(a) : Drain Current Unbalance

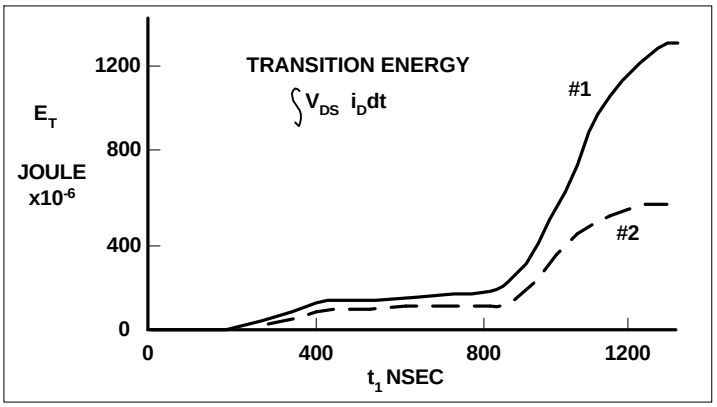


Figure 3(b): Transition Energy Unbalance

Figure 3: Unbalance Effects Due to Threshold Voltage and Gain Factor Mismatch

II. SUMMARY OF RESULTS

The primary results reported in this paper are summarized as follows:

(1) Unlike other switches parallel MOSFET current unbalance is inherently limited over wide operating ranges - for both steady-state and dynamic operations, 'runaway' conditions do not occur.
(2) These limits, however, can lead to excessive junction temperature or operation outside the SOA depending on specific power circuit and gate driver parameters.

(3) The designer has several 'open loop' options that will reduce unbalance to acceptable levels without introducing complex or expensive hardware.
(4) It is possible to limit pulse turn-on current unbalance to approximately 15% for certain applications without any device screening through appropriate design of the gate driver.
(5) Switching transition energy ratios for wide ranges of unbalance are shown to typically be in the range 1.5 to 2.5 - the importance of energy unbalance depends on application factors such as duty cycle, frequency and cooling system type.

Starting from the unbalance limits for given parameter mismatch(es), it is shown that if these limits are unacceptable for a given application, the dynamic unbalance can be reduced to acceptable levels by one or more of the following:

- restrict the dynamic load line to certain areas of the switching plane - by controlling the $I_G \bullet L_X$ product and/or the L_S / L_X ratio;
- use of a three parameter screening test with a 90% yield.

Basically, MOSFET current and switching energy unbalance can be restricted to levels whereby the use of current sharing resistors, balancing transformers and/or active power circuit feedback is avoided.

Table 1 lists all of the causes and effects of unbalance evaluated on this paper. Current differentials are monitored for SOA. Losses are monitored for junction temperature (T_J) constraints. It is assumed that the gate-source voltages of the parallel MOSFETs are identical except for a minor degree of decoupling for control of parasitic oscillations. Some of the results are as expected from other switch technologies - a few of the results are new and unique to MOSFETs. A brief explanation follows.

- Differential $R_{DS\,(on)}$ will cause current unbalance and extra conduction losses as expected, but these are limited due to the positive temperature coefficient for MOSFET resistance. The thermal 'runaway' characteristic of other semiconductor technologies does not apply to MOSFETs.
- Gain factor differentials (ΔGF) result in limited current unbalance. In the extreme, which is difficult to realize in practice, the current unbalance is limited to the gain ratio. Since turn-on differentials are very easy to control, the predominate loss differential occurs during turn-off.
- V_T also results in limited current unbalance. Before the device with the lowest threshold voltage can conduct an excess current, its gate voltage must be increased above the higher threshold voltages of the other devices - thereby limiting the maximum current conducted by the lowest threshold voltage device. Note that MOSFETs do not turn fully ON at threshold. Additional gate voltage or charge must be provided if the drain current is to be increased. This characteristic is unique to MOSFETs in comparison with other contemporary power switch technology.
- Differential gate-to-source capacitances (ΔC_{GS}) do not cause current unbalance since drain currents are controlled by the gate-to-source voltage potentials. By directly connecting all gates and sources together, a common potential is ensured. This result remains valid with a limited degree of gate decoupling resistance and common source inductance present. Typical turn-on times are sufficiently short to preclude ΔC_{GS} from generating current unbalance.

Primary Unbalance Result		
Unbalance Generator	**Current Differential**	**Energy (Loss) Differential**
Device:		
- $\Delta R_{DS\,(on)}$	steady-state & Limited	conduction
- ΔGF	dynamic & limited	turn-off
- ΔV_T	dynamic & limited	turn-off
- ΔC_{GS}	none	none
- ΔC_{GD}	none	none
Power Circuit:		
- ΔL_D	none	turn-on
- ΔL_S	dynamic	turn-on & turn-off
Gate Driver:		
- ΔR_G	dynamic	turn-on & turn-off

Table 2: Primary Effect of Unbalance Generator on MOSFET Current Level and Dissipated Energy

- Differential Miller capacitances (ΔC_{GD}) will affect the time required for the drain-to-source voltage (V_{DS}) to collapse. However, the first device to reduce V_{DS} also reduces the forward bias across other parallel devices causing them to turn-on earlier. Consequently if the gates are not strongly decoupled, no significant current unbalance develops.
- In the power circuit external to each device, differential branch inductance (L_D), which excludes source inductance common to both power ant gate driver circuits (L_S), normally does not cause current unbalance. In comparison with other technologies, this result is unusual and advantageous. Drain current is controlled by gate voltage during transitions. However, ΔL_D will cause differential drain-to-source voltages during transition ant therefore differential transition energy.
- L_S through feedback effects will cause differential currents and transition energies. As is shown in the paper, common source inductance is a critical parameter in higher frequency applications and must be given careful attention. However, worst case current differentials increase as the number of parallel devices increase - and for these designs, the presence of any $L_S > 0$ tends to reduce current unbalance due to other causes.
- Differential decoupling resistance in the gate driver will cause both current and transition energy unbalance if the gates are strongly decoupled ($R_{GC} \rightarrow 0$)

III. QUANTIFYING UNBALANCE

In this section the magnitudes of unbalance generators are reviewed. Techniques for rapidly estimating the maximum resulting current unbalance possible are presented. These techniques are also useful for setting screening levels. The realization of these limits depends on which dynamic load lines are utilized for turn-on and for turn-off. Techniques for estimating the magnitude of dynamic unbalance are included.

III (a) Parameter Variation Ranges

Paralleling unbalance is caused by differences between the MOSFET, power circuit components and layout and gate driver for each parallel branch.

(i) For International Rectifier's HEXFET Power MOSFET devices, parameter ranges are given in the data sheet for each part number. These ranges tend to be extreme and are not generally realized in practice. Table 3 lists these extremes for $R_{DS\ (on)}$, $GF_{(gfs)}$ and V_T of the largest (HEX 5) and second largest (HEX 3) chips mounted in TO-3 packages. The wide ranges tabulated indicate the possibility of significant parameter mismatch between paralleled devices that in turn would be expected to generate large unbalances.

It is well established that each production batch of these parameters. Most of the device parameters fall well within the data sheet extremes so that the odds are high that devices from one batch (or date code) will have relatively modest parameter variations. Parameter variations for 90% of the devices sampled from various production batches were constrained as listed on Table 3. This information is very useful in parallel circuit design, in terms of setting parameter mismatch extremes for computation of expected levels of unbalance or for determining degree of compensation (if required). Alternatively, it provides a guide to the minimum yield one would expect from screening tests.

However, without some screening of devices placed in parallel, the data sheet extremes will occasionally be realized and as will be shown, circuit design has to contend with or control the resulting unbalances. This trade-off between screening and circuit design is discussed further in Section IV.

(ii) The primary contributors to unbalance in the power circuit are differential drain or branch inductance (L_D) and common source inductance (L_S). These inductances are developed by interconnection wiring and possibly discrete components. Thus the variation between branches is a function of layout symmetry (including nearby magnetics) and production tolerances. Experience indicates variations of 10 - 20% are common [8, 9].

To be certain that most cases are covered, the following analysis spans 50% differentials in these inductances.

(iii) For the gate driver, if a common voltage source is used, the primary factor contributing to unbalance is mismatch between decoupling resistors if they are used. Since ±20% resistors are common, the analysis includes a differential of 50%.

III (b) Current Unbalance Limits

Unlike other switching devices such as thyristors, switchgear or power bipolar transistors, parallel MOSFET generated current unbalance has inherent limits provided the gate-to-source voltages are the same. Limit functions are derived for ON resistance, gain and threshold voltage mismatch. Gate-source and Miller capacitance mismatches have negligible effect. The function for ON resistance includes the effect of junction temperature changes.

III (b) (i) Steady-State Limits

When parallel MOSFETs are switched ON and V_{GS} for each device reaches its final (identical) value, current unbalance caused by the MOSFETs will be due to mismatch in $R_{DS\ (on)}$. A 'worst case' analysis of this current unbalance is given in Appendix A. Referring to Figure 1, branch #1 has the minimum $R_{DS\ (on)}$ and the other N-1 devices have an identical, larger value of $R_{DS\ (on)}$. Thus current unbalance is a maximum in branch #1 for a given mismatch in $R_{DS\ (on)}$.

For a large number of devices in parallel, equation 3 (refer equation A11) gives a simple quadratic for the maximum unbalance current (I_{D1}) expressed as a fraction of the balance current (I_B) that would otherwise flow for no parameter mismatch.

$$\left(\frac{I_{D1}}{I_B}\right)^2 - \left(1 - \frac{1}{\Delta T_{2JA} \bullet K}\right)\left(\frac{I_{D1}}{I_B}\right) - \left(\Delta T_{2JA} \bullet K \bullet \frac{R_{1-25}}{R_{2-25}}\right)^{-1} = 0 \qquad (3)$$

Where K = temperature coefficient for MOSFET resistance (for HEXFET Power MOSFETs, 0.6 < K < 1.2% per °C for 100 to 500 volt ratings respectively)

$R_{i\text{-}25} = R_{DS\ (on)}$ of the i^{th} branch device at 25°C (i.e. nominal) for the steady-state gate voltage selected

ΔT_{2JA} = design junction-to-ambient temperature rise for the nominal resistance
$= R_{i\text{-}25}\ I_B^2 T_{PN\theta JA}$ (refer equation A12)

T_{PN} = nomalized pulse duty cycle

θ_{JA} = junction-ambient thermal resistance

Source	Parameter Range		
	Threshold Voltage, V_T	**Transconductance or Gain Factor g_{fs}, GF**	**ON Ressitance $R_{DS\ (on)}$**
Data Sheet	2 - 4 V	60 - 140%	70 - 130%
Extremes min/max Δ =	2 V	80%	60%
Maximum Differential (Spanning Mean) for approximately 90% of production batch	0.7 V	20%	35%

Table 3: HEXFET Power MOSFET Maximum Parameter Ranges From (1) Data Sheet, (2) Single Production Batch/Date Code Screening With 90% Typical Yield.

Figure 4 illustrates the variation in current unbalance with $N \rightarrow \infty$ as a function of the nominal resistance ratio for two extreme conditions:

(a) $\Delta A_{2JA} = 0$ which represents either neglecting the effect of temperature compensation or ensuring equal junction temperature;
(b) $\Delta A_{2JA} \bullet K = 0.336$ which is representative of the rated junction temperature resistance increase from nominal for 55°C ambient. (from A3 and Al2, $0.3 < \Delta A_{2JA} \bullet K < 0.41$ for 100 to 500 volt ratings resp.)

A substantial reduction in current unbalance is predicted when temperature effects are considered for a large number of devices in parallel.

For reduced numbers of parallel devices ($N < \infty$), current unbalance is given by a cubic equation (refer to (A10)). The variation in unbalance current for 5 and 2 paralleled devices is illustrated in Figure 4. It is interesting to note that temperature compensation has a reduced effect as N is reduced. For N-l large, a decrease in branch #1 current (ΔI_{D1}) due to temperature increase causes a minor increase in the temperature of the devices for which $\Delta I_{D2} = \Delta I_{D1}/(N\text{-}l)$. With 2 parallel devices, the current increase in the second device is fully equal to the decrease in the first branch which causes a relatively large increase in branch #2 device temperature. This increase inhibits current reduction due to temperature compensation. However, for a given mismatch, temperature compensation is most effective where it is most needed - with a large number of parallel devices.

Table 4 identifies 'worst case' current unbalance for the two sets of parameter mismatch extremes given in Table 3. For two devices from the same date code, the predicted 18% maximum unbalance is reduced to 14% allowing for temperature compensation. For N large and without screening, temperature compensation reduces the predicted maximum unbalance from 85% to 56%. Note that these reductions assume a common ambient temperature. If a common heatsink is used, the reductions will not be as large (refer to condition (b) above). For simplified heatsink design, see reference 10.

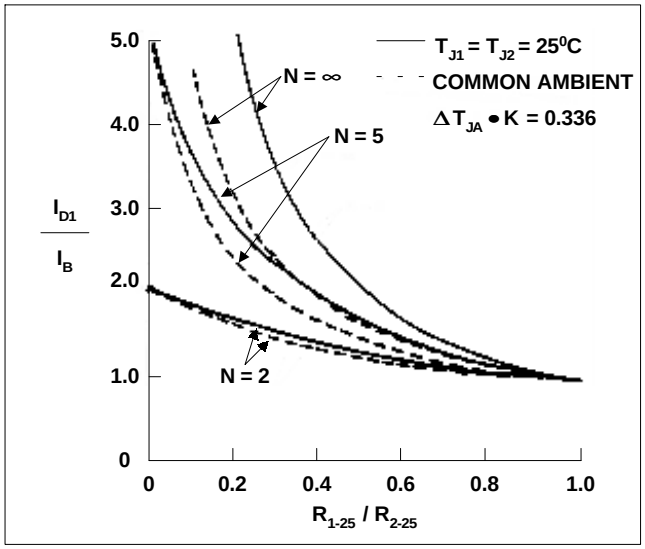


Figure 4: Worst Case Current Unbalance Ratio For #1 Branch (ID1 / IB) Vs. Nominal ON Resistance Mismatch Ratio Between #1 Branch and #2 Branch (R1-25 / R2-25) for N Parallel Devices With: (1) Common Junction Temperature; (2) Temperature Compensation From Common Ambient

N	Data Sheet $R_{DS\ (on)}$ Extrremes (D = 60%)		Production Batch /Date Code $R_{DS\ (on)}$ Extremes (D = 35%)	
	T_J Equal	T_J Compensated	T_J Equal	T_J Compensated
Large	1.85	1.56	1.43	1.30
5	1.59	1.43	1.32	1.23
2	1.30	1.27	1.18	1.14

Table 4: Maximum Current Unbalance (I_1/I_B) Due to $R_{DS\ (on)}$ Mismatch For Various Numbers of Paralleled Devices (N), With and Without Junction Temperature (T_J) Compensation

III (b) (ii) Dynamic Limits

There are upper limits to the magnitude of current unbalance caused by threshold voltage or gain mismatch These limits could be realized by relatively slow transition times and occur at the boundary of the active/ohmic regions.

It is instructive to consider an illustration of these limits for the example of a large number of devices in parallel. From Appendix B, an expression for the worst case unbalance current in branch # 1 is given by (refer equation B10):

$$\frac{I_{D1}}{GF_1} = \left[\Delta V_T + \sqrt{\frac{I_B}{GF_2}} \right]^2 \qquad (4)$$

A convenient normalizing factor that will allow this expression to represent any device is I_{DM}/GF where I_{DM} is the rated pulse current and GF is the absolute gain from equation (1). The normalized expression is (refer equation B14):

$$\frac{I_{D1N}}{GF_{1N}} = \left[\Delta V_{TN} + \sqrt{\frac{I_{BN}}{GF_{2N}}} \right]^2 \qquad (5)$$

Table 5 lists the relevant parameters and normalizing factors for all of the International Rectifier HEX-5 and HEX-3 TO-3 packaged devices. Figure 5 illustrates the variation of I_{DlN} over the parameter ranges given in the table.

This figure is immediately useful for:

(1) rapidly estimating the potential unbalance resulting from a given mismatch;
(2) determining screening levels for threshold voltage.

PART NO.	I_{DM} A	GF A/V^2 (25^0C)	V_T V (25^0C)	I_{DM}/GF	$\sqrt{I_{DM} / GF}$	DV_{TN} max.	GF_{1N} max.	GF_{2N} min.	GF_1 / GF_2 max.
Series									
IRF150, 1	70	1.75	3.00	40.0	6.32	0.316	1.4	0.6	2.33
152, 3	60			34.3	5.86	0.341			
IRF250, 1	60	3.40	3.10	17.65	4.20	0.476	1.33	0.67	2.0
252, 3	50			14.71	3.83	0.522			
IRF350, 1	25	2.63	3.00	9.51	3.08	0.650	1.44	0.56	2.6
352, 3	20			7.60	2.76	0.725			
IRF450, 1	25	5.5	3.40	4.55	2.13	0.940	1.4	0.6	2.33
452, 3	20			3.64	1.91	1.05			
IRF130, 1	30	1.00	2.90	30.0	5.48	0.365	1.4	0.6	2.33
132, 3	25			25.0	5.00	0.40			
IRF230, 1	15	1.45	3.30	10.34	3.22	0.621	1.44	0.56	2.6
232, 3	12			8.28	2.88	0.695			
IRF330, 1	8	1.45	3.25	5.52	2.35	0.852	1.43	0.57	2.5
332, 3	7			4.83	2.20	0.910			
IRF430, 1	7	1.25	3.25	5.60	2.37	0.845	1.4	0.60	2.33
432, 3	6			4.80	2.19	0.914			
IRF9130, 1	-30	-0.55	-3.00	54.5	7.38	0.407	1.43	0.57	2.5
9132, 3	-25			45.5	6.74	0.445			

Table 5: Gain Factor Constant (GF), Maximum Gain Factor Ratio (GF_1/GF_2) and Normalized Threshold Voltage (ΔV_{TN}) ant Gain Factor Ranges (GF_{1N}, GF_{2N}) For International Rectifier HEX-5 and HEX-3 TO-3 Packaged Devices

For example, consider the maximum unbalance that could occur from one IRF150 device turning on early due to the lowest V_T (2V) and a remaining large number of devices turning on at the typical V_T (3V). Here ΔV_{TN} = (3-2)/6.32 = 0.158. From Figure 5 the maximum unbalance for $GF_{1N} = GF_{2N} = 1.0$ occurs at maximum I_{BN} (1.0) and is equal to approximately 35% (I_{D1N} = 1.35).

Maximum current unbalance resulting solely from gain mismatch (i.e., $\Delta V_{TN} = 0$) is simply the gain ratio ($I_{D1N} = GF_{1N} \bullet I_B/GF_{2N}$ from Figure 5) with a large number of devices. With one device assigned the highest gain (+40%) and all others assigned the typical value (1.0), then the maximum current unbalance is simply 1.4 or 40%.

Consider the screening levels for threshold voltage and gain of the IRF150 where the maximum potential current unbalance is limited to 20% (with a balance current $I_{BN} = 0.75$). The nominal value for I_{D1N} is 0.9. For the gain range allowed by the data sheet, ±40%, the limits for I_{D1N}/GF_{1N} are 1.5 and 0.64. Similarly, I_{BN}/GF_{2N} limits are 1.25 and 0.54. Other limits, due to threshold voltage are given by the $V_{TN} = 0$ and $V_{TN} = 0.318$ loci.

The above limits define a solution region as shown in Figure 5 (shaded region) for a maximum 20% current unbalance potential with a large number of parallel devices. Any combination of screening levels for gain and threshold values that locates a point in the solution region will not cause unbalance in excess of 20%.

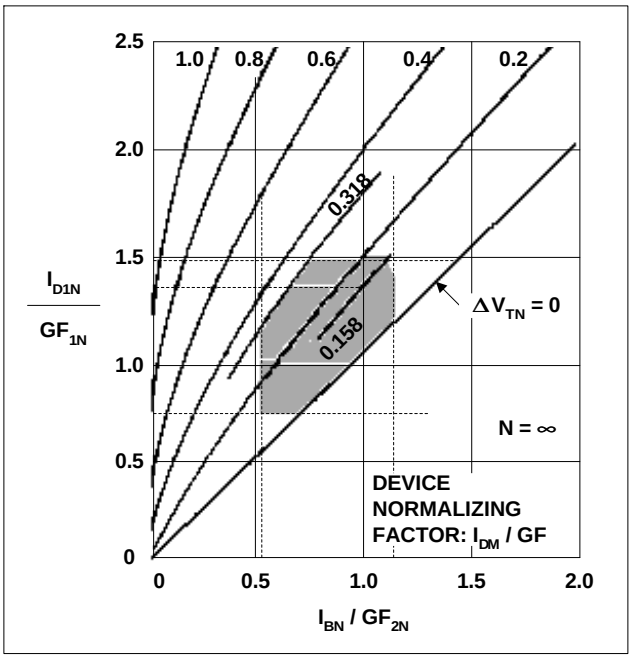


Figure 5: Normalized Worst Case #1 Branch Drain Current (I_{D1N}) Vs. Balance Current (I_{BN}) For Various Gain Factor Mismatches (GF_{1N}, GF_{2N}) and Threshold Voltage Differentials (ΔV_{TN}) Between #1 and #2 Branches (Figure 1) With a Large Number of Parallel Devices.

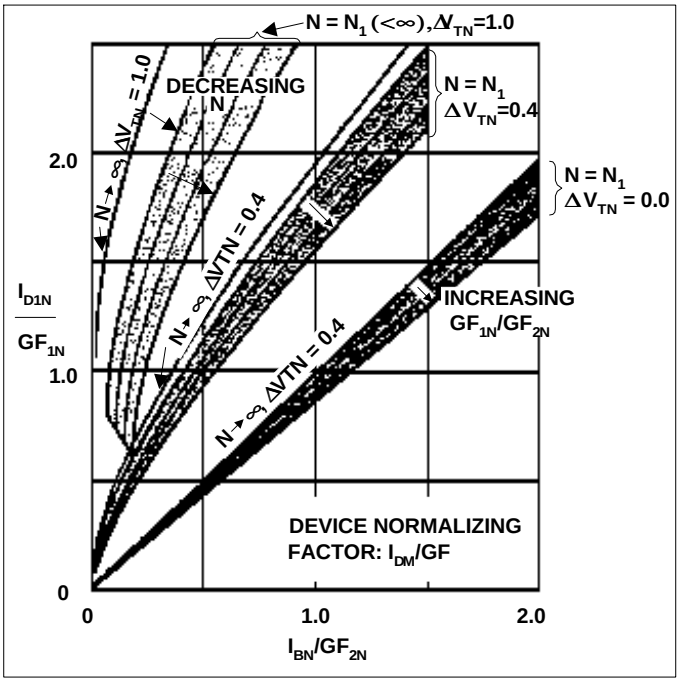


Figure 6: Illustration of the Reduction in Unbalance Current (I_{D1N}) for a Finite Number of Parallel Devices

For a smaller number of devices ($N < \infty$), screening levels can be opened up for a given performance criterion. The potential unbalance magnitude decreases with the number of parallel devices. A somewhat more complex expression describes the unbalance current for $N < \infty$ (refer equation Bl5). Figure 6 shows that the effect of reducing the number of parallel devices is generally to reduce I_{D1N} for a given set of parameter mismatches. Each locus for V_{TN} in Figure 5 breaks into a new family of loci for $N < \infty$ that are generated by the gain ratio, GF_{1N}/GF_{2N}.

Table 6 lists the variation in maximum current unbalance limits as the number of paralleled devices is decreased. The variation in limit magnitude is slightly more than two-to-one for $2 \leq N < \infty$.

N	Unbalance Cause		
	ΔV_{TN} = 0.158	GF_{1N} / GF_{2N} = 1.4	ΔV_{TN} & ΔGF
Large	35%	40%	89%
5	28%	30%	62%
2	16%	18%	36%

Table 6: 'Static' Limits For Dynamic Current Unbalance, $(I_{D1} - I_B)/ I_B$ %, Vs. Number of Parallel Devices for Threshold Voltage and Gain Mismatch Parameters: #1 Branch - Data Sheet Extremes; 82 Branch - Typical. (I_{BN} = 1.0)

Although the effects of junction temperature on dynamic balance have not been rigorously analyzed, trends may be inferred from Figure 2(b). As temperature increases, V_T decreases (-6 mV per °C) and GF decreases. This results in two trends. For the initial pulse current, the hotter device has a higher drain current for a particular V_{GS}, but as the pulse develops, this device will have a lower drain current (particularly for lower voltage rating devices). The effects of temperature on dynamic balance may compensate each other.

III (c) Realizable Dynamic Unbalance

Limits have been identified for MOSFET generated current unbalance. Whether or not these limits are realized depends on the dynamic load lines for turn-on and turn-off selected by the designer.

In the first part of this section, dynamic current unbalance and transition energy differentials are mapped for two general series using worst case analysis for each:

Series #1: Analysis for eleven parallel devices for which a single device in branch #1 is assigned worst case adverse data sheet extremes. The other ten devices, equivalent to a large number selected over many production batches, are assumed identical and assigned typical parameter values.

Series #2: Analysis for two parallel devices in which each is assigned data sheet parameter extremes to maximize current unbalance in #1 branch. Single production batch/date code extremes are also evaluated.

In the second part, unbalance generators other than MOSFETs are reviewed.

The influence of specific dynamic load lines on current unbalance and transition energy differentials have been evaluated by computer simulations based on 4th order Runge-Kutta numerical techniques. To quantify the nature of the transitions from OFF-ON-OFF, the switching plane has been mapped using Q-loci (refer Appendix C) where the product of average translation gate current (I_G) and commutation inductance (L_X) uniquely determines a base dynamic load line in the switching plane. From Appendix C,

$$Q = I_G \bullet L_X \qquad (6)$$

The basic dynamic load line or Q-locus is deflected towards a higher transition energy or slower transition time as the ratio L_S / L_X is increased (refer Figures C2a and C3a in Appendix C). The switching transition energies dissipated by the device are also mapped by Q-loci for the IRF150 (refer Figures C2b and C3b).

Three Q loci, $4X10^{-9}$ (Q_0), $20X20^{-9}$(Q_1) and $100X10^{-9}$ 9 (Q_2) amp-henry, span a wide range in the switching plane for the IRF150 and are the basis for the following analysis. The switching transition each locus represents is characterized as follows:

Q_0: relatively slow transition or high switch energy dissipation, with low peak turn-off voltage.
Q_1: intermediate transition.
Q_2: relatively fast transition or low switch energy dissipation, with high peak turn-off voltage.

Series #1: Dynamic Unbalance For Eleven Parallel Devices

#1 HEXFET Power MOSFET drain current increase and transition energy for the parameter mismatches listed in Table 7 are illustrated as a function of Q and L_X in Figures 7 and 8.

A 40% mismatch in gain in Figure 7(a) results in a maximum increase in the #l HEXFET Power MOSFET current of 12.4A or 35%. This limit is the same as the static limit predicted by equation (Bl5) for eleven devices in parallel. The Q_0 locus realizes this limit. As Q is increased, the unbalance current decreases.

The ratios of transition energy dissipated for #1 HEXFET Power MOSFET compared with #2 are illustrated in Figure 7(b). They range between 1.2 and 1.5 except during turn-on for the Q_1 and Q_2 loci. The ratio becomes indeterminate as the energy values become very small. Even though the energy ratio is greater than unity throughout the switching plane, the absolute transition energy for #1 HEXFET Power MOSFET with the increased unbalance current decreases as Q is increased for both ON and OFF transitions.

The results of a two-thirds threshold mismatch are illustrated in Figures 7(a) and 7(b). The maximum drain current increase is 44% and occurs for the Q_0 locus. For switching loci with higher values of Q, the dynamic current unbalance is reduced as illustrated. The transition energy ratios range between 1.2 and 1.7. Loci with higher values of Q have lower transition energy.

Dynamic current unbalance for the simultaneous mismatch of both gain and threshold voltage are illustrated in Figure 8(a). The peak increase in #1 HEXFET Power MOSFET current is 32.6 A or 93% above the matched parameter value.

This value is equal to that derived from the product of the current ratios for the individual mismatches. Transition energies are illustrated in Figure 8(b).

The ratios are higher, ranging between 1.5 and 2.5. Higher valued Q loci are associated with lower turn-on and turn-off transition energies.

Series #2: Dynamic Unbalance For Two Parallel Devices

In each of the following analyses, the clamped inductive load is 70 A giving each device a balance current of 35 A. The switch comprised of two IRFl50's is considered ON when the total switch current is equal to 70 A, each device is in the ohmic region and has a gate-to-source voltage of at least 10 V.

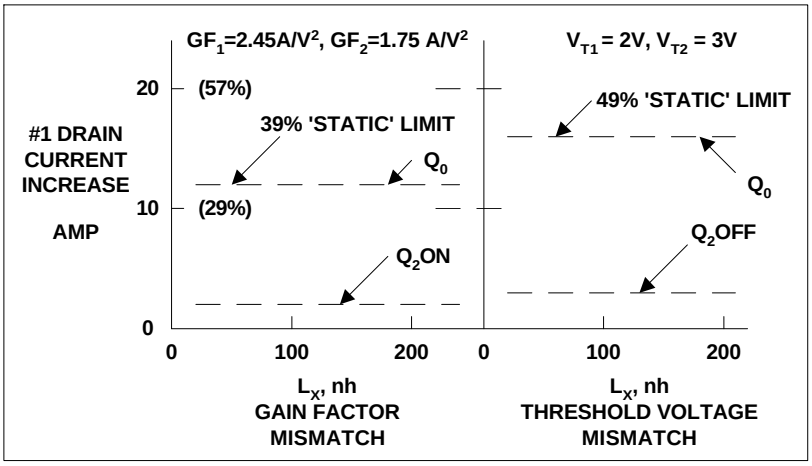


Figure 7(a): #1 IRF150 Drain Current Increase Range Above Balance Current (I_B = 35 A) For $Q_0 \leq Q \leq Q_2$

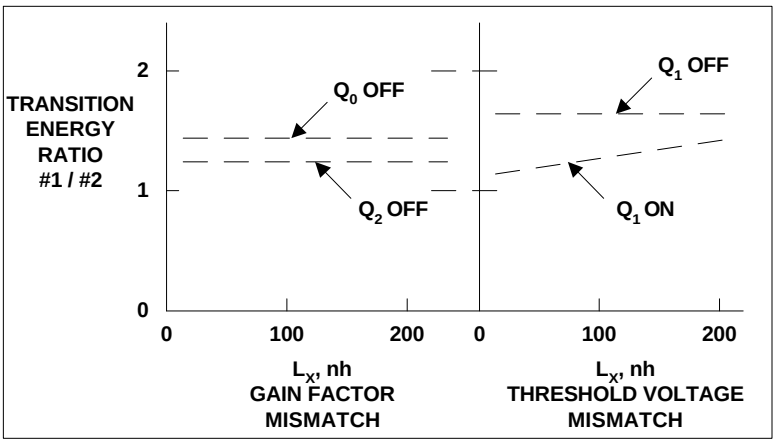


Figure 7(b): Transition Energy Ratio Band For $Q_0 \leq Q \leq Q_2$

Nominal values for V_{SS}, L_X and L_D are 50V, 200nh and 100nh, respectively. Two sets of four general cases are analyzed. For each set, two values of L_S/L_X are used: L_S = 20nh, L_S/L_X = 10%, a value that could be appropriate for the TO-3 package with a common lead to the source pin; L_S = lnh, L_S/L_X = 0.5%, a minimum value that could be associated with dual source connections to the MOSFET chip. For each L_S/L_X, two basic dynamic load lines are analyzed (Q_1 and Q_2 loci, refer Appendix C).

Figure 7(a) & 7(b): HEXFET Power MOSFET IRF150 Current and Transition Energy Unbalance Vs. Dynamic Load Line (Q Locus) and Commutation Inductance (L_X) for (1) Gain Factor Mismatch, (2) Threshold Voltage Mismatch. (N = 11, I_B = 0.5 I_{DM}, $L_S/L_X \leq 5\%$)

	BRANCH #1	BRANCH #2	V_{SS} = 50 V I_L = 385 A V_{DR} =11 V C_{GS} = 2,650 µfd C_{GD} = 350 µfd L_X RANGE = 20-200 nh Q RANGE = 4-100 x 10 - 9 A-h
N	1	10	
V_T	2	3V	
G_F	2.45	1.75A/V^2	

Table 7: Parameters For Worst Case Dynamic Current Unbalance Study With N = 11.

III (c) (i) Effect of Decoupling Resistance (R_G)

There is a preferred level of gate decoupling that eliminates parasitic oscillations without significantly increasing unbalance due to parameter mismatch. With no gate decoupling (R_G = 0, Figure l), high frequency current oscillations (20-100MHz) are predicted through the Miller capacitance. To avoid oscillations, analysis indicates R_G/N should be greater than 5% of the total driver resistance.

An upper limit for R_G/N is given by unbalance considerations. In comparing current unbalance due to threshold voltage and/or gain mismatch, no changes are noted between R_G/N equal to 0% or 100%.

For device capacitance mismatch, significant current unbalance occurs for R_G/N = 100% (refer Table 8). With R_G/N = 0%, no unbalance occurs for either gate-source or Miller capacitance unbalance.

Therefore, it is recommended that R_G/N be set at approximately 10% of the total driver resistance. Unless otherwise noted, this value is used for the remaining analysis in the paper.

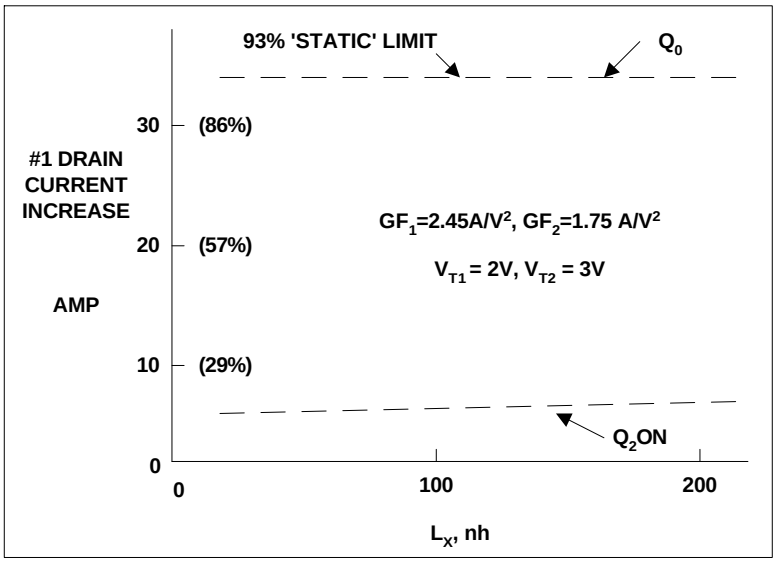


Figure 8(a): #1 IRF150 Drain Current Increase Range Above Balance Current (I_B = 35 A) For $Q_0 \le Q \le Q_2$

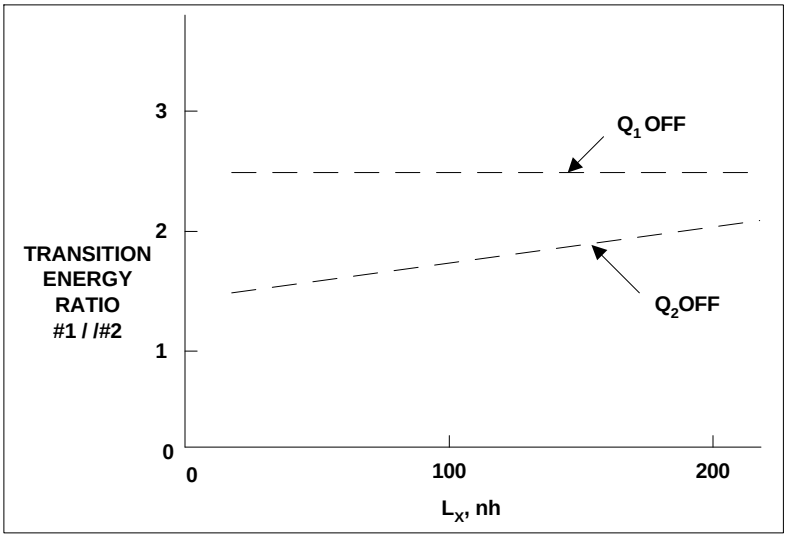


Figure 8(b): Transition Energy Ratio Band For $Q_0 \le Q \le Q_2$

Figure 8(a) & 8(b): HEXFET Power MOSFET IRF150 Current and Transition Energy Unbalance Vs. Dynamic Load Line (Q Locus) and Commutation Inductance (L_X) For Combined Gain Factor and Threshold Voltage Mismatch (N = 11, I_B = 0.5 I_{DM}, $L_S/L_X \le 5\%$).

	Q_1		Q_2	
L_S / L_X	ΔC_{GS}	ΔC_{GD}	ΔC_{GS}	ΔC_{GD}
10%	8.1A (23%)	9.6A 927%)	3.1A (9%)	2.7A (8%)
0.5%	14.2 (41%)	17.1 (49%)	2.8 (8%)	7.3 (21%)

Table 8: Current Unbalance, I_{D1} - I_B, Due to Device Capacitance Mismatch (Refer Table 9) With Completely Decoupled Gates. (N = 2, I_B = 0.5 I_{DM}, R_G/N = 100%)

III (c) (ii) MOSFET Generated Unbalance

In this next set of analysis, the dynamic current and transition energy unbalances due to extreme data sheet parameter variation are examined (refer Table 3). The analysis is based on the worst case of simultaneous extreme for V_T, GF, C_{GS} and C_{GD} variations for the IRF150 (refer Table 9). Because this combination is rare, the analysis is restricted to two parallel devices.

Device	V_T (V)	GF (A/V^2)	C_{GS} (pf)	C_{GD} (pf)
#1	2.0	2.45	1500.	200.
#2	4.0	1.05	3800.	500.

Table 9: IRF150 Parameter Extremes From Data Sheet

Current (ΔI) ant transition energy (E_T) unbalance resulting from these simultaneous mismatches are listed in the first two rows of Table 10. The maximum differential current occurs for minimum L_S/L_X ant for the minimum value of Q (Q_1). At 76%, this is slightly greater than the 'static' limit and is attributed to gate voltage decoupling caused by R_G/N equal to 10%.

Minimum current unbalance (18%) during turn-on occurs for minimum L_S/L_X and maximum Q (Q_2). The low value for L_S/L_X causes a relatively high unbalance (67%) during turn-off. Figure 9(a) illustrates the drain current for each device. If $R_{DS(on)}$ is matched, the differential current established during turn-on will decay as indicated by the dashed lines at a rate determined by the parallel loop L/R time constant.

During turn-off, the peak drain-source voltage would reach 217V. Figure 9(b) illustrates the turn-off with the voltage clamped at 100V.

The switching energy unbalance covers a wide range for these cases. The maximum ratio (8:1) occurs with an intermediate level of current unbalance (59%).

The next set of analysis is based on the simultaneous mismatch extremes for threshold voltage and gain to be expected from a single production batch (refer Table 3). Table 11 lists the production batch extremes (90% screening yields) for the IRF150 used in this analysis. Due to insufficient capacitance data, the data sheet extremes of Table 9 are used - the resulting current unbalance is minimal due to the weak degree of gate decoupling.

Unbalance Generator	L_S / L_X	'Static' Limit	Turn-On ΔI, A		Turn-On E_T, μJ		Turn-Off ΔI, A		Turn-Off E_T, μJ	
			Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
Data Sheet Extremes (Table 3)	10%	25.9A (74%)	20.1 (57%)	11.3 (32%)	230/120	21/47	20.8 (59%)	13.3 (38%)	1200/150	610/130
	0.5%	25.9	26.6 (76%)	6.4 (18%)	81/22	4/4	26.6 (76%)	23.5 (67%)	960/130	490/100 (150/91, V_Z=100V
Single Production Batch Typical Extremes For 90% Yield (Table 3)	10%	8.4 (24%)	7.4 (21%)	4.2 (12%)	220/170	28/36	7.4 (12%)	4.2 (12%)	740/420	410/260
	0.5%	8.4	11.8 (34%)	4.0 (11%)	110/60	5/3	11.0 (31%)	4.0 (11%)	620/420	320/220

Table 10: Current Unbalance ($\Delta I = I_{D1} - I_B$) and HEXFET Power MOSFET Transition Energy Unbalance (E_T, #1/#2) Vs. L_S/L_X and Q for Two Sources of Parameter Mismatch (N = 2, I_B = 35A, R_G/N = 10%).

Results of this analysis are listed in the latter part of Table 10. Maximum current unbalance occurs as expected with minimum L_S/ L_X and Q. However, the current excess at 34% is greater than the 24% allowed by the static limit. This excess is due to the 10% gate decoupling. Without gate decoupling or without capacitance mismatch, current unbalance drops to 20%, within the 'static' limit. The percentage effect of 10% gate decoupling increases as the unbalance magnitude decreases.

Minimum current unbalance of 11% occurs for the Q_2 loci. Switching transition energy ratios are generally in the range of 1.5:1. These unbalance results are substantially lower than those computed for data sheet extremes.

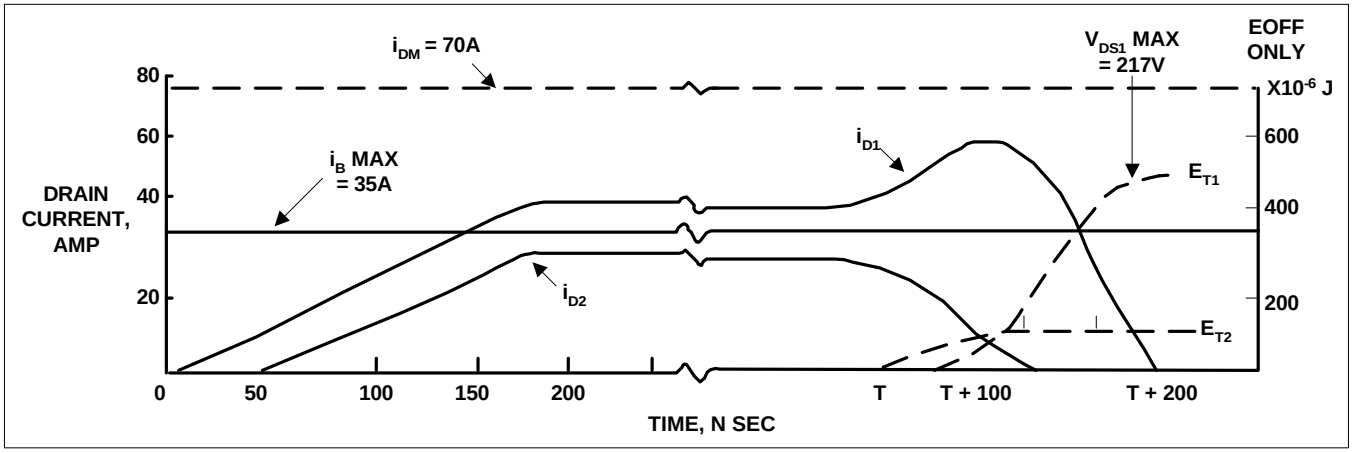
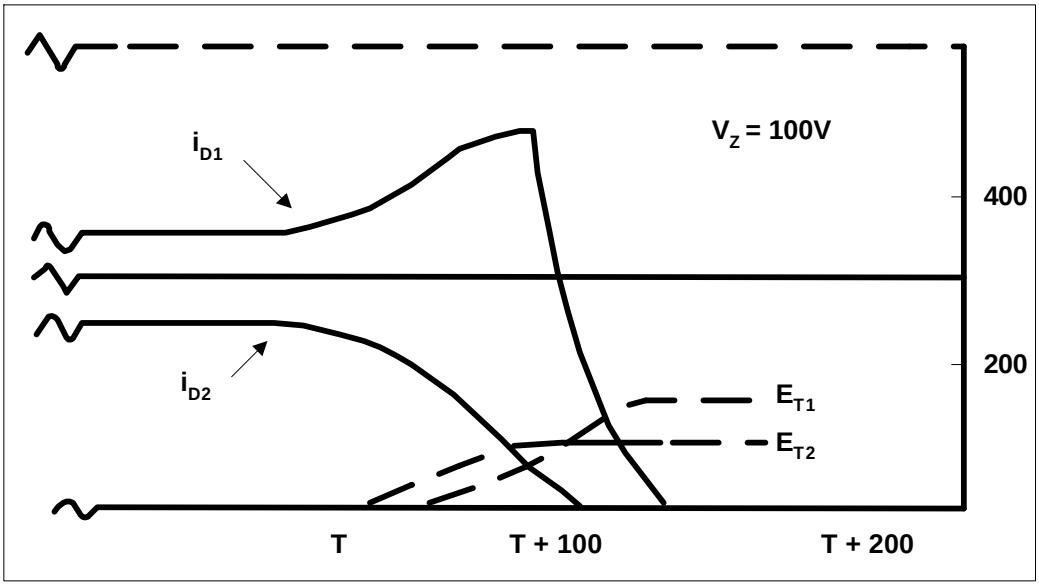


Figure 9(a): Unristricted Drain-Source Voltage (V_{DS}) During Turn-Off



(b) Drain-Source Voltage Clamped At Rated Value (V_Z = 100V)

III (c) (iii) Non-Device Parameter Differentials

$L_D \pm 25\%$: Mismatch between the drain inductance (L_D) of parallel branches does not cause current unbalance for L_S/L_X greater than 1% and Q less than Q_2. Unlike other switches, during turn-on and turn-off, drain current is controlled by gate-to-source voltage. It is not normally controlled by individual branch inductance.

Variations in L_D will affect the drain-source voltage and thus transition energy is unbalanced. Table 12 illustrates transition energy unbalance for N = 2. The differentials increase for large values of N. As L_S/L_X is decreased or, as Q is increased during turn-on, the unbalance increases but the absolute energy level decreases. During turn-off, the differentials are relatively unaffected by L_S/L_X or Q. For this example, L_D/L_X is 50% such that differential L_D is lost in the larger absolute turn-off energy.

Device	V_T	GF
	(V)	(A/V^2)
#1	2.65	1.93
#2	3.35	1.57

Table 11: IRF150 Parameter Extremes Expected From Single Production Batch/Date Code.

L_S / L_X	Transition Energy			
	ON		OFF	
	Q_1	Q_2	Q_1	Q_2
10%	210/180	51/19	540/580	320/340
0.5%	110/67	6/3	470/520	270/270

Table 12: Transition Energy Unbalance (#1 device/ #2 device, microjoules) Due to Drain Inductance Unbalance, $L_D \pm 25\%$: $L_{Dl} = 75\%$; $L_{D2} = 125\%$ ($N = 2$, $I_B = 35A$, $R_G/N = 10\%$)

$L_S \pm 25\%$: Mismatch in common source inductance results in both current and transition energy unbalance during turn-on as shown in Table 13.

For a nominal value of 10% for L_S/L_X, current unbalance is approximately 15% for N = 2 and 33% for N = 11. For L_S/L_X = 0.5%, the unbalance is negligible due to the low relative magnitude of source inductance.

The higher value for Q results in a slightly higher level of unbalance. This result is the opposite of that for all other sources of unbalance where increasing Q results in lower current unbalance. In this case, the cause of unbalance is amplified by increasing Q which offsets the reduced time in the active region.

N	LS / LX	Turn-On				Turn-Off	
		ΔI		E_T		E_T	
	Nominal	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
2	10%	5.0 (14%)	5.9 (17%)	220/170	24/31	540/580	360/300
	0.5%	0.8 (2%)	0.3 (1%)	88/85	4/4	490/500	270/280
11	10%	10.2 (29%)	12.5 (36%)	280/220	59/57	560/580	410/340
	0.5%	1.4 (4%)	0.5 (1%)	90/87	4/4	490/500	260/270

Table 13: Current (ΔI, amp) and Transition Energy (E_T, #1/#2, Microjoules) Unbalance Due to Common Source Inductance Unbalance, $L_S \pm 25\%$: $L_{S1} = 75\%$, $L_{S2} = 125\%$. ($N = 2$, $I_B = 35A$, $R_G/N = 10\%$)

Transition energy unbalance proportion is less than the original ± variation in L_S.
$R_G \pm 25\%$: To determine the maximum unbalance due to gate resistor mismatch, R_{GC} is set equal to zero. Table 14 shows the maximum current unbalance of 23% occurs for minimum L R_S and Q. For minimum L_S the turn-off transition energy variation approaches ± 25%.

The current unbalance results are comparable with those listed in Table 8 for gate-source capacitance mismatch of ±43%. For the Q_1 locus, the mismatch is not significant. For the Q_1 locus, the current unbalance due to capacitance mismatch is proportionately greater . For all of the non-device parameter mismatches, the effect of the adverse mismatch on device #1 during turn-on is to deflect the Q locus to the right in the switching plane (refer Figure C2a) which is a higher transition energy region for other factors remaining equal. During turn-off, the Q locus is also deflected to the right, but this results in lower transition energy. Consequently adverse current unbalance also increases peak drain-source voltage during turn-off.

LS / LX	Turn-On				Turn-Off	
	ΔI		E_T		E_T	
	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
10%	5.0 (15%)	3.1 (9%)	100/69	38/29	390/460	320/350
0.5%	8.2 (23%)	3.7 (11%)	23/15	5/4	290/470	220/350

Table 14: Current (ΔI, %) and Transition Energy (E_T , #1, #2, microjoules) Unbalance Due to De-Coupling, Resistance (R_{GC}=0) Unbalance, $R_G \pm 25\%$: $R_{G1} = 75\%$, $R_{G2} = 125\%$. ($N = 2$, $I_B = 35A$).

III (d) Summary

This completes the current and transition energy unbalance mapping for mismatch between parallel branch parameters. Two sets of HEXFET Power MOSFET parameter mismatch extremes from data sheet and single production batch (date code) sources are identified. Estimates are given for non-MOSFET parameter mismatch. The results are summarized as follows.

(i) Unbalance is limited for ON resistance, gain or threshold voltage mismatch.

- $N \rightarrow \infty$: $I_{D1}/I_B < R_2/R_1$ (steady-state)
  $< G_{F1}/G_{F2}$ (dynamic)
  $<$ 44% per volt for IRF150 AV_T (dynamic)
- $N < \infty$: Generally, the larger the unbalance for $N \rightarrow \infty$, the greater the unbalance reduction as N is reduced.

(ii) Significant reductions from the above limits are possible. Dynamic current unbalance realized from the above and from other causes is a function of the dynamic load line as described by a base Q locus ($Q = I_G \bullet L_X$) and a deflection dependent on the L_S/L_X ratio. Switching time and transition energy increases as L_X/I_G and/or L_S/L_X increase. Peak device voltage during turnoff increases as Q increases or as L_S/L_X decreases.

- Increasing Q reduces turn-on and turn-off current unbalance.
- For the higher Q values, decreasing L_S/L_X reduces turn-on unbalance and increases turn-off unbalance.
- For lower Q values, turn-on and turn-off current unbalance tend to be equal and both are reduced as L_S/L_X is increased.

(iii) With HEXFET Power MOSFET data sheet parameter mismatch extremes, turn-on current unbalance is limited to 15% for $Q = Q_2$ and $L_S/L_X = 0.5\%$.

(iv) With fully decoupled gates ($R_{GC} = 0$), current unbalance due to device capacitance mismatch is maximized. For weakly decoupled gates ($R_{GC}/N <$ 5% driver resistance, parasitic current oscillations occur in the Miller capacitance.

(v) Current unbalance sensitivity to threshold voltage mismatch increases as the device voltage rating increases.

(vi) Current unbalance due to ON resistance mismatch is reduced by allowing different junction temperatures. This reduction is maximized for a large number of devices.

(vii) With current unbalance present, the peak turn-off voltage increases as the L_D/L_X ratio is increased.

(viii) For N large, the transition energy increase ranges between 50 and 150%.

IV. GUIDELINES FOR CONTROLLING DYNAMIC UNBALANCE BETWEEN PARALLEL BRANCHES

Different techniques are available for controlling current unbalance. The most effective combination will consider:

(1) allowable level of unbalance - depends on the application
(2) options available for control.

There are wide ranges for both of these categories such that no single recommendation is generally useful. In this section, items (1) and (2) are reviewed to highlight the salient features of MOSFETs with respect to paralleling. Guidelines are developed for ensuring acceptable levels of unbalance.

IV (a) Application Factors

The optimum approach for a given user depends in part on the application. In particular, the transition-to-conduction energy ratio (E_T/E_C), the pulse duration-to-loop time constant ratio (T_P/τ) and the number of paralleled devices influences the technique chosen to control current balance.

Table 15 lists typical values of E_T/E_C for different pulse duty cycles and frequencies. It indicates that a high duty cycle, low repetition rate pulse could tolerate dynamic current balancing techniques that increased transition energy (within limits) since this would not initially increase the thermal loading on the cooling system. Conversely, low duty cycle, high repetition rate pulses would prefer current balancing techniques that maintained or reduced transition energy.

	Frequency	
Duty Cycle	**Low**	**High**
High	<<1	~1
Low	~1	>> 1

Table 15: Typical Transition (E_T) to Conduction (E_C) Energy Ratios (E_T/E_C) Vs. Pulse Characteristics

Current unbalance developed between parallel branches through the turn-on transition decays during the constant switch current interval at a rate determined by the time constant (τ) of the parallel loop. For pulse duty cycles in the range 50-100%, the balance current (I_B) is typically ≤ 50% of I_{DM}, the rated peak current (refer Figure 10(a)), due to rms current or thermal constraints. Therefore, for long pulses ($Tp >> \tau$), a relatively large dynamic current unbalance during turn-on case be tolerated due to the large SOA margin and to the relatively short duration of the excess current. Similarly, during turn-off, a relatively large current different is permissible.

With short duty cycle pulses, I_B may approach I_{DM} (refer Figure 10 (b)) thereby eliminating the excess SOA margin. For both turn-on and turn-off, margin for dynamic current unbalance is minimized.

For MOSFET parameter mismatch, the relative degree of resulting current unbalance is summarized in Table 16.

Two or three devices screened with 90% yield from a given production batch result in low current unbalance. Conversely, a large number of paralleled devices reflecting data sheet parameter extremes with only a few of these adversely mismatched could develop large unbalance currents - but the probability of the combination occurring is very low.

IV (b) Dynamic Balancing options

At least three approaches can be applied to improve dynamic unbalance (refer Table 17):

A - eliminate the cause by matching the parameters listed in I(c) (i), (ii) and (iii) above, i.e. realize a balanced system through screening;

B - modify the power circuit to compensate for or cancel the effect of the mismatch, i.e. minimize the magnitude of resulting unbalance;

C - modify the gate driver to offset the effects of parameter mismatch, i.e. minimize the duration of unbalance.

Techniques A & B have been previously reported. [1, 2, 8, 9]

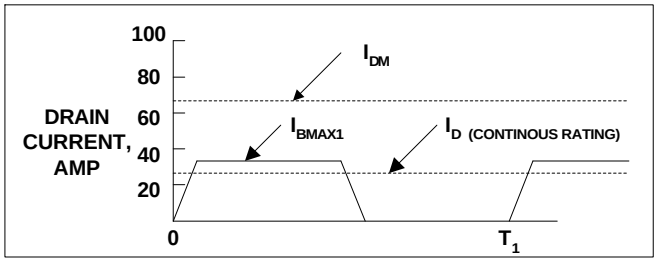


Figure 10a. Intermediate to High Duty Cycle Pulses Provide Large Peak Current Margin

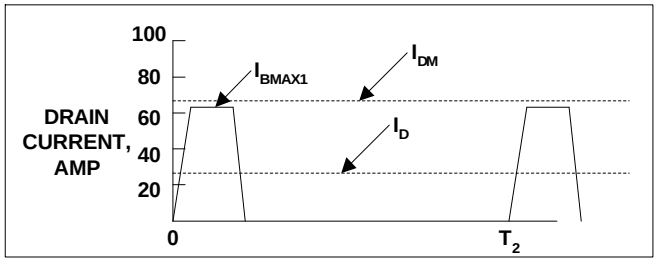


Figure 10b. Short Duty Cycle Pulses May Leave Small Peak Current Margin

Figure 10. Variation In IRF150 Peak Current Margin for Current Pulses of Equal RMS Drain Current

Device Unbalance Generator	Number of Parallel Devices	
	Low (<5)	High (>10)
Data Sheet Extremes	moderate	large (improbable)
Single Production Batch	low	moderate

Table 16: Relative Magnitude of Devices Generated Current Unbalance

IV (b) (i) Screening

From Section III(b) technique A derives screening limits for X given application based on permissible unbalance and the degree of parameter mismatch allowable for that unbalance. Various combinations are possible.

The mismatch limits set the screening levels and the next step is to evaluate each combination.

(A) Screen Parameters	(B) Modify Power Circuit
- GF (g_{fs})	- Current Balancing Transformers (L_D)
- V_T	- Active Feedback to Gate Driver
- C_{GS}	- L_S/L_X
- C_{GD}	
	(C) Modify Gate Driver
- L_D	
- L_S	- R_G
- R_G	- I_G

Table 17: Three General Approaches for Dynamic Current Balancing

The data of Table 10 shows that current unbalance can be reduced by more than a factor of two by using HEXFET Power MOSFETs from a single date code and setting the 90% yield screening limits of Table 3. With this technique current unbalance for two parallel devices ranges between 11 and 34% depending on how the MOSFETs are applied.

For the remaining parameters in Table 17, L_D ant L_S differentials can be minimized by ensuring symmetrical layouts (include nearby magnetic). For MOSFETs, ΔL_D affects only transition energy and is significant only for larger values of parallel devices. For unusually fast drivers ($Q > Q_2$), ΔL_D will affect current balance. R_G differentials are minimized by specifying close tolerance resistors. However if R_G/N is $\leq 10\%$ of the total driver resistance the effect of mismatched R_G will be minimal.

IV (b) (ii) Comparison of Techniques B and C

Technique B is may be implemented by adding current balancing transformers to the power circuit (SCR and Darlington circuits) or by adding current transformers and modifying the device driver to accept current feedback from the power circuit (power bipolar circuits). With MOSFETs, a third approach is effective. This utilizes source inductance as a simple method of reducing current unbalance. In the following, the characteristics of techniques B and C will be compared. For technique B, one method for reducing current unbalance is to introduce source inductance that is common to both the gate driver ant the train-source power circuit (L_S in Figure 1). Additional di/dt due to current hogging modifies the gate voltage of the unbalanced device in a direction to inhibit further unbalance. There are side effects to this approach, however.

Consider the effect of L_S on the Q loci in Figure C2(a) in Appendix C. The introduction of common inductance to the gate and power circuit results in increased drain-to-source voltage during turn-on and therefore a higher transition energy Figure C2b maps the increase in turn-on energy for increased values of L_S. Similarly during turn-off the addition of common source inductance in Figure C3b increases the transition energy dissipated by the device. However as shown in Figure C3a the peak drain-to-source voltage is reduced during turn-off. These results are consistent since the lower drain-to-source voltage means a longer time is required to commutate the current in the external power circuit inductance L_X. Therefore the greater amount of energy drawn from the supply during this increased time contributes to the increased device transition energy.

A primary reason for limiting current unbalance magnitude is to control the thermal load of each device. Technique (C) allows an alternate method for limiting excess thermal load due to current unbalance. In a given power circuit the total transition energy dissipated in each device can be reduced by increasing the Q value of the switching loci during turn-on and turn-off. This is accomplished by increasing the average gate current during the active region transition increase V_{DR} and/or reduce R_{GC}. Figures C2b and C3b show the substantial reductions possible in transition energy for a given power circuit design (i.e. given L_X). To maximize this energy reduction, L_S should be minimized. However during turn-off the combination of a high Q value ant low value for L_S may result in excessive drain-to-source voltage (Figure C3a). To remain within the SOA at lease two choices are available:

(1) relatively small increase in L_S with a corresponding increase in transition energy (on and off) that must be dissipated by the device;
(2) locate a diverter circuit that will limit the peak drain-to-source voltage and absorb more than the resulting increase in turn-off transition energy.

The diverter may be a zener diode or a diode-capacitor clamp with a resistor to return supply energy to the supply. The choice between techniques B and C for controlling the effects of current unbalance may be dictated by the frequency and/or loading the MOSFET switch operates at.

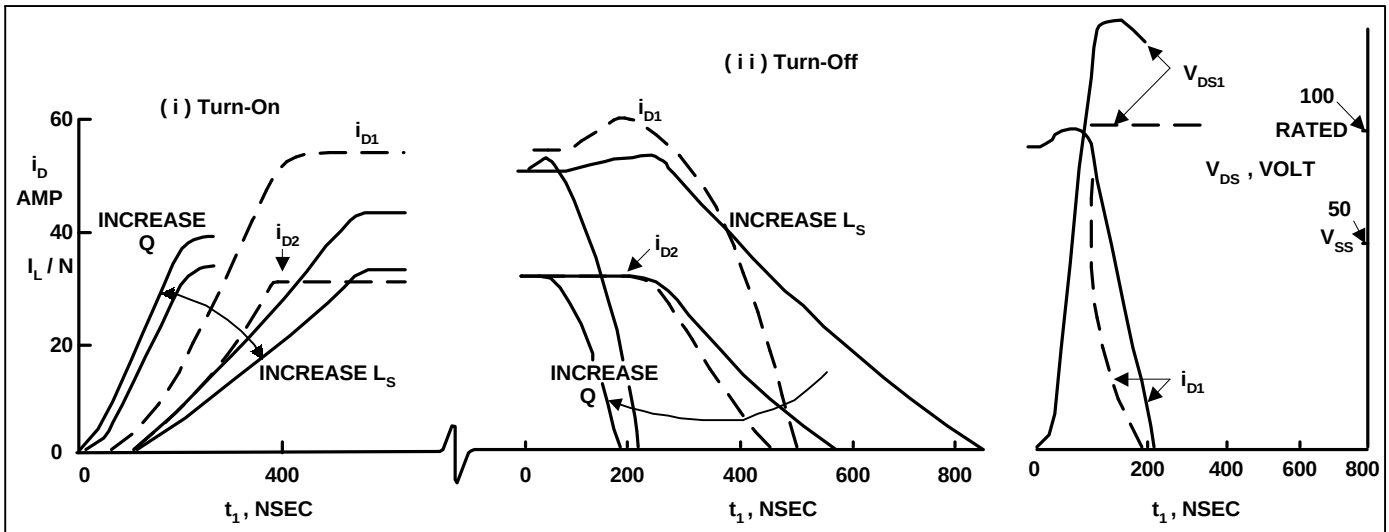


Figure 11(a): Drain Current and Voltage for #1 and #2 HEXFETs

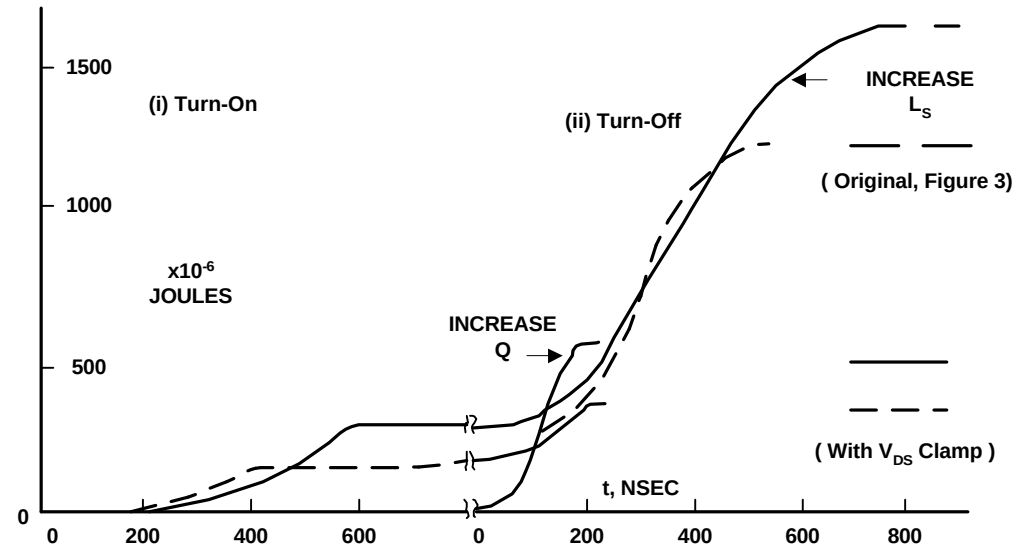


Figure 11(b): Transition Energy for #1 HEXFET

Figure 11. Comparison of Methods for Reducing Peak Dynamic Current Unbalance: Technique B - Increasing Common Source Inductance, L_S / L_X = 20%, Q =Q1 (R_{GC} = 5.24 Ω); Technique C - Increasing Q by Reducing R_{GC}, L_S / L_X = 5%, Q = Q_2 (R_{GC} = 1.29)

Returning to the dynamic current unbalance example of Figure 3 the above information is applied to reduce the unbalance. Using technique B the common source inductance, L_S, is increased from 10 to 40 nh. This modifies the basic Q_1 switching loci in Figures C2 and C3 from the original L_S = 5% to L_S = 20%. The transition energies increase. The impact of this change is illustrated in Figure 11. The original current unbalance differentials of 23A during turn-on ant 29A during turn-off are reduced to 13A and 22A differentials, respectively. The total transition energy dissipated by the device increases by 33% from 1330 to 1780 microjoules. It is interesting to note that for a case temperature of 87 °C, the device would be limited to an operating frequency of 42kHz due to these transition losses alone.

To apply technique C, the basic Q locus is shifted. Consider the results of increasing Q from Q_1 to Q_2 by reducing R_{GC} from 5.24 to 1.29Ω. For Q_2 with L_S = 5%, Figures C2 and C3 predict significantly lower transition energies and an increase to peak turn-off voltage to 125V.

The effect on dynamic current unbalance is shown in Figure 11(a). The original differentials of 23A during turn-on and 29A during turn-off are reduced to 5A and 22A differentials, respectively. Figure 11(b) shows that the transition energies are reduced as expected. Figure 11(a) also confirms a higher than rated peak drain-source voltage (V_{DS1}) during turn-off. The effect of including an energy diverter circuit such as a zener diode or a diode-capacitor-return resistor is also illustrated (dashed). With the HEXFET Power MOSFET voltage clamped at 100V, the drain current reduces more rapidly. This results in a further reduction of the total HEXFET Power MOSFET transition energy to 360 microjoules. Excluding other losses this would raise the operating frequency limit from 42kHz using technique B to 155kHz for technique C. The diverter circuit increases the turn-off energy due to the lower turn-off voltage from 620 to 890 microjoules for #1 branch in this example. Part of this increase can be returned to the supply, depending on the diverter circuit design.

IV (b) (iii) Limiting Unbalance with the Gate Driver

It has been generally shown that increasing the Q value of the dynamic load line reduces current unbalance, particularly during turn-on Technique C is most effective for larger pulse duty cycles where IB ~ 0.5 I_{DM} (Figure 10(a)).

By increasing Q sufficiently, it has been shown in Table 10 that the peak dynamic current unbalance generated by data sheet parameter extremes can be held to approximately 15% during turn-on By matching $R_{DS(on)}$, this unbalance limit can be held until turn-off.

Technique C requires a very low L_S/L_X ratio and as shown in Figure 9, it results in a large unbalance current and high peak voltage during turn-off. For higher duty cycle pulses the unbalance current can be accommodated within the SOA. An energy diverter circuit may be added to clamp the voltage. Alternatively , depending on E_T/E_C, a lower value for Q may be used for turn-off.

As given in equation (6), Q may be increased by raising the average gate driver current or the commutation inductance. This choice may be dictated by operating frequency since the former reduces transition energy whereas the latter raises it.

For medium to high duty cycle current pulses, applied over wide frequency range, parallel current unbalance can be constrained to modest levels by appropriate gate driver design without any device (HEXFET Power MOSFET) screening except for $R_{DS(on)}$.

IV (b) (iv) Combined Techniques For Minimum Overall Unbalances

For the shorter pulse of Figure 10(b) in which I_B approaches the SOA limit of I_{DM}, both turn-on and turn-off dynamic current unbalance must be limited.

To minimize the device unbalance generators, the designer can minimize gate decoupling resistance and screen devices from a given production batch (date code) with 90% yield limits. For practical reasons L_S/L_X may approach 10%. This tends to equate turn-on and turn-off unbalance and also raise transition energy which is significant in short pulses. To limit transition energy increased Q through an augmented gate driver may be used.

Figure 12 illustrates current and energy balance using the above techniques. This is predicted without the use of current balancing transformers drain current feedback to the driver circuit or current sharing resistors.

IV (c) Summary of Recommendations for Balancing Parallel MOSFET Currents

The following recommendations are generally applicable. For certain extreme operating conditions such as very high frequency, large numbers of parallel devices, ultra fast gate drivers, some recommendations may not apply (refer to paper).

IV (c) (i) General

Screening, Parameter Matching

- MOSFET gate-to-source and Miller capacitance mismatch are not significant provided decoupling resistance is limited to less than 10% of total driver resistance
- Branch inductance and decoupling resistance (for above recommendation) mismatch are not significant.
- Matching common source inductance (for $L_S/L_X > 1\%$) assists dynamic current balance.
- Screening MOSFET $R_{DS(on)}$ is sufficient for steady-state current balance.
- MOSFET threshold voltage and gain factor (transconductance) screens are effective for dynamic current balance.

Power Circuit Modifications

- Additional series resistance, current balancing transformers or feedback to the gate driver are not needed for current balance.
- Increasing common source inductance assists dynamic current balance. This also increases transition energy.

Gate Driver Modifications

- Minimizing decoupling resistance assists dynamic current balance by reducing differential gate-source voltages between parallel MOSFETs Partial gate decoupling (approximately 10%) may be required for parasitic oscillation control.
- Increasing the dynamic load line Q value assists dynamic current balance. This reduces transition energy, but increases peak turn-off voltage Restrict Q value to not more than Q_2 for turn-on, otherwise differential branch inductance may contribute to current unbalance.

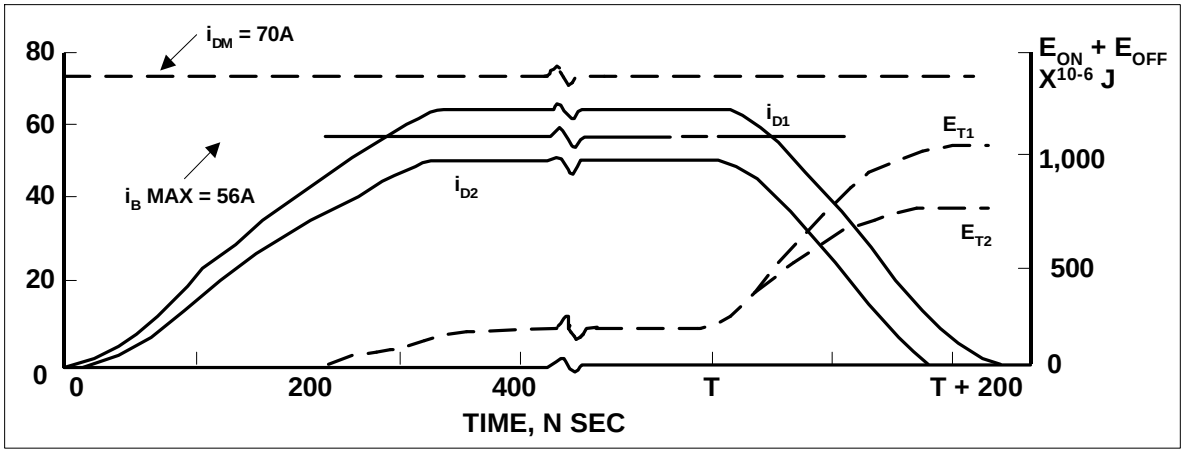


Figure 12: IRF150 Current and Energy Unbalance For N=2 With Techniques A, B and C Combined For Short Pulse Duty Cycle-Single Production Batch Parameter Mismatch (Tables 3 and 11), L_S/L_X=10%, R_G/N 10%, Q=Q_2

IV (c) (ii) Pulse Duty Cycle > 30%

Starting from a general set of parameter mismatch to balance turn-on current, minimize L_S/L_X and increase Q to Q_2. For low frequency applications with $E_T/E_C << 1$, reduce Q to Q_1 during turn-off to alleviate turn-off voltage stress For high frequencies, with ETlEc >> 1, use Q_2 and an energy diverter circuit for turn-off.

IV (c) (iii) Pulse Duty Cycle < 30%

To minimize turn-on and turn-off current differentials, increase L_S/L_X and increase Q to Q_2. For high frequency, with $E_T/E_C >> 1$, the value for L_S/L_X required to offset parameter mismatch may generate excessive losses. Some screening or matching may be require to allow a lower L_S/L_X ratio.

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APPENDIX A

Current Unbalance Limits for ON Resistance Mismatch

Equations ant graphs describing parallel branch current unbalance due to mismatched ON-state drain-source resistancesm$R_{DS(on)}$ are derived for the 'worst case' circuit of Figure 1. The first branch is assigned a reduced resistance and the remaining N-1 branches are assigned identical values (refer Figure A-1).

Current unbalance graphs are derived for two general cases (refer Figure 4):

(1) $0 \le R_{DS(on1)} \le R_{DS(on2)} \le 1.0$; N = 2, 5, ∞; T_J held constant at 25°C.

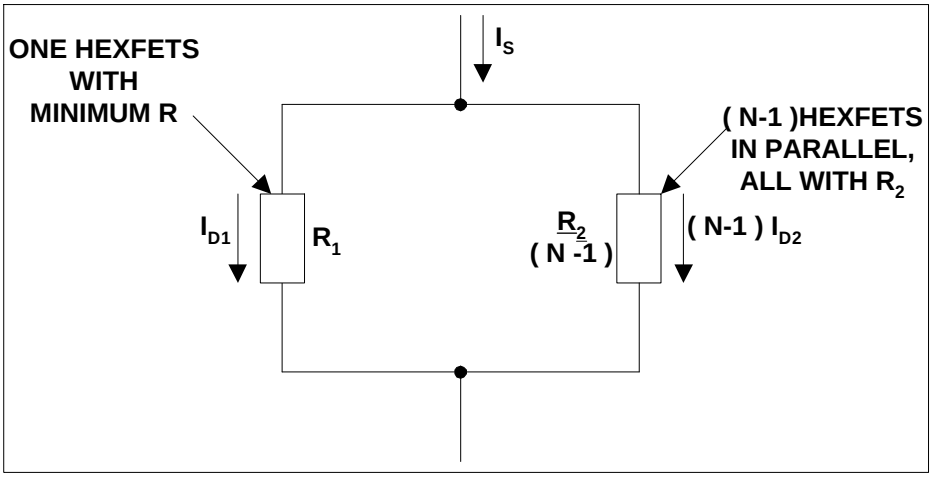

Figure A1 : Equivalent Circuit for Computing Worst Case Steady-State Current Unbalance Due To $R_{DS\ ON}$ Mismatch

(2) for above parameter range, the unbalance current is corrected for junction temperature change with the junction-to-ambient design temperature rise set at 56°C.

For the circuit (Figure A1),

$I_S = I_{D1} + (N\text{-}1)\, I_{D2}$ (A1)

with equal voltage drop:

$I_{D1}R_{1T} = I_{D2}R_{2T}$ (A2)

where the subscript 'T' indicates the resistance value at temperature, T.

$R_{iT} = R_{i\text{-}25}\,\{1 + [(T_A\text{-}25) + I^2_{Di}R_{iT}\theta_{JA}]K\}$ (A3)

where Ri-25 is the i^{th} branch limiting maximum value of ON resistance at 25°C, θ_{JA} is the total junction-to-ambient resistance in deg. C/W, and K is the per unit change of ON resistance per °C.

Solving (A3) for R_{iT} and substituting into (A2),

$$\mathbf{I_{D1}} \cdot \frac{\mathbf{R_{1-25}}}{\mathbf{1 - R_{1-25} I_{D1}^2 \theta_{JA} K}} = \mathbf{I_{D2}} \cdot \frac{\mathbf{R_{2-25}}}{\mathbf{1 - R_{2-25} I_{D2}^2 \theta_{JA} K}} \quad \text{(A5)}$$

The balanced current (I_B) for each device is,

$I_B = I_S/N$ (A6)

Substituting from (A6) and (A1) into (A5),

$$\mathbf{I_{D1}} \cdot \frac{\mathbf{R_{1-25}}}{\mathbf{1 - R_{1-25} I_{D1}^2 \theta_{JA} K}} = \frac{\mathbf{NI_B - 1}}{\mathbf{N - 1}} \cdot \frac{\mathbf{R_{2-25}}}{\mathbf{1 - (NI_B - I_{D1})^2 \cdot \dfrac{R_{2-25}\theta_{JA}K}{(N-1)^2}}} \quad \text{(A7)}$$

Expressed as a cubic equation of I_{D1}, (A7) becomes,

$$\frac{\mathbf{R_{1-25}R_{2-25}\theta_{JA}KN}}{\mathbf{(N-1)^2}} \cdot \mathbf{I_{D1}}^3 - \frac{\mathbf{R_{1-25}R_{2-25}\theta_{JA}KN(N+1)I_B}}{\mathbf{(N-1)^2}} \cdot \mathbf{I_{D1}}^2 - \frac{\mathbf{1}}{\mathbf{N-1}} \left\{ \mathbf{R_{2-25}} + \left[\mathbf{(N-1)} - \frac{\mathbf{\theta_{JA}KR_{2-25}(NI_B)^2}}{\mathbf{(N-1)}} \right] \mathbf{R_{1-25}} \right\} \cdot \mathbf{I_{D1}} + \frac{\mathbf{R_{2-25}NI_B}}{\mathbf{N-1}} = \mathbf{0} \quad \text{(A8)}$$

Dividing (A8) by I_B^3, $R_{2\text{-}25}$, $\theta_{JA}K$, rearranging terms and setting the design junction-to-ambient temperature rise for nominal resistance (ΔT_{2JA}) equal to,

$\Delta T_{2JA} = R_{2\text{-}25}\, I_B^2\, \theta_{JA}K$ (A9)

equation (A8) becomes,

$$\left(\frac{\mathbf{I_{D1}}}{\mathbf{I_B}}\right)^3 - \mathbf{(N+1)}\left(\frac{\mathbf{I_{D1}}}{\mathbf{I_B}}\right)^2 + \left[\mathbf{N} - \frac{\mathbf{N-1}}{\mathbf{N}}\left(\mathbf{N-1} + \frac{\mathbf{R_{2-25}}}{\mathbf{R_{1-25}}}\right) \cdot \frac{\mathbf{1}}{\mathbf{\Delta T_{2JA} \cdot K}}\right]\left(\frac{\mathbf{I_{D1}}}{\mathbf{I_B}}\right) + \mathbf{(N-1)}\left(\mathbf{\Delta T_{2JA} \cdot K} \cdot \frac{\mathbf{R_{2-25}}}{\mathbf{R_{1-25}}}\right) = \mathbf{0} \quad \text{(A10)}$$

For $N \rightarrow \infty$, (A10) reduces to a quadratic,

$$\left(\frac{I_{D1}}{I_B}\right)^2 - \left(1 - \frac{1}{\Delta T_{2JA} \cdot K}\right)\left(\frac{I_{D1}}{I_B}\right) - \left(\Delta T_{2JA} \cdot K \cdot \frac{R_{1-25}}{R_{2-25}}\right)^{-1} = 0 \qquad \text{(A11)}$$

Since rms current determines average junction temperature, for pulse currents with peak current I_B and normalized duty cycle T_{PN}, equation (A9) becomes,

$$\Delta T_{2JA} = R_{2\text{-}25}\, I_B{}^2\, T_{PN}\, \theta_{JA} \qquad \text{(A12)}$$

APPENDIX B

Current Unbalance Limits For Gate and Threshold Voltage Mismatch

Maximum current differentials for gain and/or threshold voltage mismatch(es) occur in the active region during relatively slow transitions in which common source inductance (L_S) voltage drops are negligible.

This current unbalance has limits which may be derived by holding the switch current (i_S) at the maximum value for a given transition (I_S) and computing the maximum unbalance current. For worst case unbalance between paralleled devices, assume N MOSFETs are arranged so that one device with adverse parameter mismatch is in the first branch and N-l identical devices are located in the remaining branches as illustrated in Figure Bl.

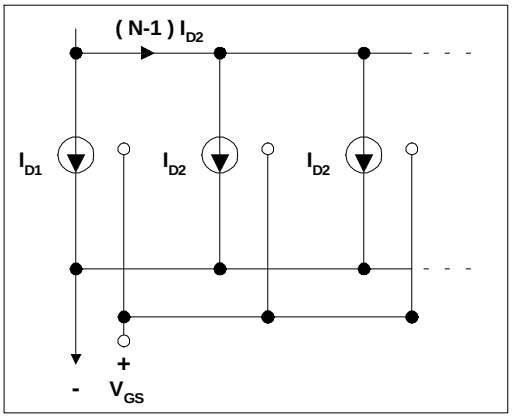

Figure B1 : Equivalent Circuit for Determination of Worst Case 'Static' Unbalance Current Limits

From Figure Bl,

$$I_S = I_{D1} + (N - l)\, I_{D2} \qquad \text{(Bl)}$$

Substituting from equation (1) and rearranging (Bl),

$$I_{D1} = I_S - (N\text{-}1)\, GF_2\, (V_{GS} - V_{T2})^2 \qquad \text{(B2)}$$
$$= GF_1\, (V_{GS} - V_{T1})^2 \qquad \text{(B3)}$$

Then, from (B2) and (B3),

$$V_{GS}{}^2 - \frac{2\left[GF_1 V_{T1} + (N-1)GF_2 V_{T2}\right]}{GF_1 + (N-1)GF_2} \cdot V_{GS} + \frac{GF_1 V_{T1}{}^2 + (N-1)GF_2 V_{T2}{}^2 - I_S}{GF_1 + (N-1)GF_2} = 0 \qquad \text{(B4)}$$

Solving for V_{GS},

$$V_{GS} = \frac{GF_1 V_{T1} + (N-1)GF_2 V_{T2}}{GF_1 + (N-1)GF_2} + \sqrt{\frac{-(N-1)GF_1 GF_2\left[V_{T1} - V_{T2}\right]^2 + \left[GF_1 + (N-1)GF_2\right] I_S}{\left[GF_1 + (N-1)GF_2\right]^2}} = 0 \qquad \text{(B5)}$$

The balance current for each device is given by,

$I_B = I_S/N$ (B6)

Also, let the differential threshold voltage be,

$V_{T1} - V_{T2} = \Delta V_T$ (B7)

Substituting from equations (B5), (B6) ant (B7) into equation (l),

$$\mathbf{I_{D1} = GF_1(V_{GS} - V_{T1})^2}$$
$$\mathbf{= \frac{GF_1}{[GF_1 + (N-1)GF_2]^2}} \quad \text{(B8)}$$
$$\mathbf{\cdot\left\{(N-1)GF_2\Delta V_T + \sqrt{N[GF_1 + (N-1)GF_2]I_B - (N-1)GF_1GF_2\Delta V_T{}^2}\right\}}$$

Then,

$$\mathbf{\frac{I_{D1}}{GF_1}}$$
$$\mathbf{= \left\{ \frac{(N-1)}{\frac{GF_1}{GF_2} + (N-1)} \cdot \Delta V_T + \sqrt{\frac{N}{\frac{GF_1}{GF_2} + (N-1)} \cdot \frac{I_B}{GF_2} - \frac{(N-1)\Delta V_T{}^2}{\left[\sqrt{\frac{GF_1}{GF_2} + (N-1)\sqrt{\frac{GF_2}{GF_1}}}\right]^2}} \right\}} \quad \text{(B9)}$$

For a large number of parallel devices, the worst case current unbalance for branch #1 (with adverse parameter mismatch) is given by,

$$\mathbf{\left.\frac{I_{D1}}{GF_1}\right|_{N\to\infty} = \left[\Delta V_T + \sqrt{\frac{I_B}{GF_2}}\right]^2} \quad \text{(B10)}$$

A convenient normalizing factor for this equation is I_{DM}/GF where for a given device,

I_{DM} = rated peak pulse current
GF = active region gain (from equation (l))

Let

$$\mathbf{\frac{I_{D1N}}{GF_{1N}} = \frac{I_{D1}}{GF_1} \div \frac{I_{DM}}{GF}} \quad \text{(B11)}$$

$$\mathbf{\frac{I_{BN}}{GF_{2N}} = \frac{I_B}{GF_2} \div \frac{I_{DM}}{GF}} \quad \text{(Bl2)}$$

$$\Delta V_{TN} = \Delta V_T \div \sqrt{\frac{I_{DM}}{GF}} \qquad \text{(Bl3)}$$

Then the normalized maximum unbalance current for $N \rightarrow \infty$ is given by,

$$\frac{I_{D1N}}{GF_{1N}} = \left\{ \Delta V_{TN} + \sqrt{\frac{I_{BN}}{GF_{2N}}} \right\}^2 \qquad \text{(Bl4)}$$

For $N < \infty$, from equation (B9)

$$\frac{I_{D1N}}{GF_{1N}} = \left\{ \frac{(N-1)}{\frac{GF_{1N}}{GF_{2N}} + N - 1} \cdot \Delta V_{TN} + \sqrt{\frac{N}{\frac{GF_{1N}}{GF_{2N}} + N - 1} \cdot \frac{I_{BN}}{GF_{2N}} - \frac{(N-1)\Delta V_{TN}^2}{\left[\sqrt{\frac{GF_{1N}}{GF_{2N}}} + (N-1)\sqrt{\frac{GF_{2N}}{GF_{1N}}} \right]^2}} \right\}^2 \qquad \text{(Bl5)}$$

APPENDIX C

Dynamic Load Lines and Transition Energy

For MOSFETs, dynamic load lines can be generalized by introducing a concept that relates the device and its gate driver to the power circuit. The concept of 'Q' loci, although not precise, allows one to organize significant factors influencing switching loci into simple groupings that are very useful for prediction. Q loci are used to map dynamic load lines and transition energies.

The Q locus for a MOSFET relates its average gate current during transition through the active region to the external circuit inductance (L_X) that is, in part, controlling the transition time (see Figure C1). In reference to Figure 1:

$Q = I_G \bullet L_X$ (C1)

where L_X is the commutation inductance,

$L_X = L_D + (L_{SS1} + L_{SS2}) \bullet N$,

and I_G equals the average device gate current during the active region transition.

Source inductance common to the gate ant drain power circuits (L_S, refer Figure 1) has been omitted from equation (C1). It is given separate treatment later. Dynamic load lines for the IRF150 are mapped by Q loci (solid lines) in Figure C2a ant C3a. For low values of Q, the device supports the supply voltage during the turn-on transition. During turn-off, the device develops a relatively Low voltage in excess of the supply to reduce the branch current. Loci for high Q values indicate that the external inductance supports the supply voltage during turn-on. Also, the device develops a large voltage to drive the branch current to zero during turn-off.

Equation C1 states that the switching locus in the active region depends only on the product of average gate current and the power circuit inductance controlling the transition. The transition time will vary depending on the specific inductance value. However, for a given value of inductance, a higher Q value means shorter transition time ant lower switching energy as shown by the solid lines in Figures C2b ant C3b. The introduction of common source inductance (L_S) to the gate and power circuit results in increased drain-to-source voltage during turn-on and therefore a higher transition energy. The dashed lines in Figures C2a and

b map the dynamic load line deflection and the increase in turn-on energy for increased values of L_S/L_X.
Similarly, during turn-off, the addition of common source inductance in Figure C3b increases the transition energy dissipated by the device. However, as shown in Figure C3a, the peak drain-to-source voltage is reduced during turn-off. These results are consistent since the lower drain-to-source voltage means a longer time is required to commutate the current in the external power circuit inductance, L_X. Therefore, the greater amount of energy drawn from the supply during this increased time contributes to the increased device transition energy.

To determine the value of R_{GC}, the following procedure is used:

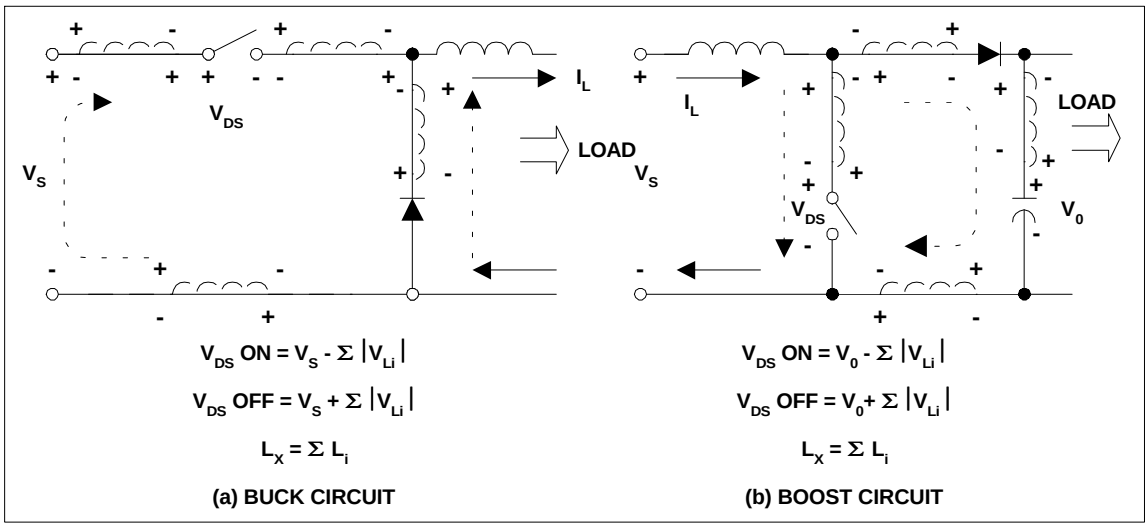

Figure C1: Illustration of Commutation Inductance, L_X , for Two Common Circuits - L_X Controls Current Transfer Between the Two Branches

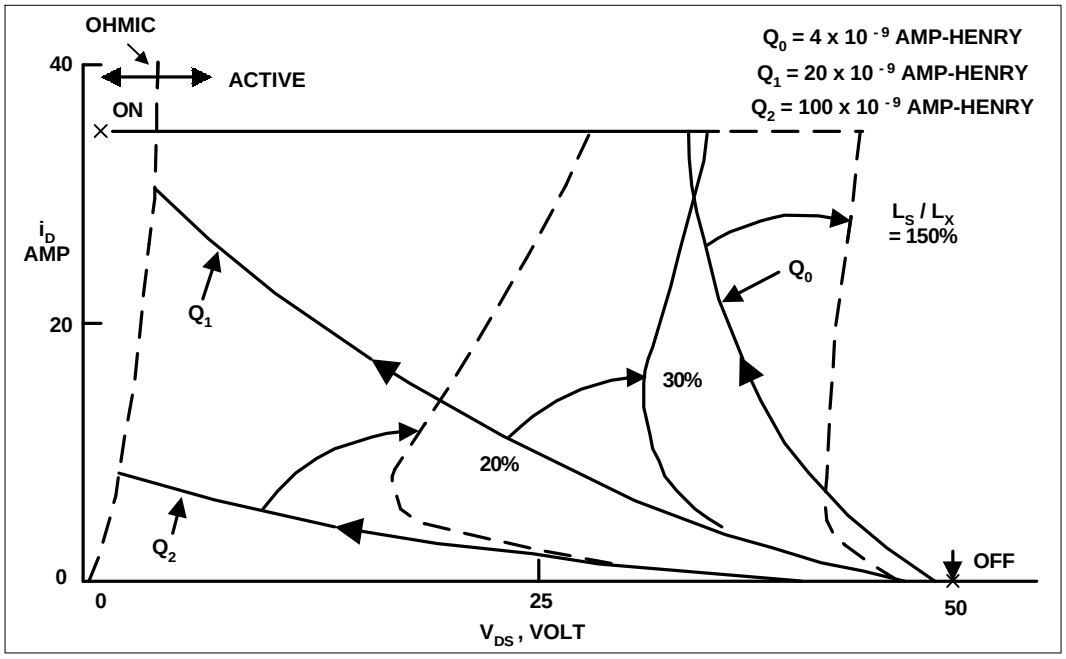

Figure C2(a): Dynamic Load Line Mapping By Q Loci Including Deflection By L_S / L_X

From equation C1:

$$I_{G2} = \frac{Q}{L_X}$$

$$\cong \frac{V_{DR} - \left(\frac{V_{T2} + V_B}{2}\right)}{R_{G2}} \qquad \text{(C2)}$$

where V_B is the value of V_{GS2} at the active/ohmic region boundary for the specific Q locus ($V_{GS2} = V_{DS} + V_{T2}$, refer Figure C2a).

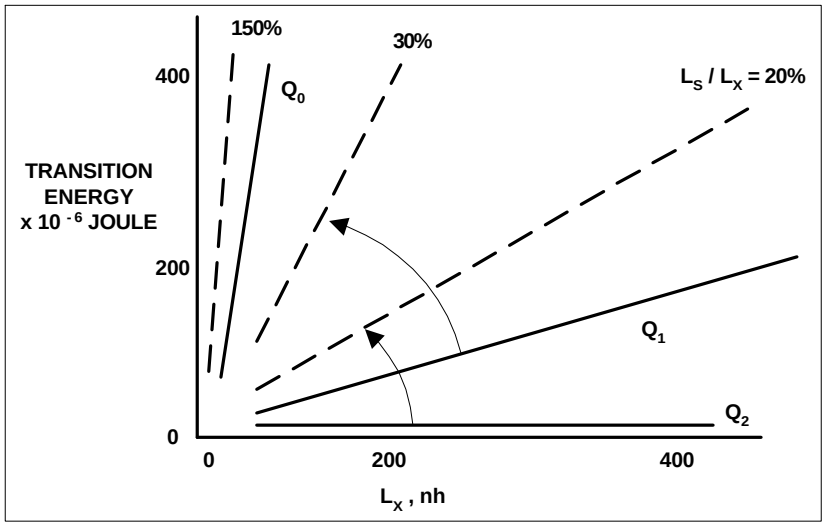

Figure C2(b): Transition Energy Mapping By Q Loci

Figure C2(a) & C2(b): Q-Loci For IRF150 Turn-On

$$R_{G2} \cong \frac{V_{DR} - \left(\frac{V_{T2} + V_B}{2}\right)}{Q} L_X \qquad \text{(C3)}$$

For 100% decoupling between N parallel devices, let

$$R_{GC} = R_{G2}/N \qquad \text{(C4)}$$

and set R_{Gi} equal to zero.

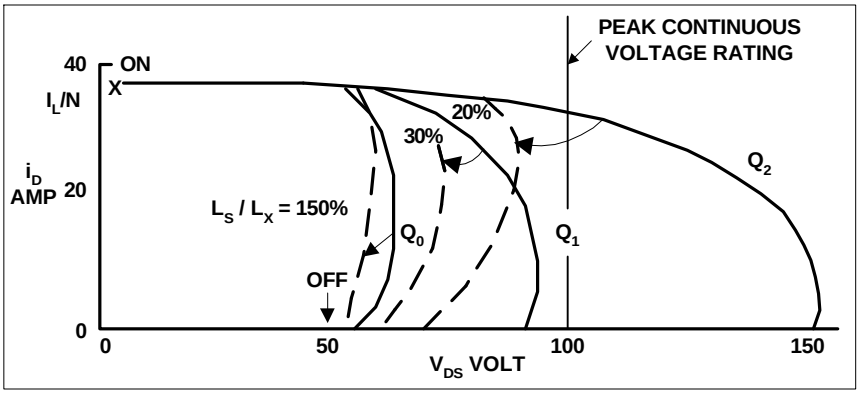

Figure C3(a): Dynamic Load Line Mapping By Q Loci Including Deflection By L_S / L_X

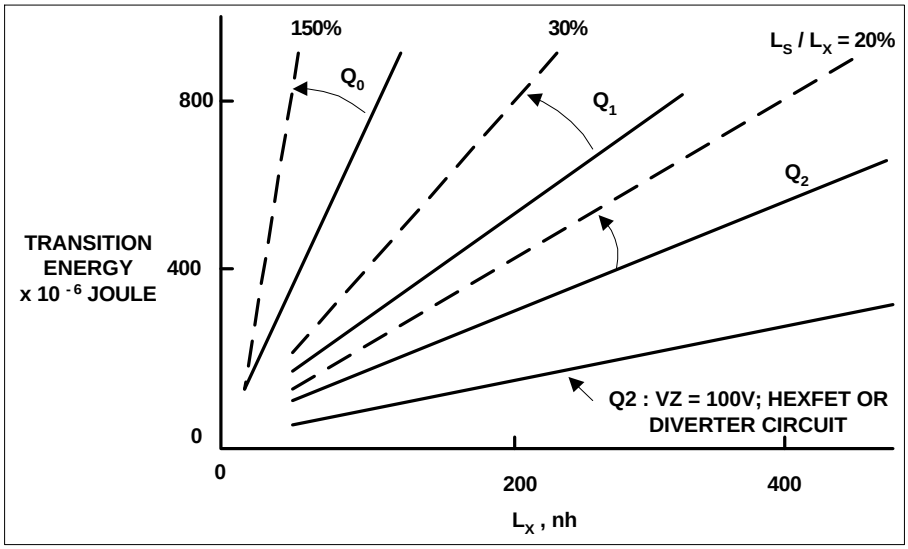

Figure C3(b): Transition Energy Mapping By Q Loci

Figure C3(a) & C3(b): Q-Loci For IRF150 Turn-Off