Flat Panel PDP Displays

SPARTAN-IIE FPGA

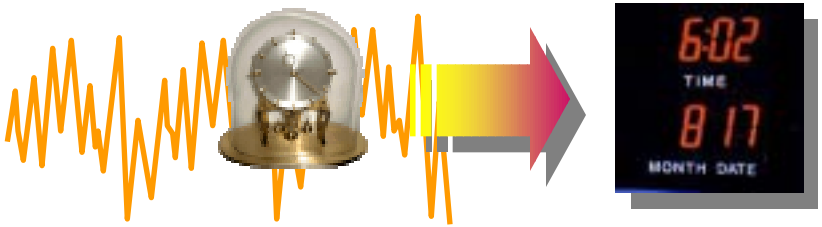
esp EMERGING STANDARDS & PROTOCOLS

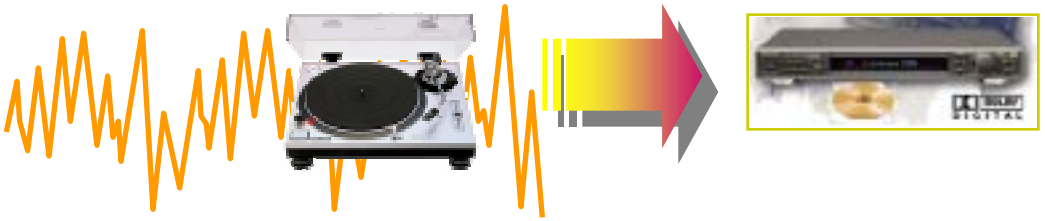
Agenda

- Introduction and market overview
- System analysis and design challenges
- Xilinx value in digital PDP display systems
  - System I/O
  - Forward error correction
  - Image processing
  - Content protection
  - Component interconnectivity
  - System control
  - Memory and controllers
  - Clock Generation/distribution
- Xilinx programmable solutions
- Xilinx eSP
- Summary

Introduction & Market Overview

The Digital Age of Consumer Electronics





Digital technology brings

- Higher accuracy
- Higher reliability
- Faster speed
- Lower power
- Lower cost

Digital Logic Spawns New Consumer Products

Digital TV

Revolutionizing the way we watch television

Consumer Satellite Modems

Revolutionizing high speed home Internet access

Desktop Video Editing

Delivering video editing to the home

Smart Card

Revolutionizing the way we purchase products

MP3 Players

The new revolution in portable digital music

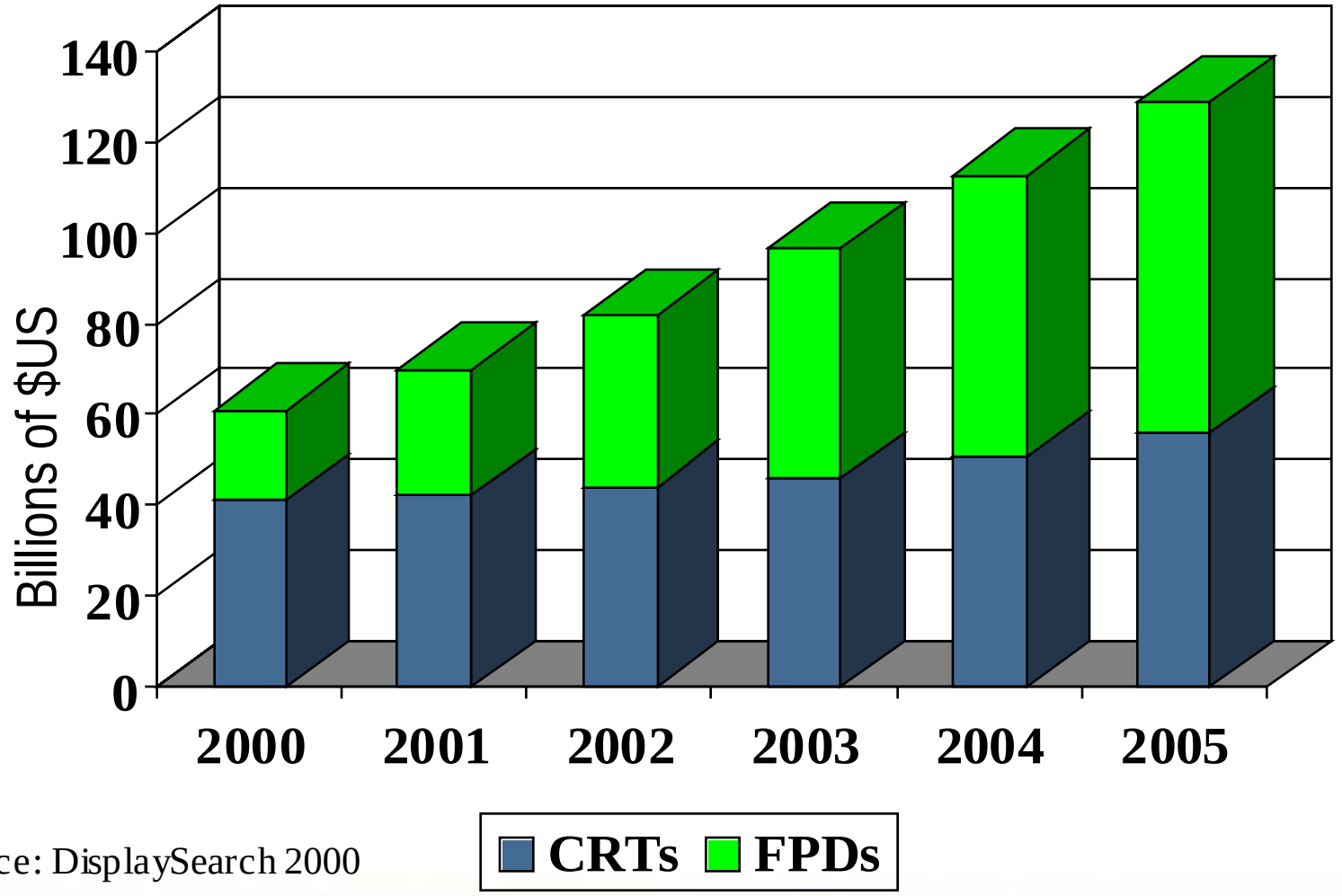
Convergence Is Happening!

- Digital revolution
  - Infrastructure: Circuit-switched to IP-based networks
  - Analog TV to digital TV
- Internet is ubiquitous
  - Being deployed within commercial channels
    - Business-to-Business commerce, secure transaction processing, banking
  - The ultimate vehicle for digital content delivery
- Deregulation of global infrastructure
  - Multiple industries such as telecom, cable and utilities

So Why Digital Displays?

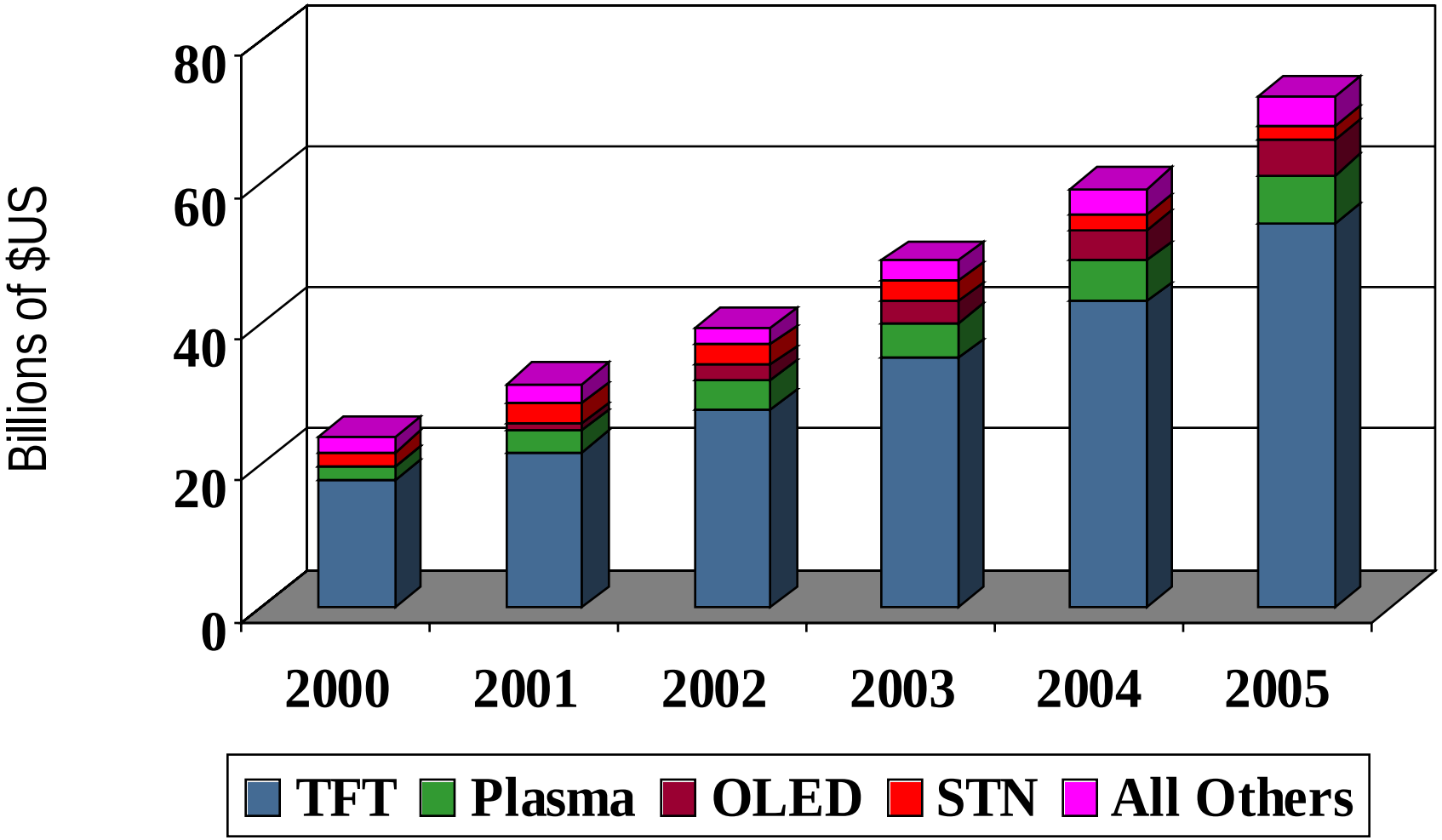
- Content has become predominantly digital
  - PC, digital TV, DVD, the Internet
- Quality
  - Digital content enables superior display processing
    - Filtering, color correction, image enhancement
  - Higher resolutions
- Industrial design
  - Digital has enabled “Flat Panel Display”
  - Wall-mounted and portable
- Cost
  - Ability to leverage semiconductor economies of scale

FPD Forecast vs. CRT



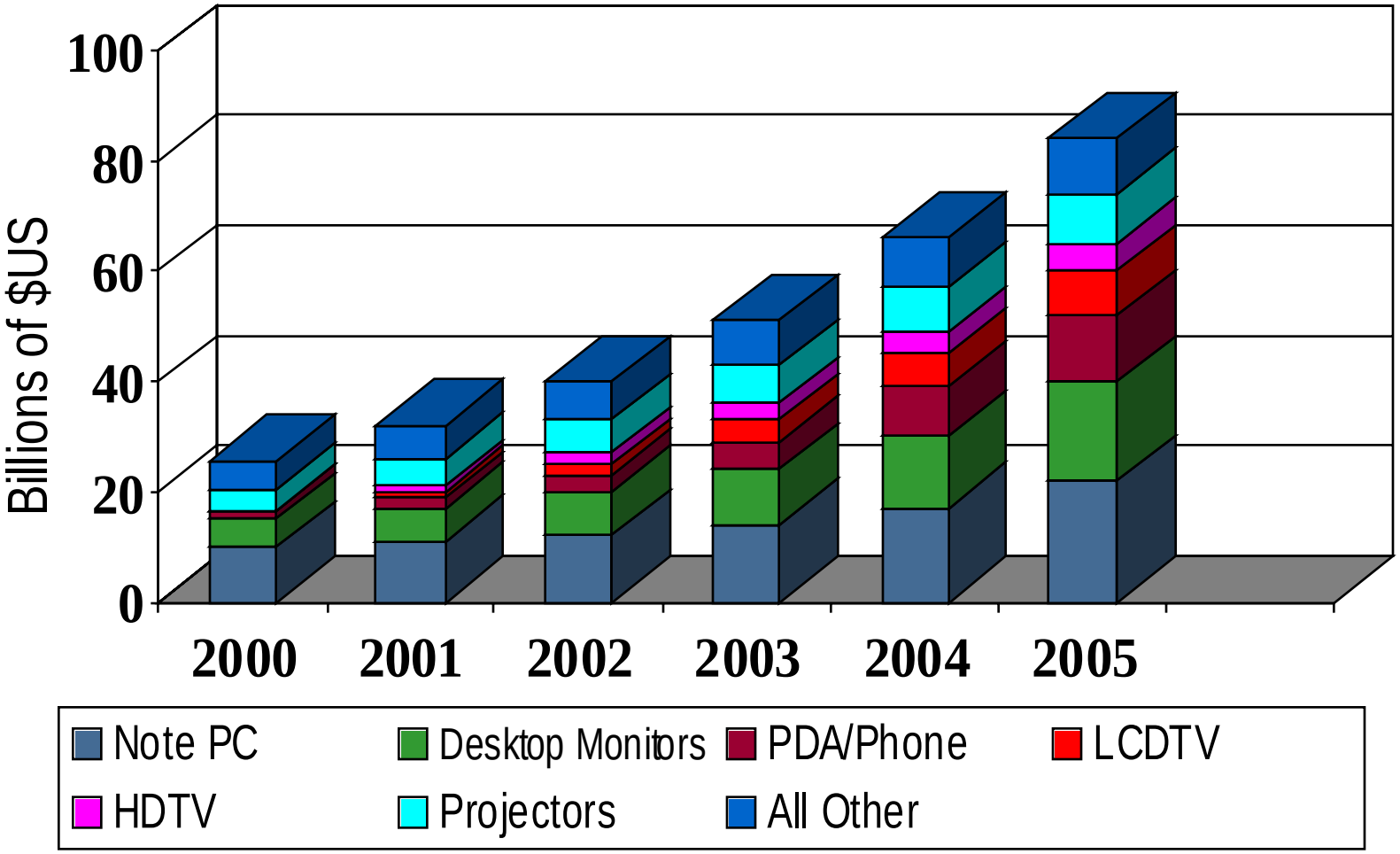
Source: DisplaySearch 2000

FPD Forecast by Technology



Source: DisplaySearch 2000

Display Forecast by Application



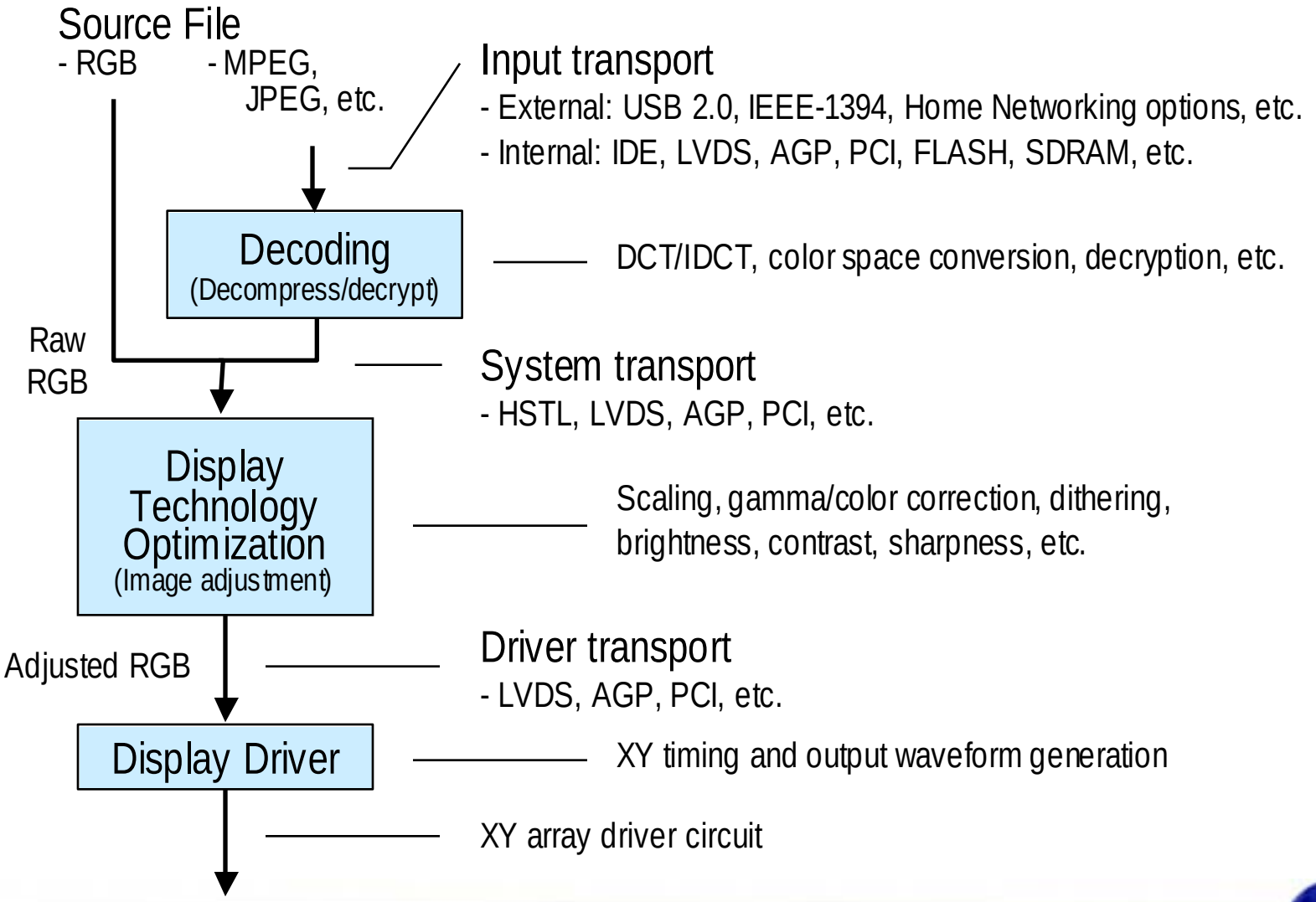
Source: DisplaySearch 2000 (displays) and Stanford Resources 2001 (Projectors)

Accelerators/Inhibitors

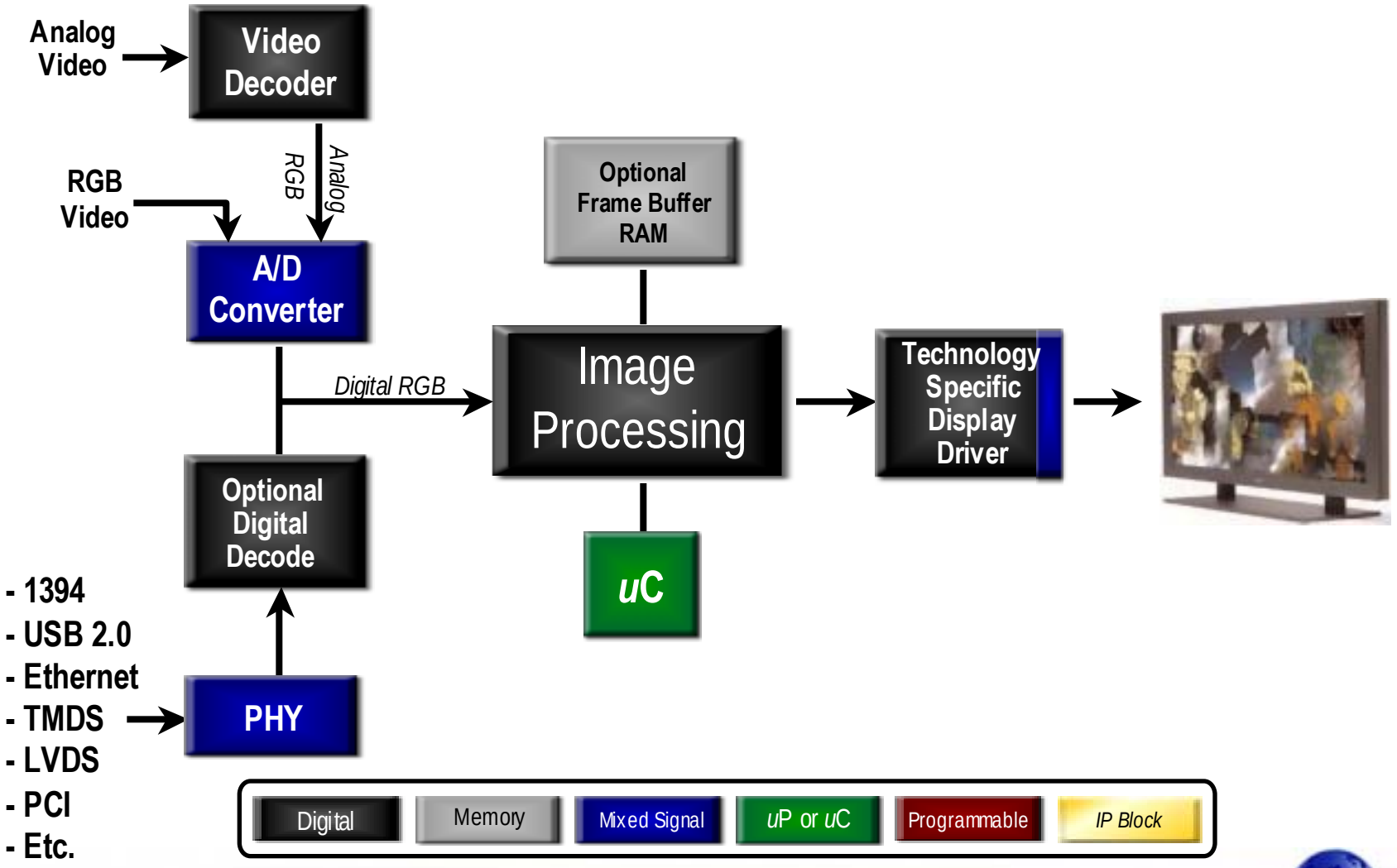
- Accelerators
  - Improving quality
  - Expanding content
    - The Internet
    - DVD
  - Digital TV deployment
  - Broadband access
  - Superior form factor
    - Less desk space
- Inhibitors
  - Cost is still high
  - Content protection is in flux
    - Must avoid a video Napster scenario
  - Standards are in flux
  - Broadband deployment is slower than expected

PDP Display System Analysis and Design Challenges

Digital Display System Data Flow



Generic Display System Block Diagram



Digital Display Design Challenges

- System connectivity
  - Which interface options should you support? Can you support more options to increase the accessible market?
- Component interconnectivity
  - How do you integrate the best selection of components to address your application?
- Image processing
  - How do you meet the performance challenge? How do you maintain compatibility with geographically divergent and continuously evolving formats and standards?
- User interface
  - How do you implement the best possible user interface to your design?
- System control
  - How do you control the system?
- Display driver circuitry
  - How do you best implement the driver circuit to get to market quickly and achieve supplier flexibility for this high dollar BOM component?

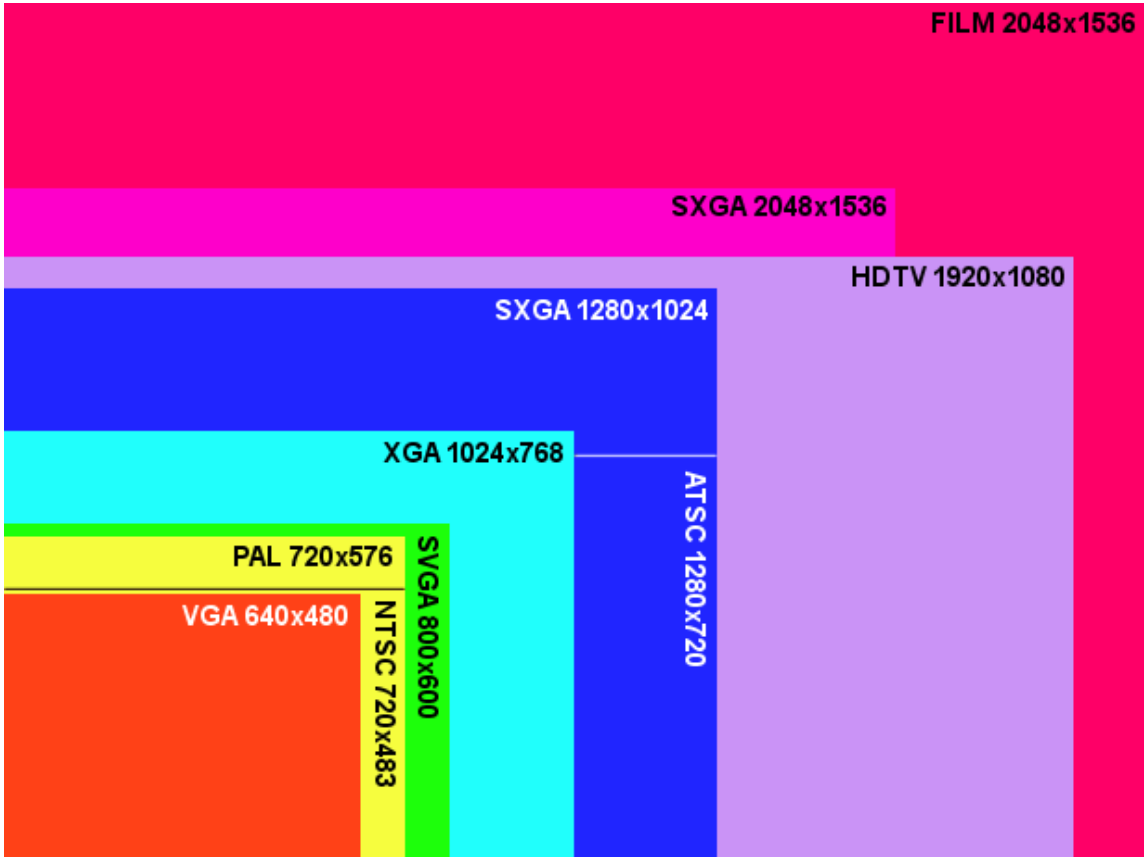
Digital Display Design Challenges System Connectivity Options

- High speed serial options
  - 1394
  - USB 2.0
- High speed parallel
  - TMDS
  - LVDS
  - PCI
  - AGP
- Broadband network
  - Ethernet
  - Cable/Satellite/DSL
  - Wireless

Digital Display Design Challenges
Display Image Processing

- Variable resolutions and refresh rates
- Variable scan mode characteristics
- High performance requirements
- Variable file encoding formats
- Variable content security formats

Digital Display System Challenges
Ratios and Resolutions



Courtesy: Snell & Wilcox

Digital Display System Challenges
Video Scanning Formats

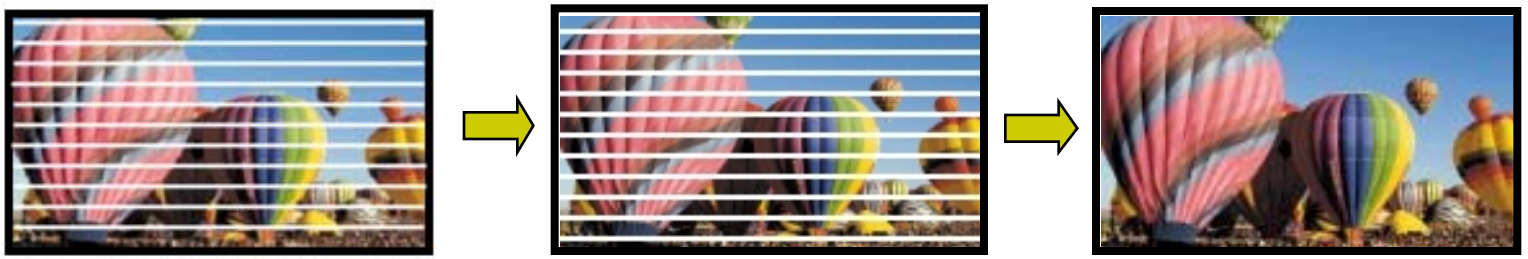
Definition	Lines/Frame	Pixels/Line	Aspect Ratios	Frame Rates
High (HD)	1080	1920	16:9	23.976p, 24p, 29.97p, 29.97i, 30p, 30i
High (HD)	720	1280	16:9	23.976p, 24p, 29.97p 30p, 59.94p, 60p
Standard (SD)	480	704	4:3, 16:9	23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p
Standard (SD)	480	640	16:9	23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p

- Table III is well known in the broadcast industry
- List of standard formats from ATSC A.53 DTV standard
- 36 different formats available!
- Doesn't take into account line doubling, etc.

Digital Display System Challenges
Interlace/Progressive Scan

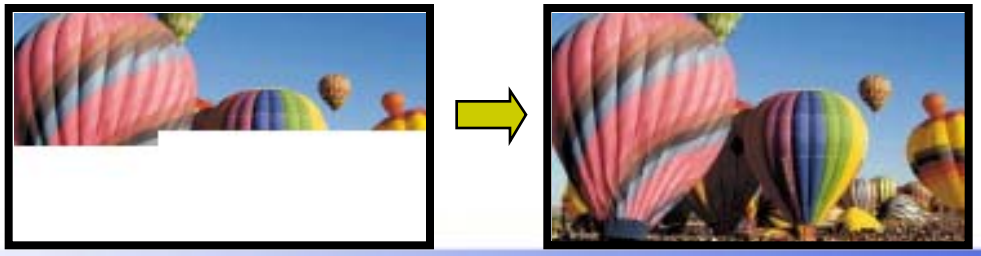
Interlace

First all odd lines scanned (1/60sec) **then all even lines (1/60sec)** **presenting a full picture (1/30sec)**



Progressive

All lines scanned in single pass **presenting a full picture (1/60sec)**



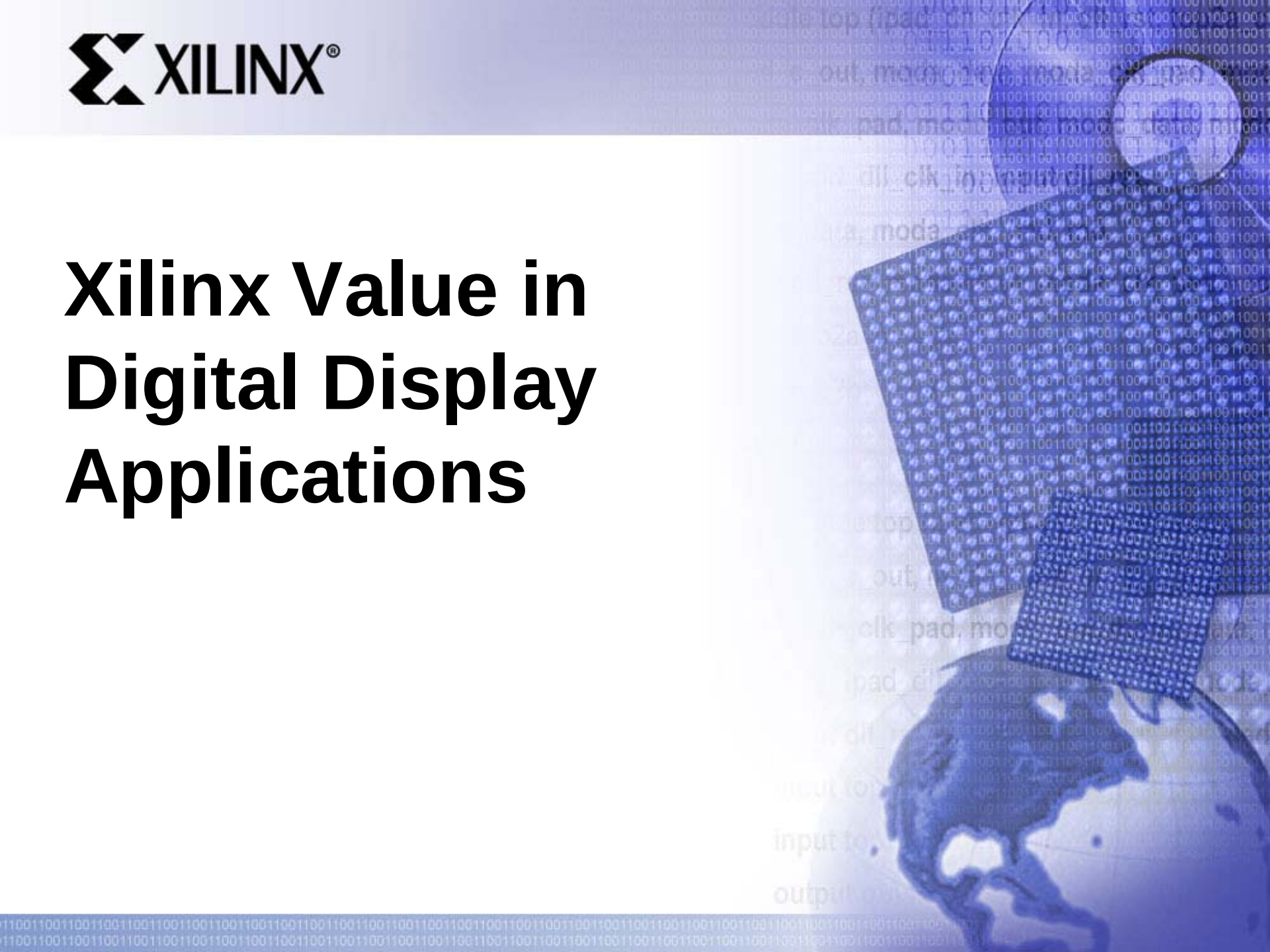
Digital Display System Challenges Performance

- Take an HDTV example:
  - 1920 x 1080 resolution
  - 24-bit pixels
    - 8-bit Red, Green and Blue values
  - 30 progressive frames per second
- Bandwidth = 1920 x 1080 x 24 x 30 = 1.49Gbps

Digital Display Design Challenges System Integration and Control

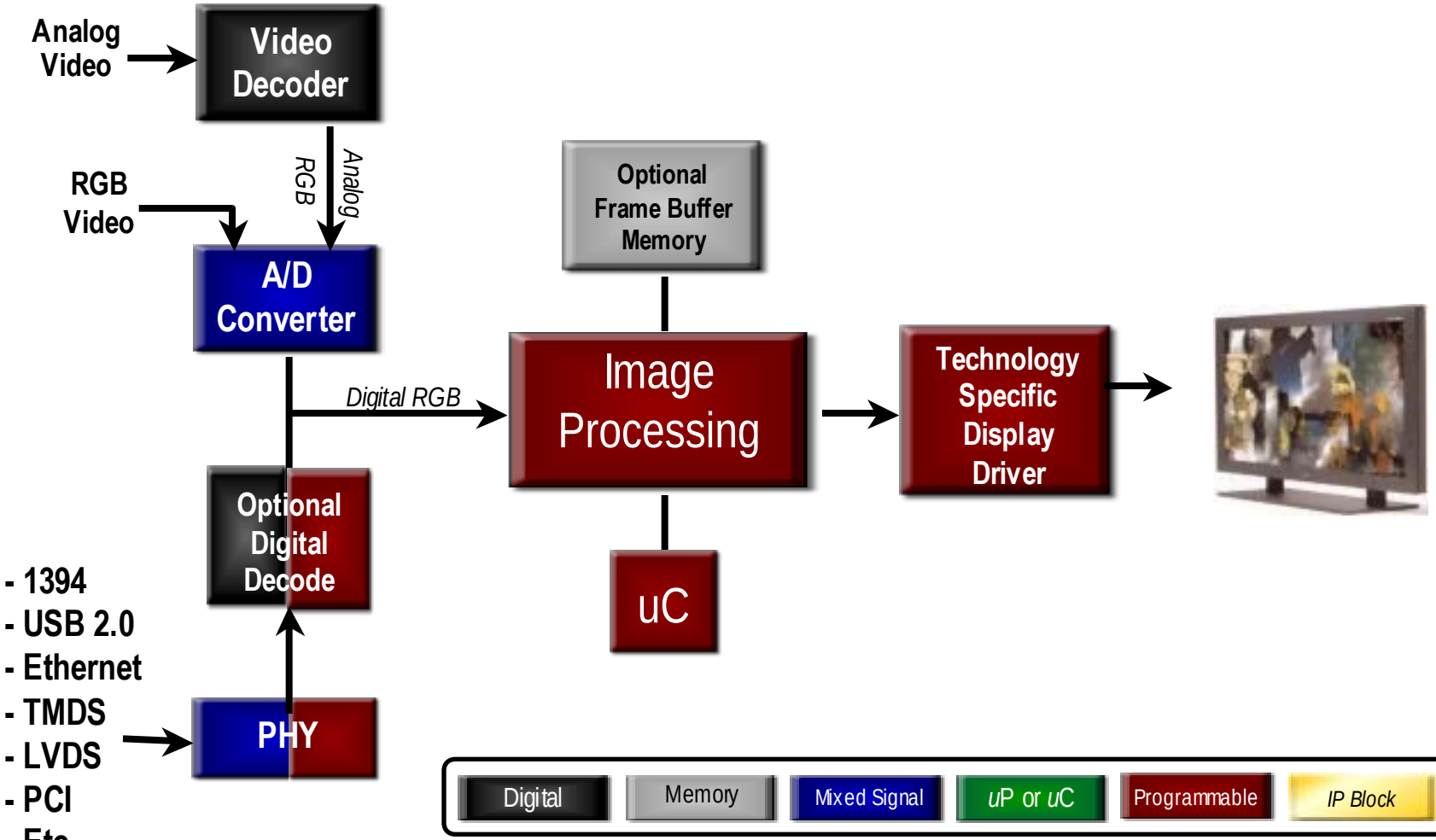
- Component interconnection
- System control logic
- Memory and storage subsystems
- User interface integration
- Supervisory system control

Xilinx Value in Digital Display Applications

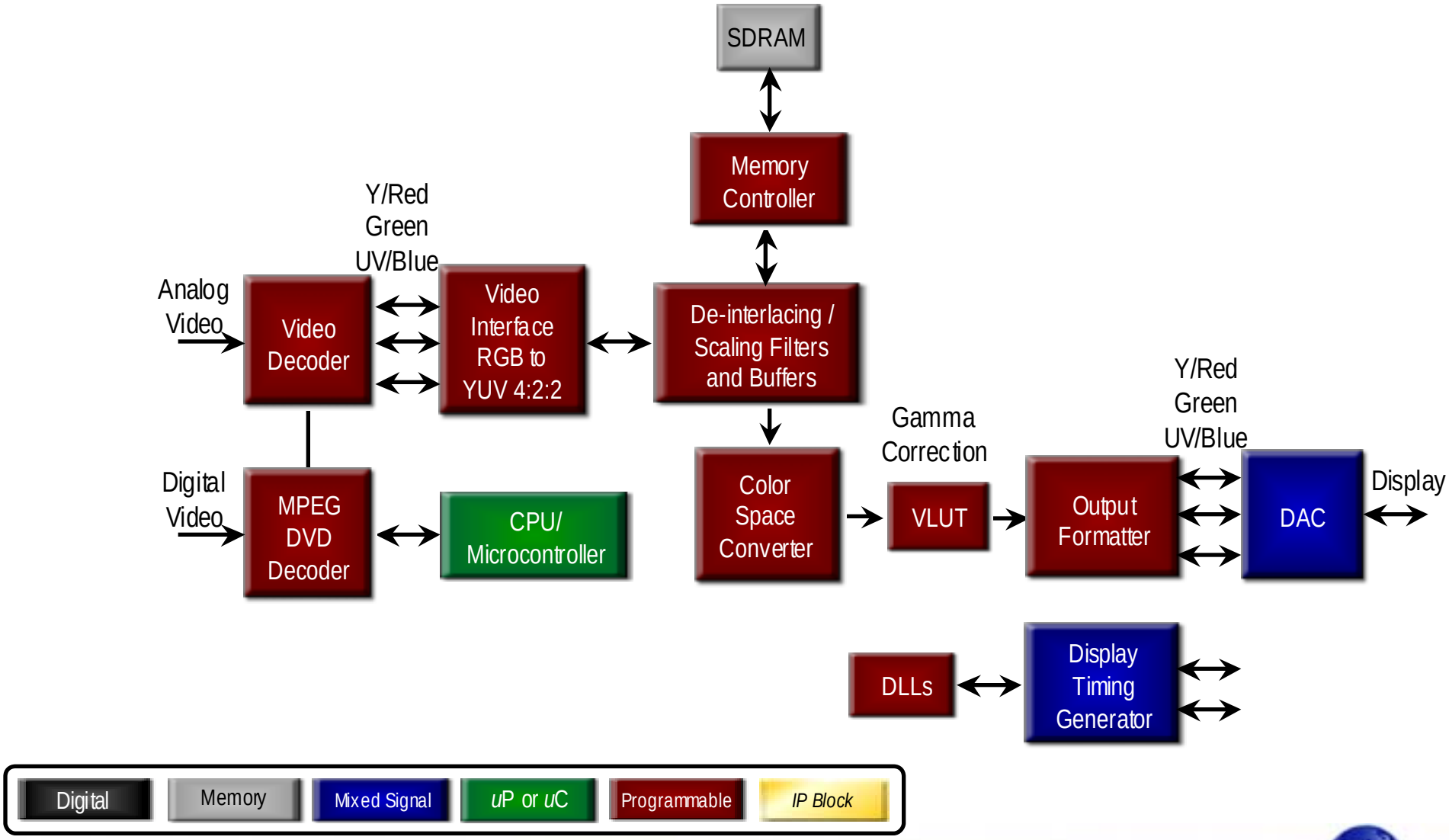


Programmable Logic Utility

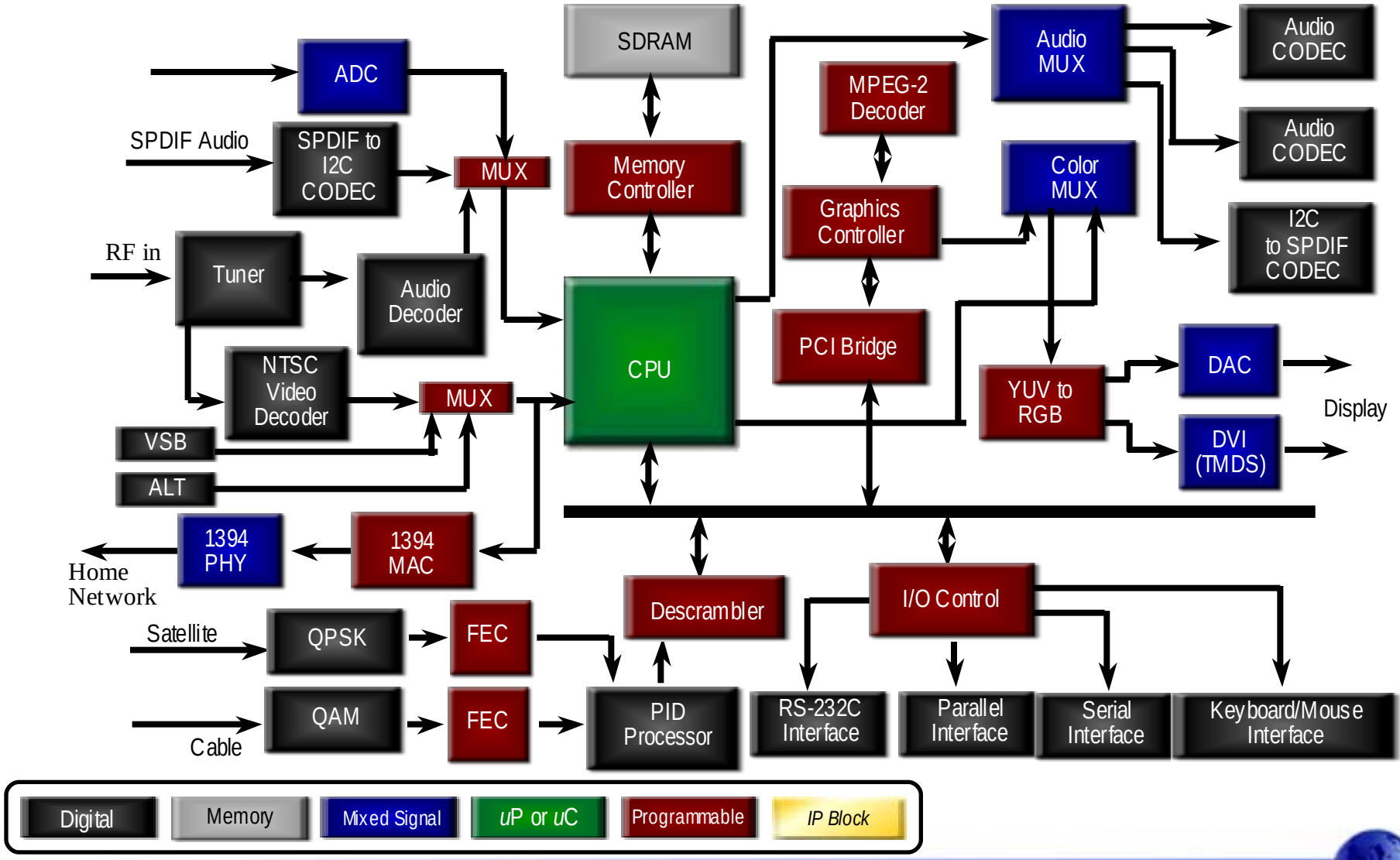
Where FPGAs Add Value



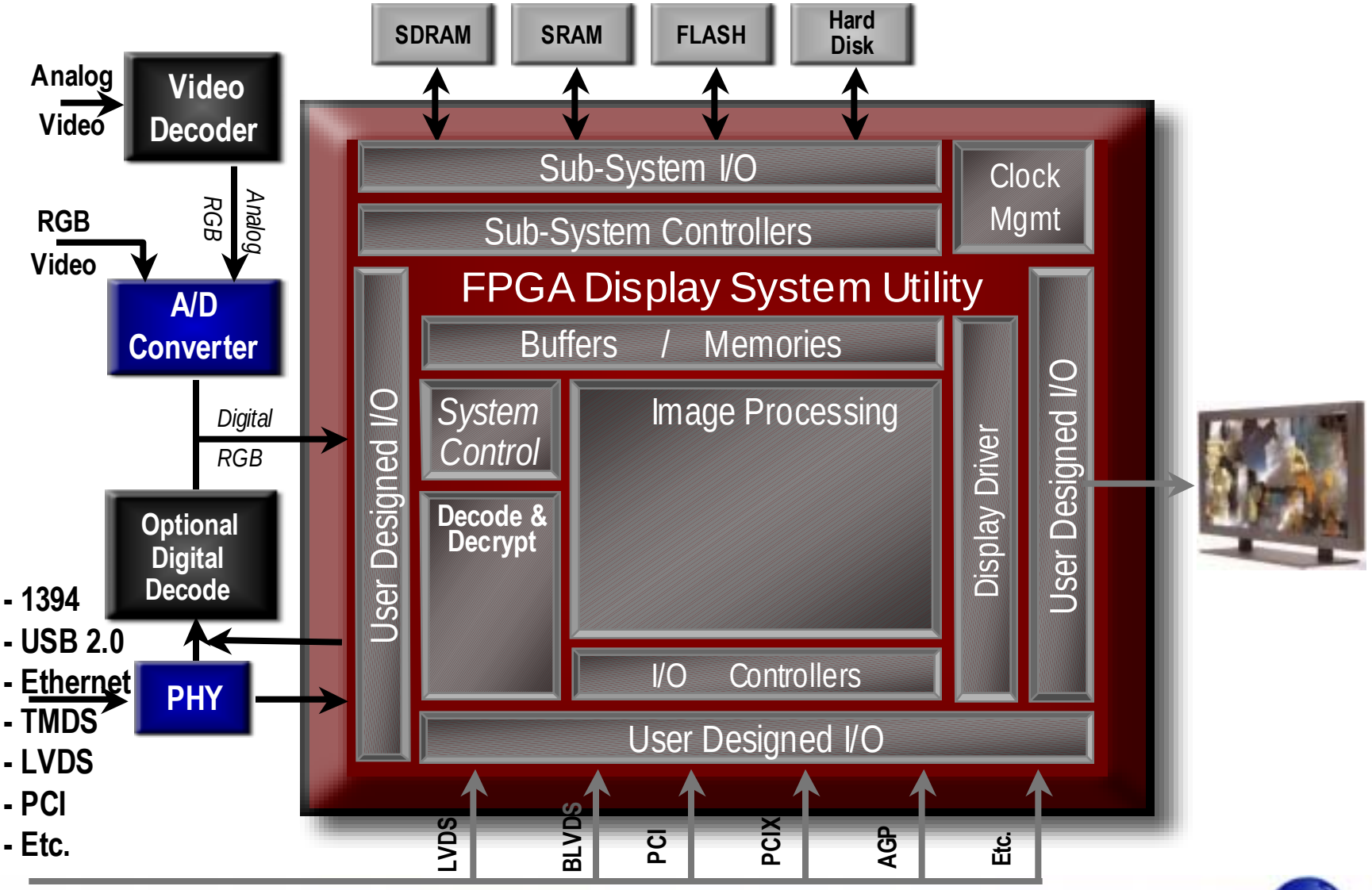
Flat-Panel Display Controller



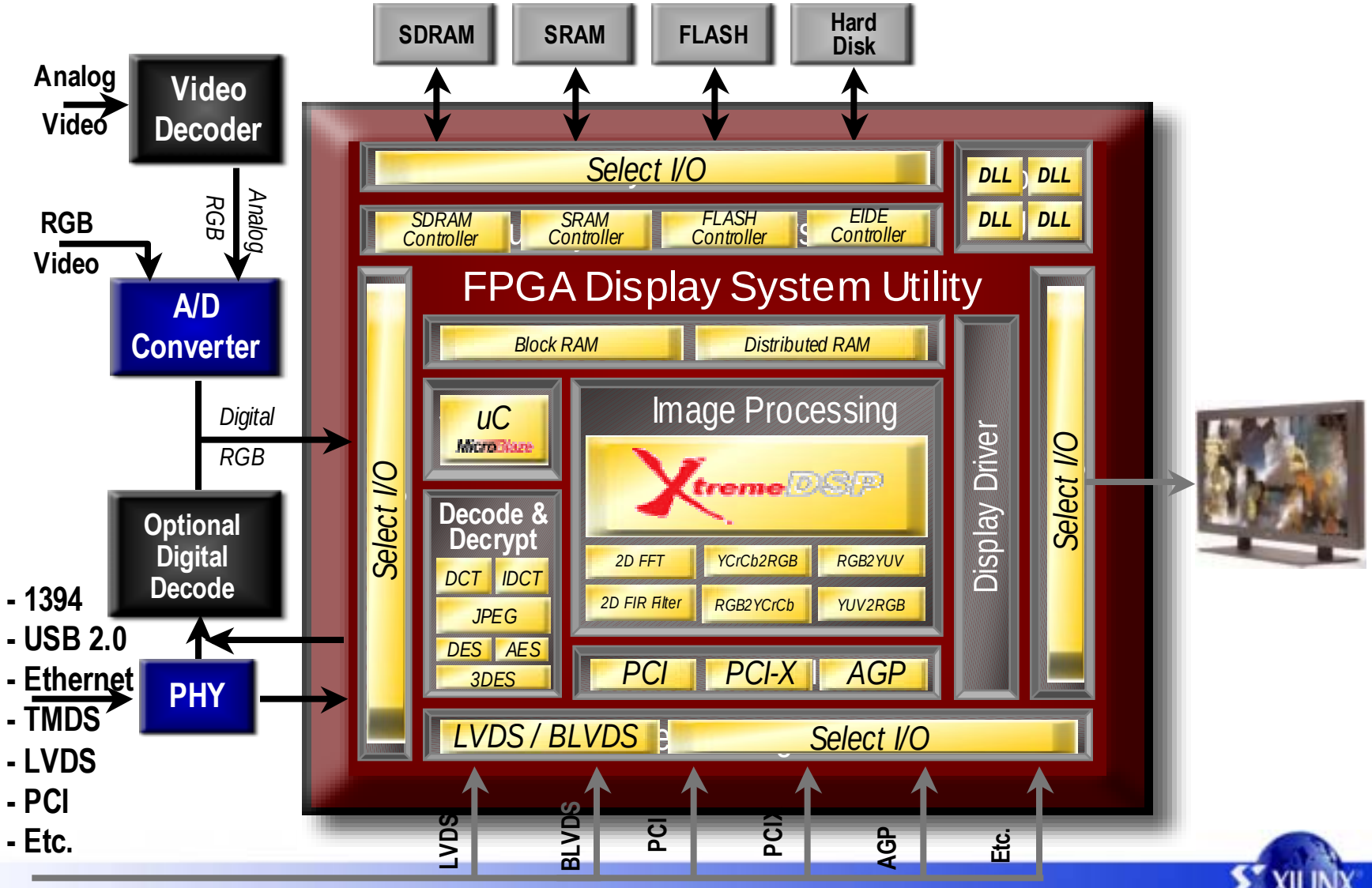
Digital TV System



Display System Design Challenge



FPGA Standard Features and IP
Accelerating Time-to-Market

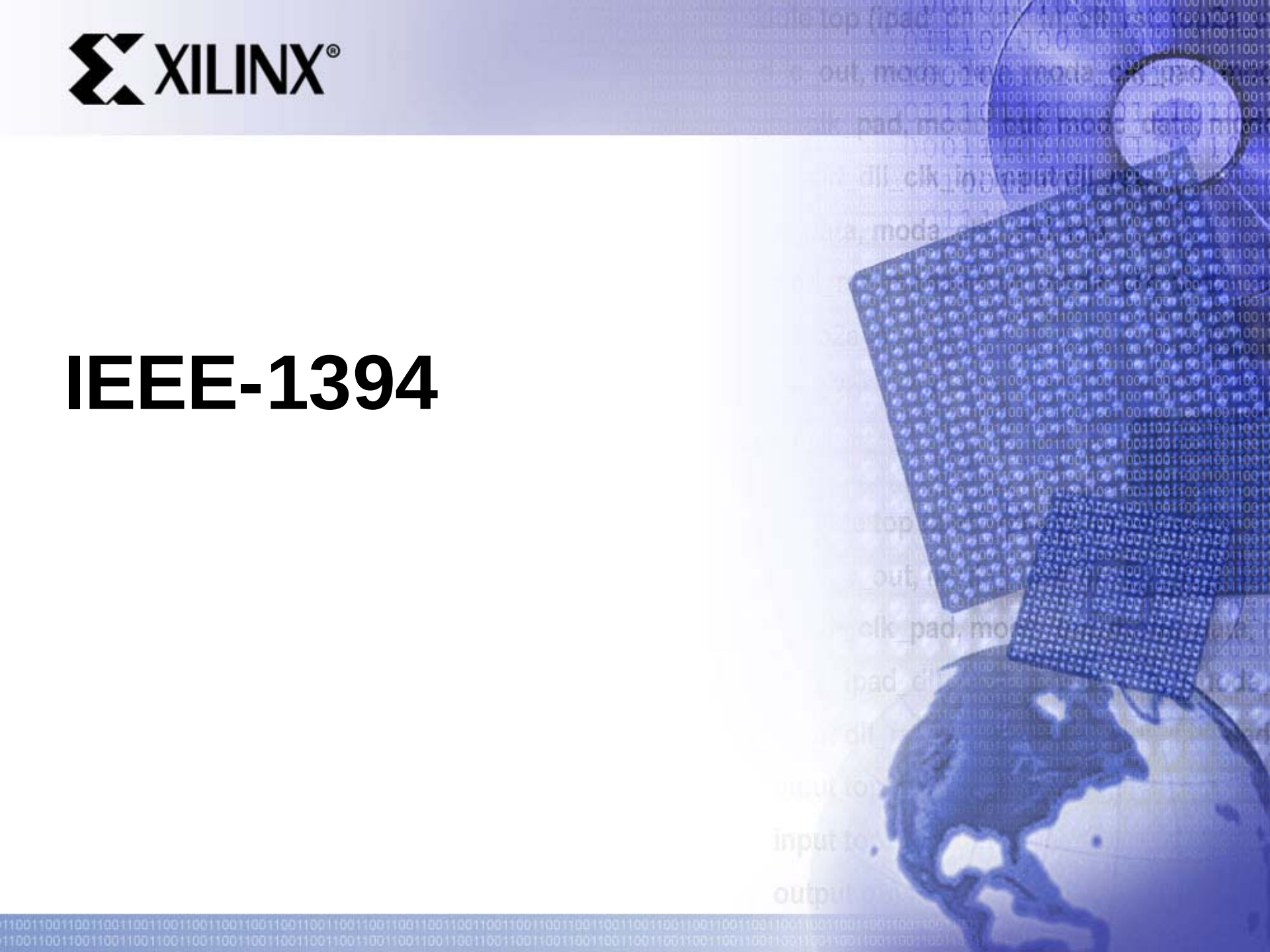


Spartan-IIE Features
Value for Digital Video

Spartan-IIE Silicon Features	Value for Digital Video Applications
FPGA Fabric and Routing, Up to 300,000 System Gates	Performance in excess of 30 billion MACs/second
Delay Locked Loops (DLLs)	Clock multiplication and division, clock mirror, Improve I/O Perf.
System I/O - HSTL-I, -III, -IV	High-speed SRAM interface
System I/O - SSTL3-I, -II; SSTL2-I, -II	High-speed DRAM interface
System I/O - GTL, PCI, AGP	Chip-to-Backplane, Chip-to-Chip interfaces
Differential Signaling - LVDS, Bus LVDS, LVPECL	Bandwidth management (saving the number of pins), reduced power consumption, reduced EMI, high noise immunity
SRL-16	16-bit Shift Register ideal for capturing high-speed or burst-mode data and to store data in DSP applications
Distributed RAM	DSP Coefficients, Small FIFOs
Block RAM	Video Line Buffers, Cache Tag Memory, Scratch-pad Memory, Packet Buffers, Large FIFOs

XILINX®

IEEE-1394



IEEE-1394 & Multimedia Industry

- 1394 is the lowest-cost digital interface available for audio/video applications
- New audio/video applications are the primary market for IEEE-1394
  - Digital Television (DTV)
  - Multimedia CDROM (MMCD)
  - Home Networks
- IEEE-1394 has been accepted as the standard digital interface by the Digital VCR Conference

Why IEEE-1394?

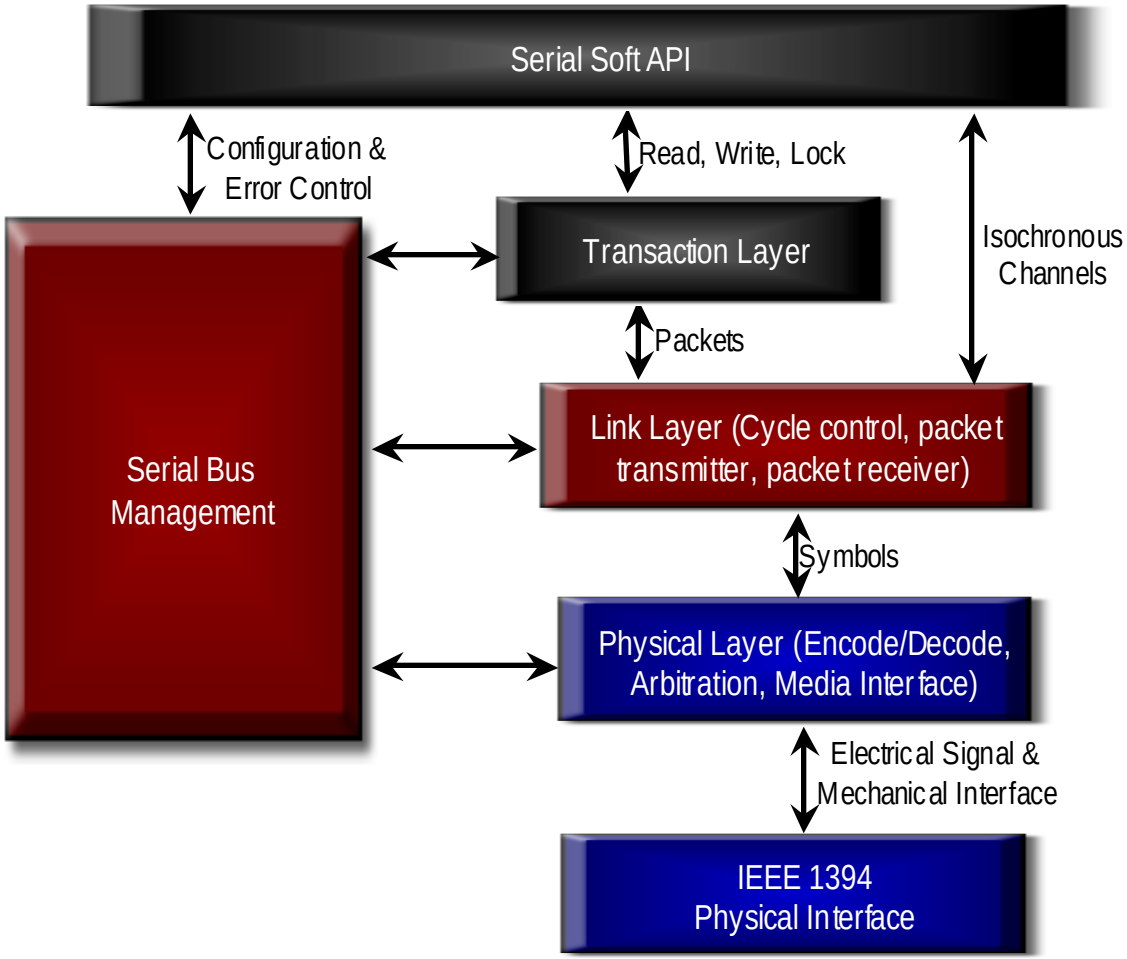
- A hardware and software standard for transporting data at 100, 200, 400, or 800 megabits per second (Mbps)
- A digital interface
  - There is no need to convert digital data into analog and tolerate a loss of data integrity
- Physically small
  - The thin serial cable can replace larger and more expensive interfaces
- Inexpensive and Easy to use
  - There is no need for terminators, device IDs, or elaborate setup

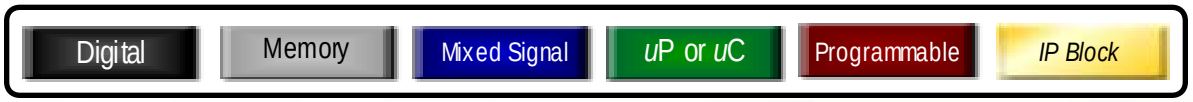
Why IEEE-1394?

- Hot pluggable
  - Users can add or remove 1394 devices with the bus active
- Scaleable architecture
  - May mix 100, 200, and 400 Mbps devices on a bus
- Flexible topology
  - Support of daisy chaining and branching for true peer-to-peer communication
- Non-proprietary
  - There is no licensing problem to use for products

Audio/Video Digital Interface of Choice!

IEEE 1394 Protocol Stack

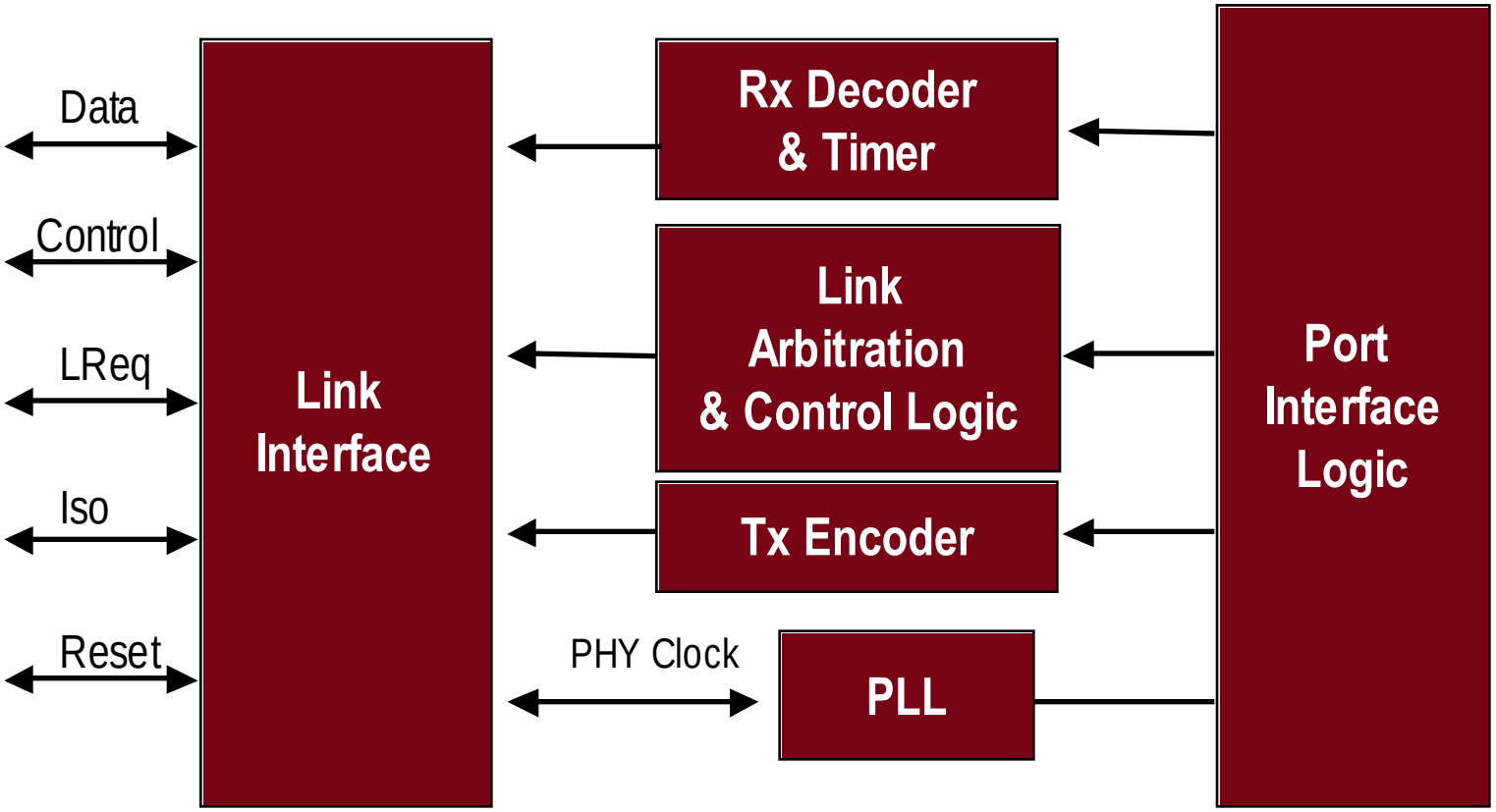




1394 PHY Layer

- The physical layer provides the initialization and arbitration services
  - It assures that only one node at a time is sending data
- The physical layer of the 1394 protocol includes:
  - The electrical signaling
  - The mechanical connectors and cabling
  - The arbitration mechanisms
  - The serial coding and decoding of the data being transferred or received
  - Transfer speed detection

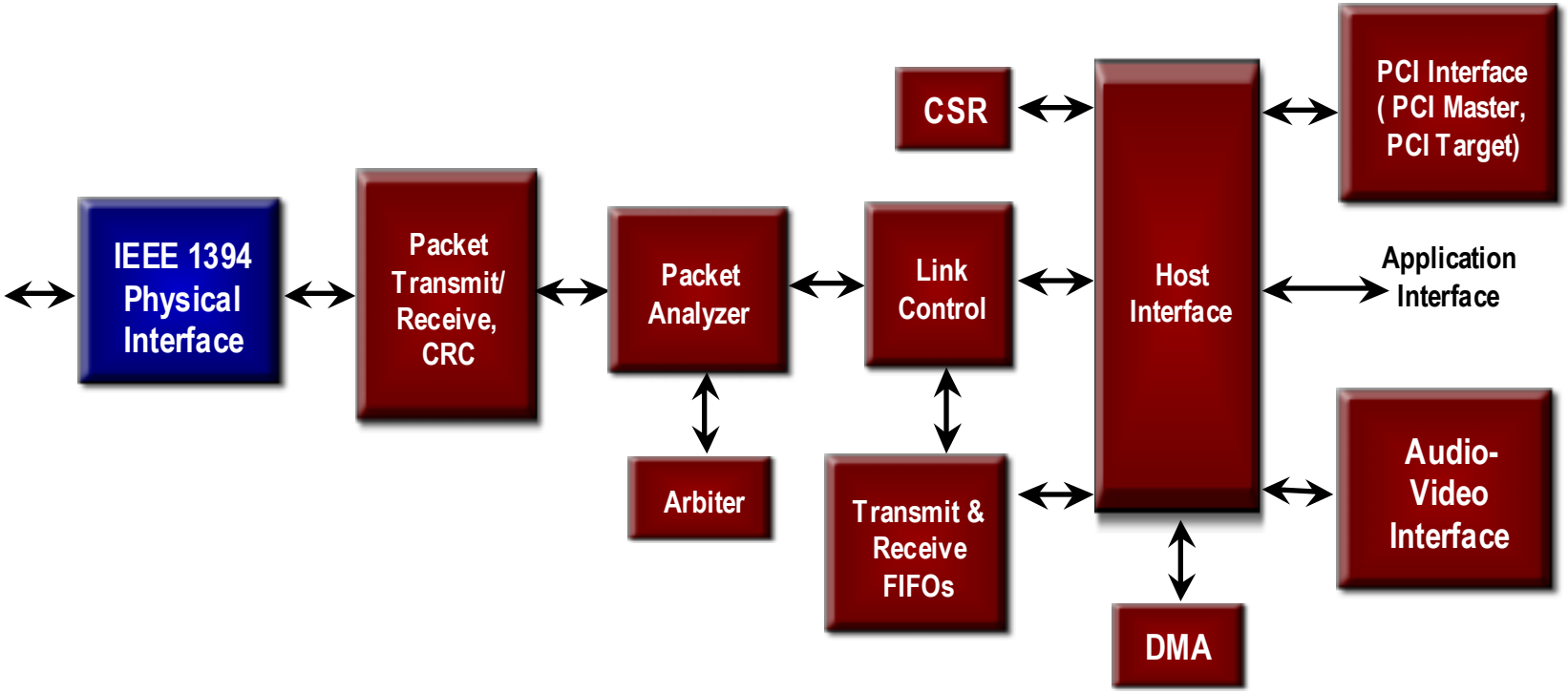
1394 PHY Layer



Link Layer

- Gets data packets on and off the wire
- Does error detection and correction
- Does retransmission
- Handles provision of cycle control for isochronous channels
- The link layer supplies an acknowledged datagram to the transaction layer
  - A datagram is a one-way data transfer with request confirmation

Link Layer

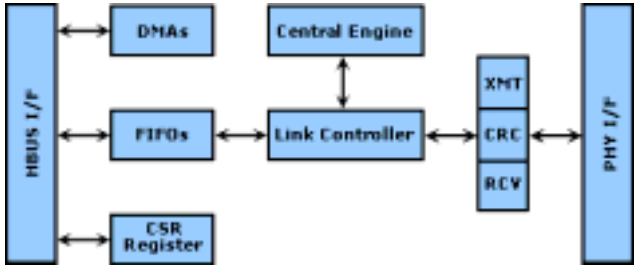


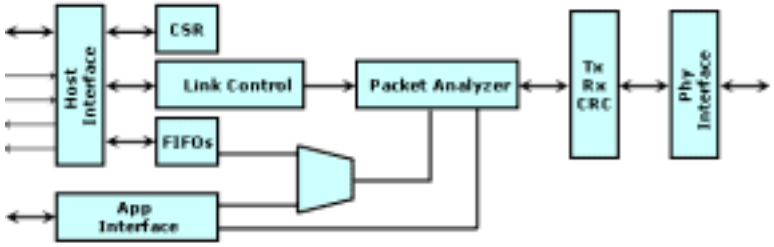
Xilinx FPGAs are ideal for implementing Link Layer Functionality

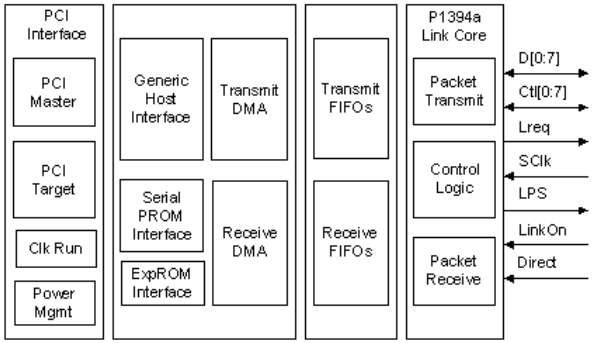
Digital | Memory | Mixed Signal | *u*P or *u*C | Programmable | *IP Block*

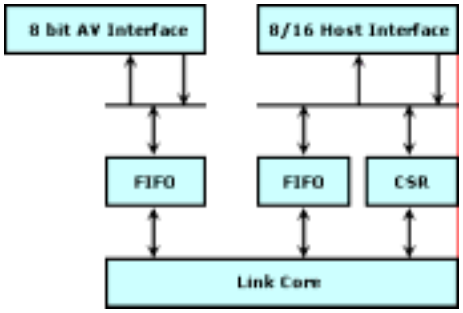
Link Controller IP

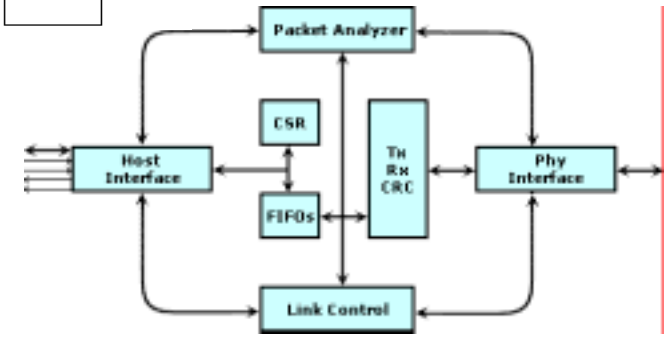
Xilinx Enabled Differentiation

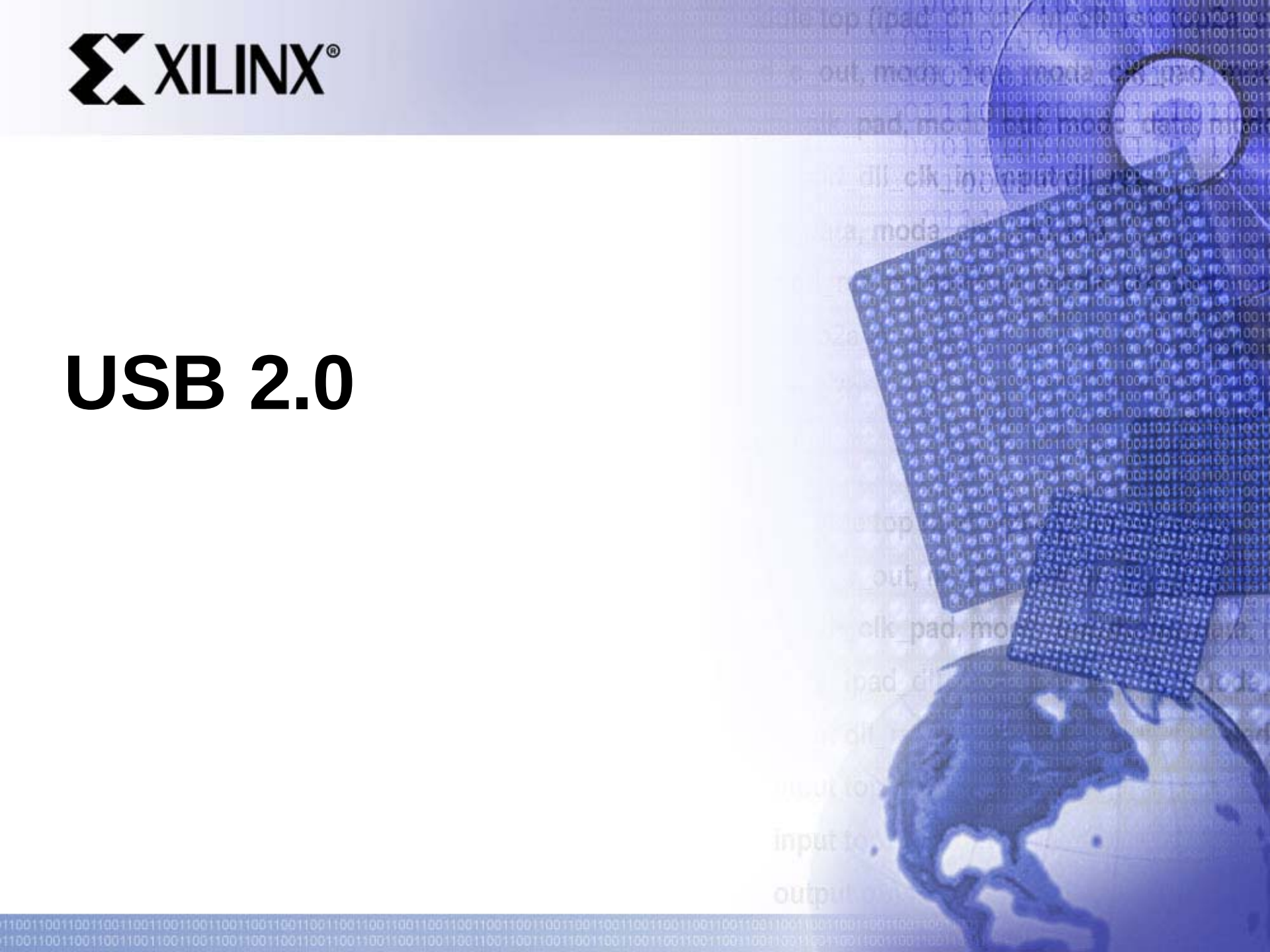






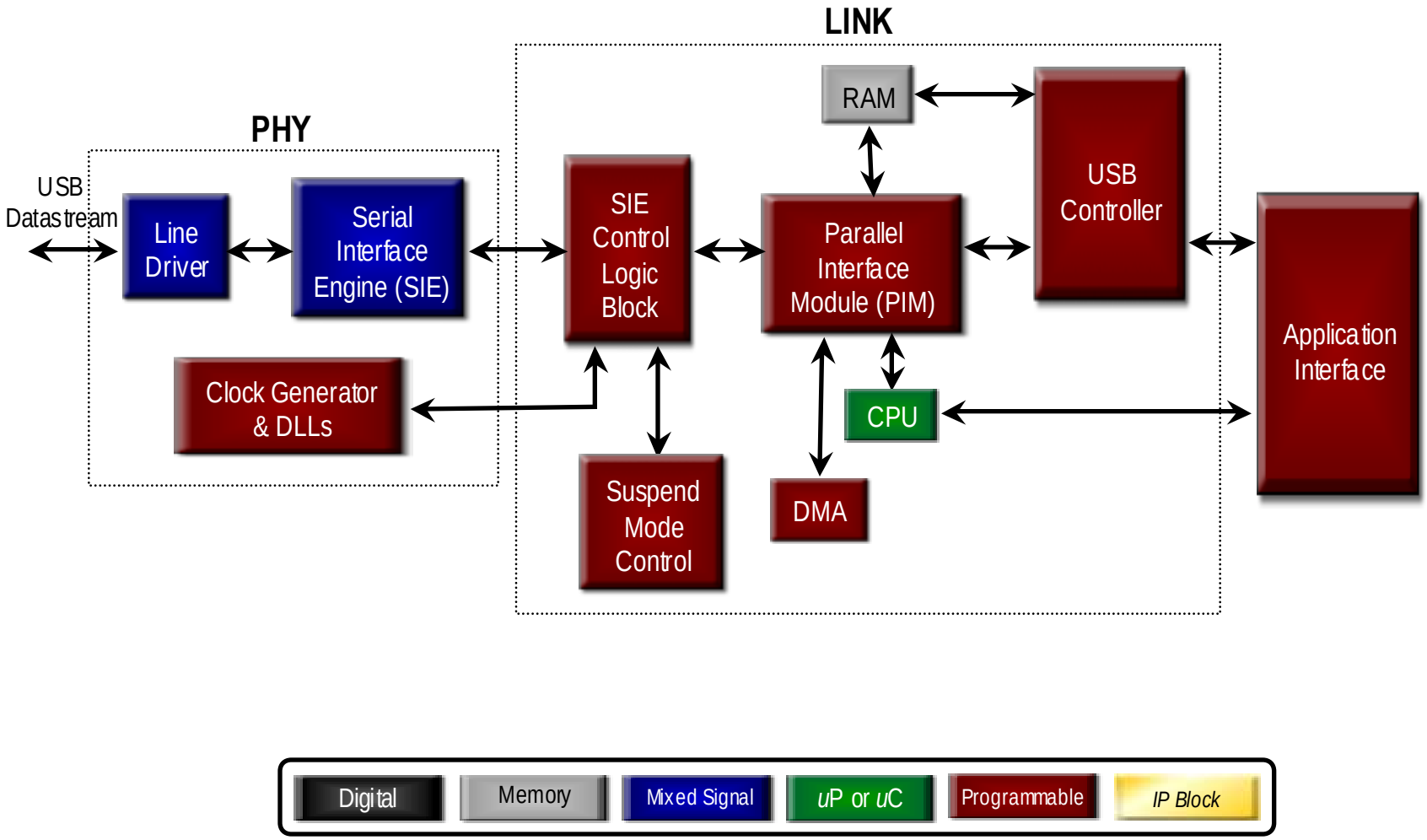




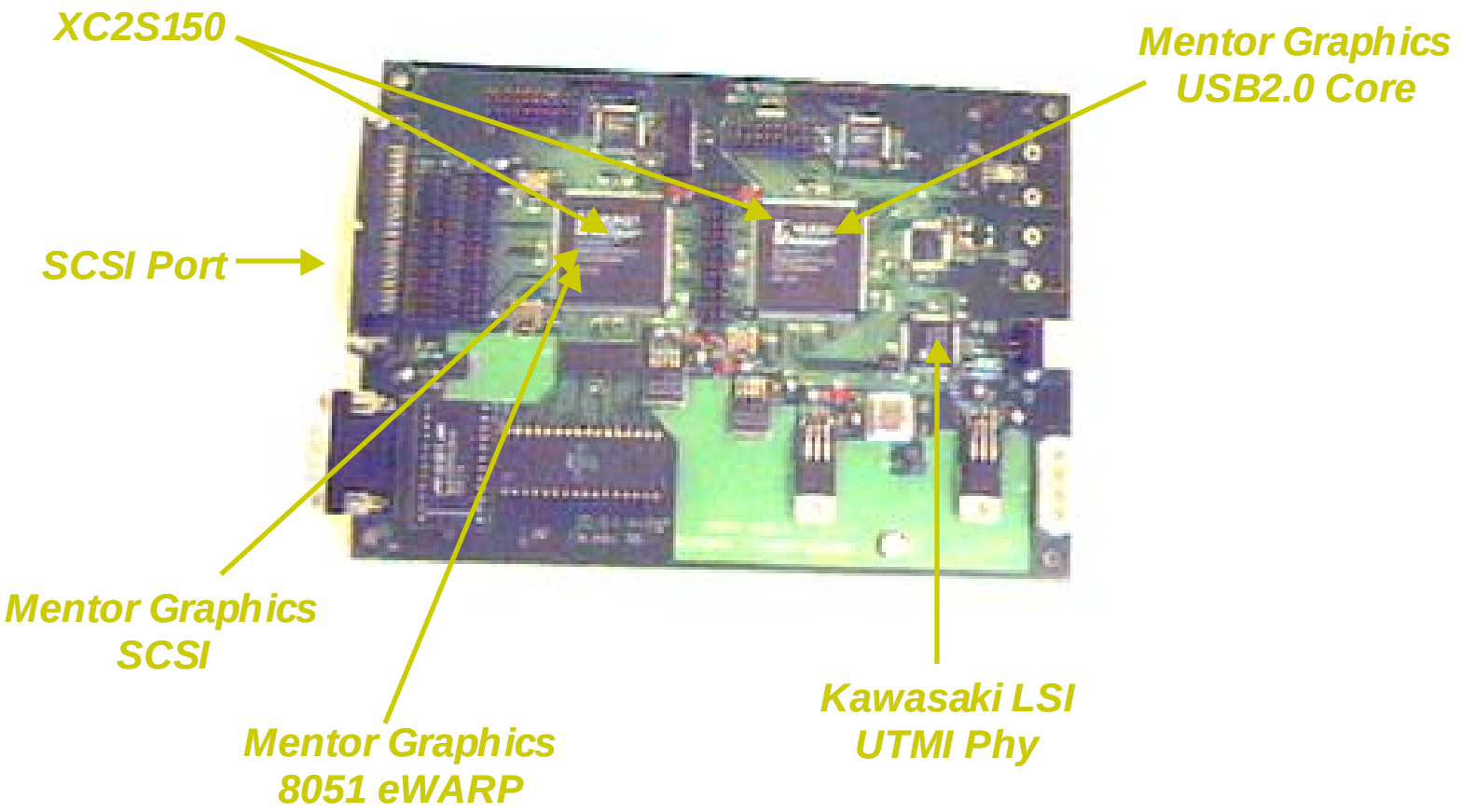


USB 2.0

USB 2.0 IP Core



The Xilinx USB 2.0 Solution



First USB 2.0 Mass Storage Reference Design

The Xilinx USB 2.0 Solution

- Kawasaki LSI, Mentor Graphics and Xilinx have partnered and developed the industry's first UTMI-compliant USB 2.0 upgradable reference design
  - Provides a USB 2.0 to SCSI technology bridge, and can be used to provide end-to-end high-bandwidth data storage
    - For hard disk drives, CD writers, DVD ROMs, etc.
  - Flexible and upgradable USB 2.0 technology bridge to multiple home networking standards
    - Such as HomePNA, HomePlug, HomeRF, IEEE-1394, IEEE 802.11b

DVI

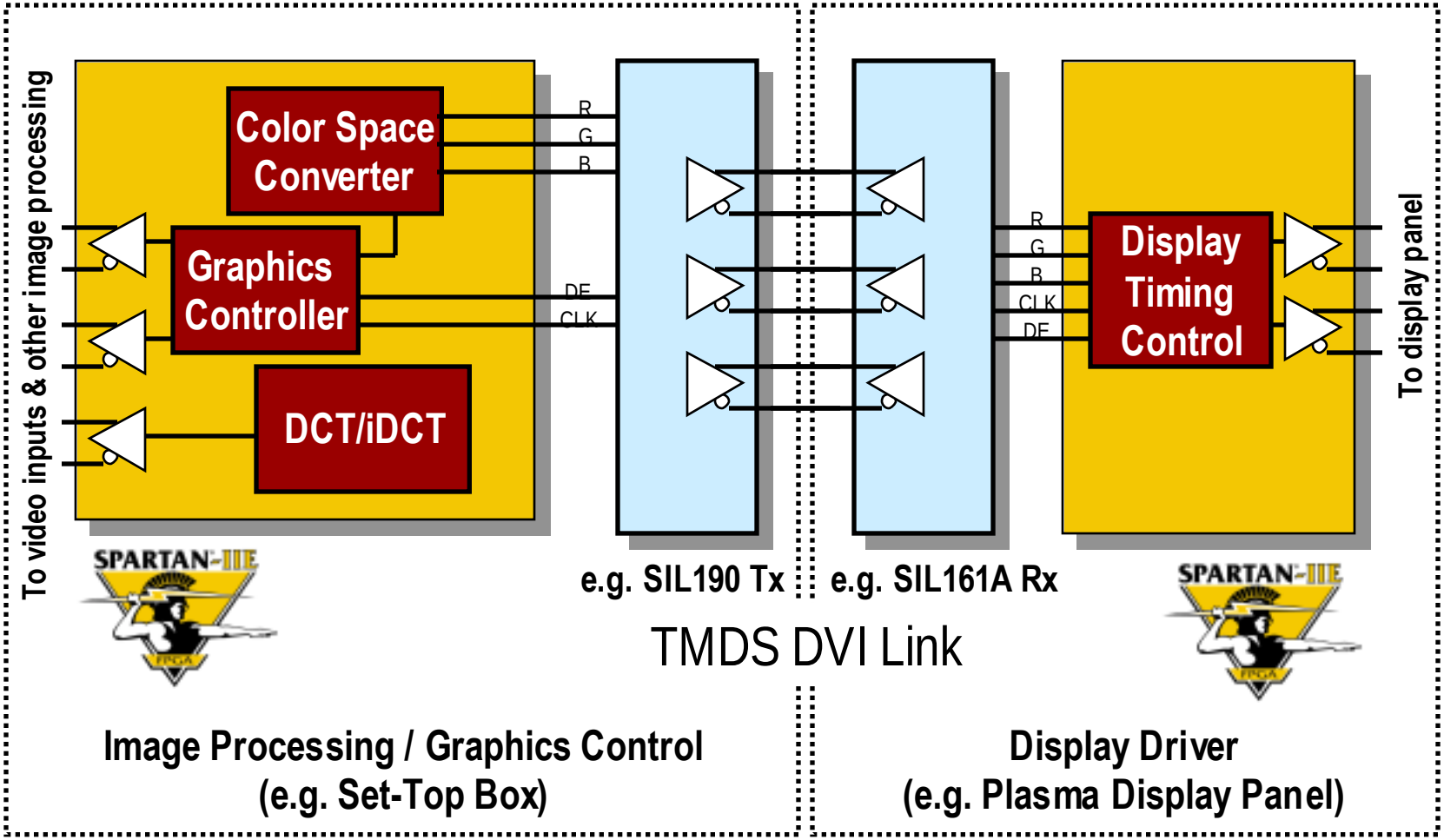
DVI Overview

- Interface to link digital graphics sources to digital displays
- One-way link supporting uncompressed HDTV signals
- Removes an unnecessary analog-digital-analog conversion step (current methods) - enables pure digital signal to display
- Based on Transition Minimized Differential Signalling (TMDS)
- Developed and promoted by the Digital Display Working Group (DDWG)

DVI & IEEE-1394

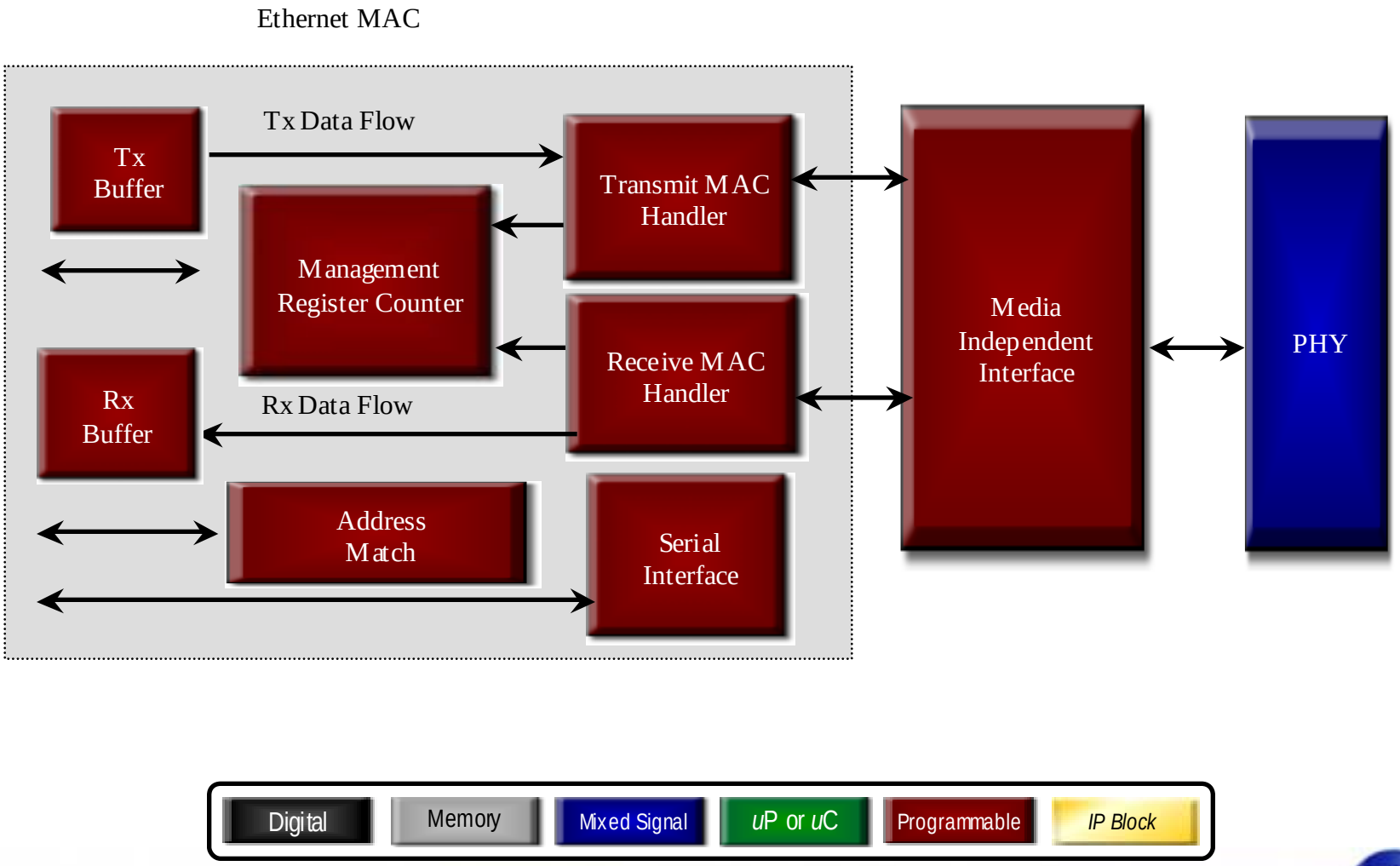
	Stream	Bit Rate	Architecture	Command & Control	Applications
IEEE-1394	Compressed MPEG-2 Transport	1394: 100, 200, or 400 Mbps, Scalable 1394b: 800 Mbps to 3.2 Gbps, Scalable	Peer-to-peer	Support for AV command & control	Storage, networking
DVI	Uncompressed baseband	Single link DVI: 4.9 Gbps Double link DVI: 9.9 Gbps	Point-to-point	No support for AV command & control	Digital interface between a graphics chip and a monitor

Xilinx in Example DVI System



Fast Ethernet

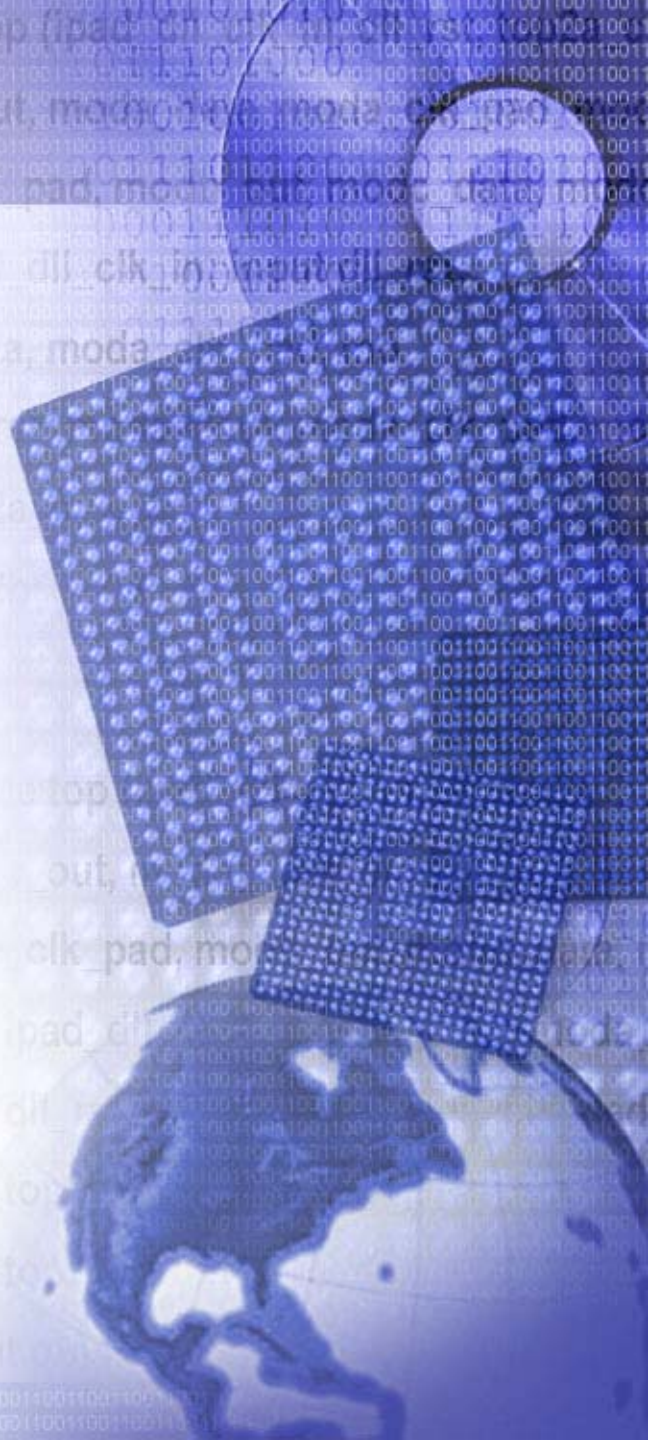
Fast Ethernet PHY and MAC



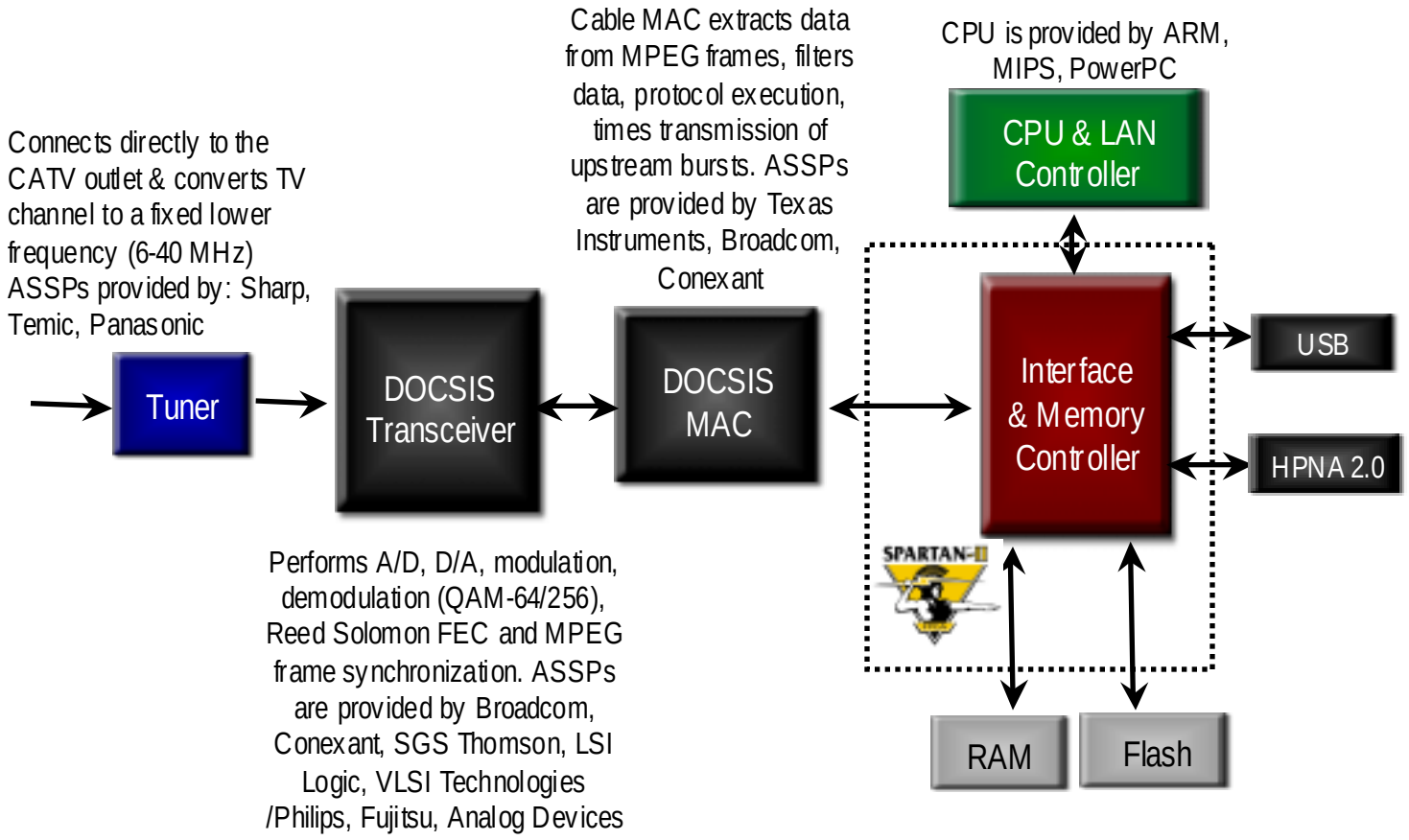
Ethernet & Home Networking

- For the home networking purists, Ethernet equipment offers cheap, proven, and mature products
- The Ethernet market is second behind the phoneline technology
- Cahners In-Stat Group expects that Ethernet technology will be deployed in 30% of home networking units shipped
- Distribution of video for entertainment applications requires larger bandwidth
  - MPEG 2 (used in HDTV) requires between 24 to 35Mbps
    - Fast Ethernet delivers video data at 100Mbps

Cable Modem I/F



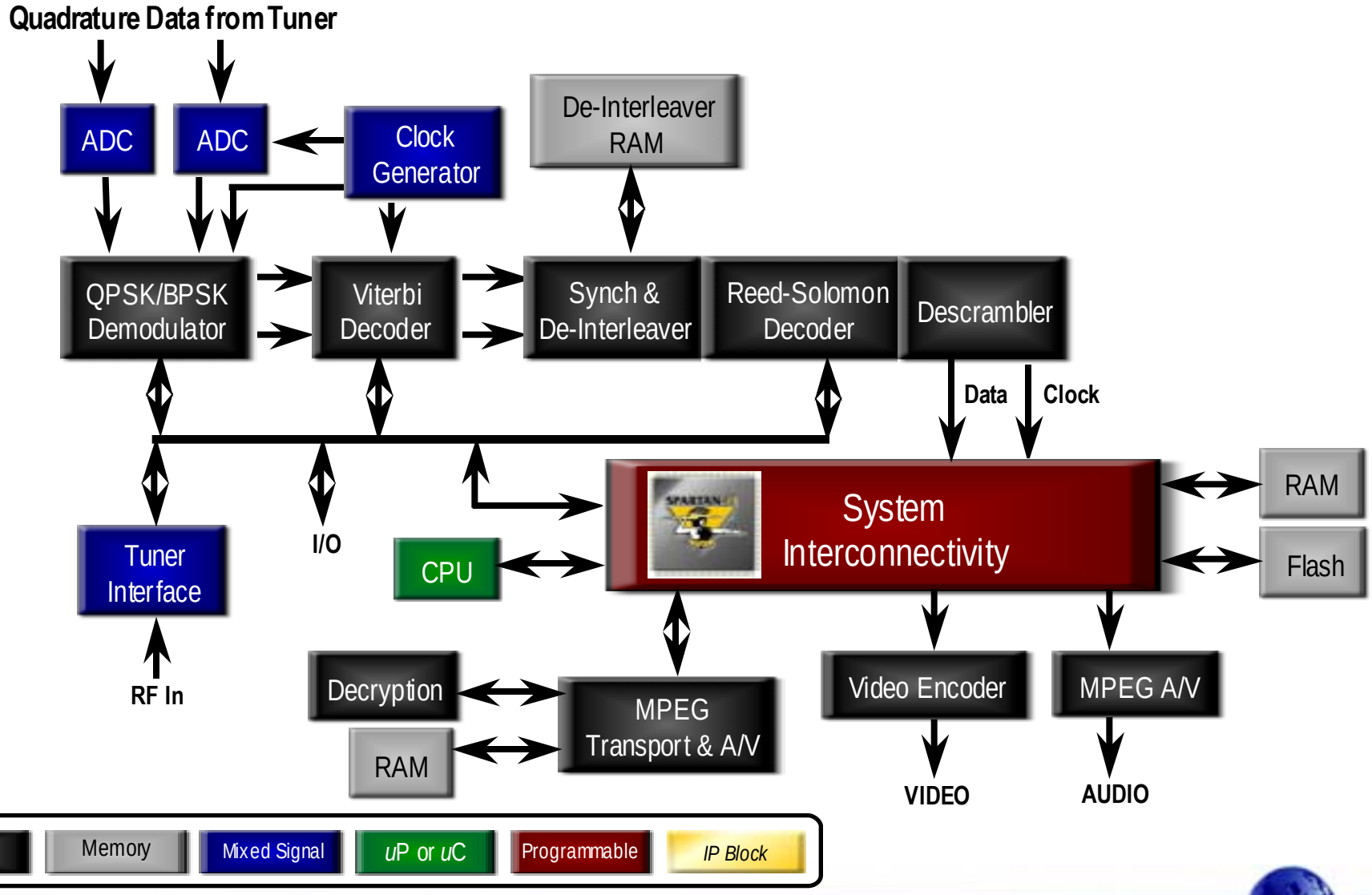
Cable Modem - Block Diagram



Digital | Memory | Mixed Signal | *u*P or *u*C | Programmable | *IP Block*

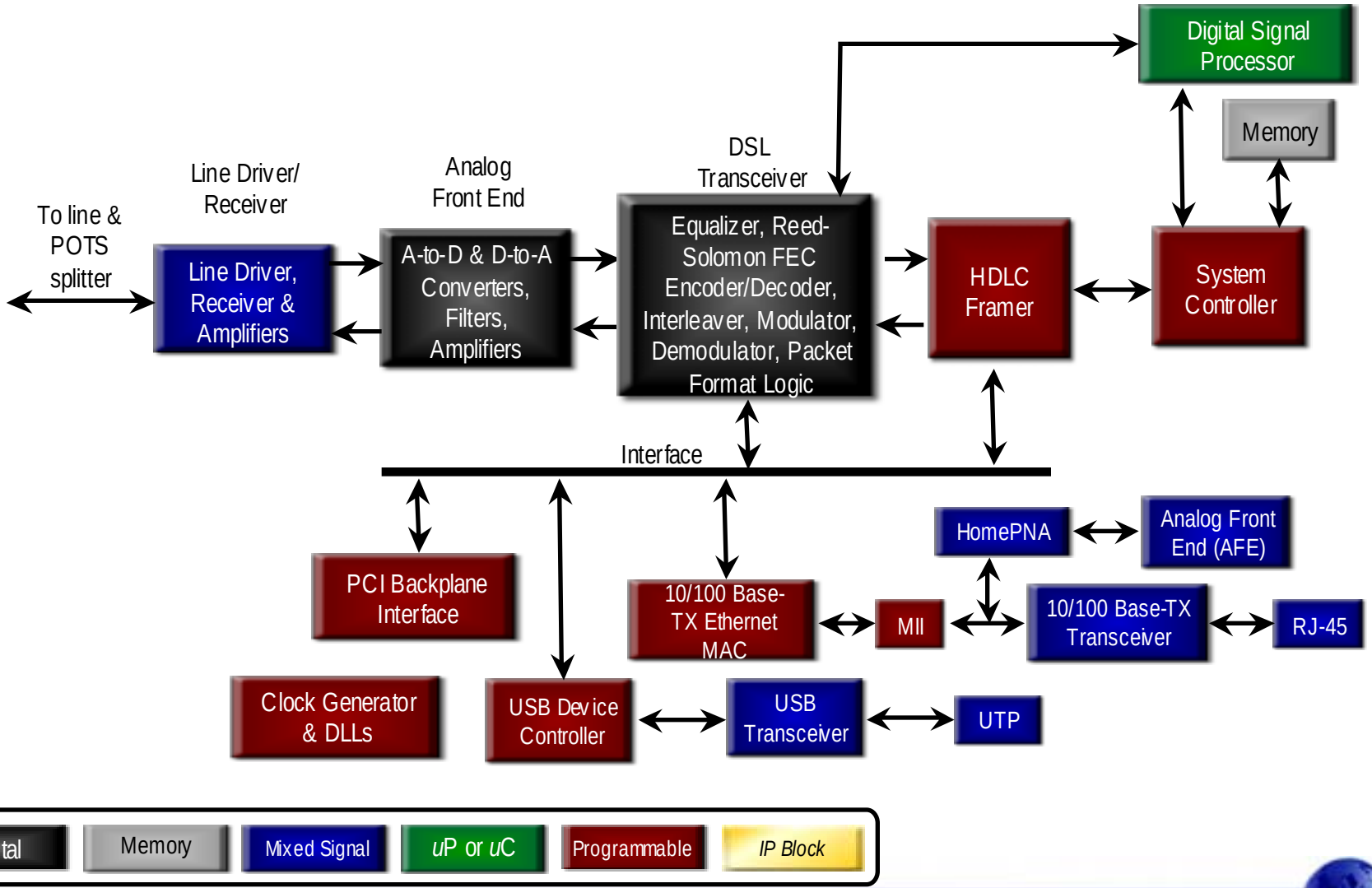
Satellite Modem I/F

Satellite Modems

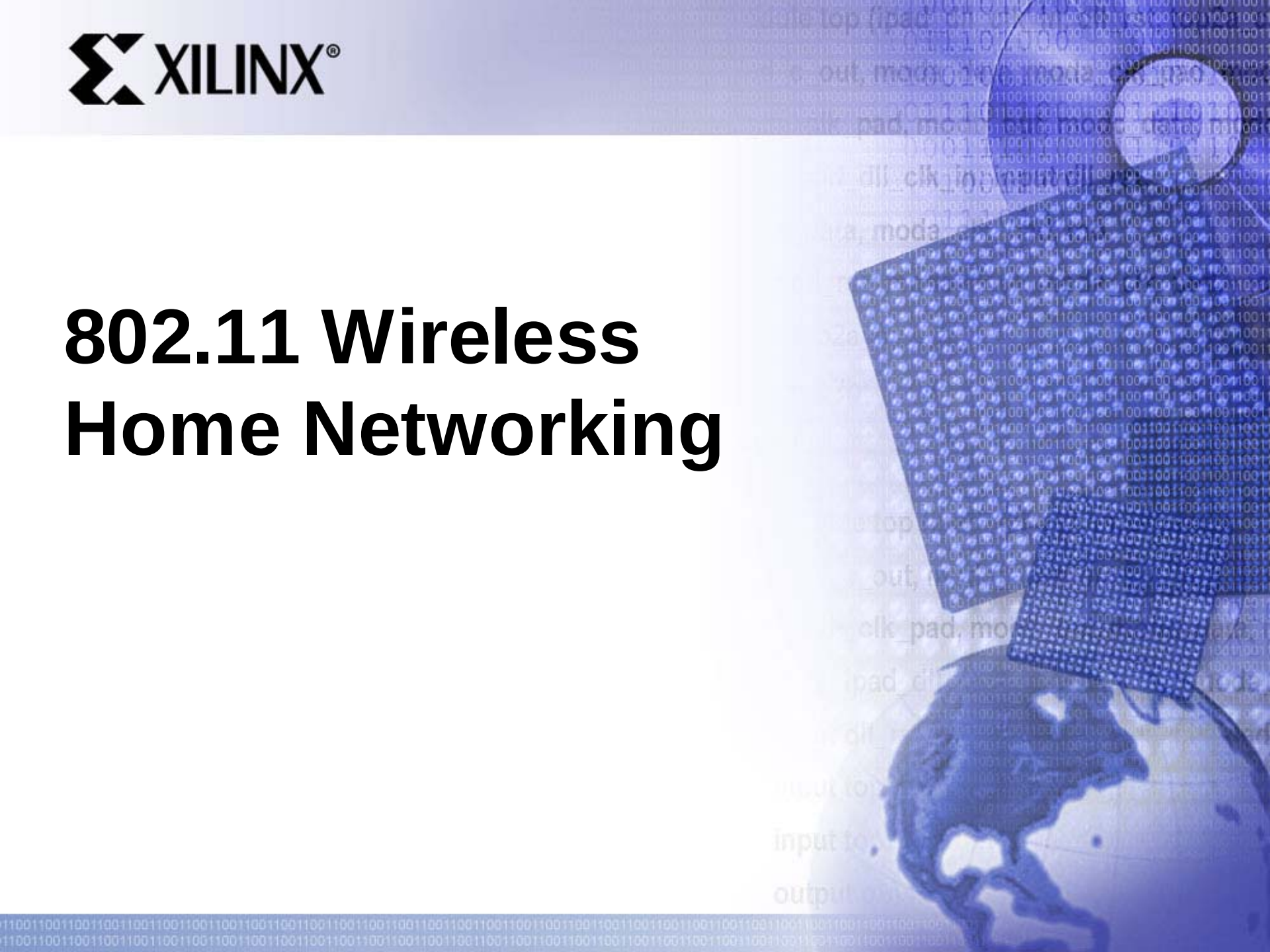


xDSL Modem I/F

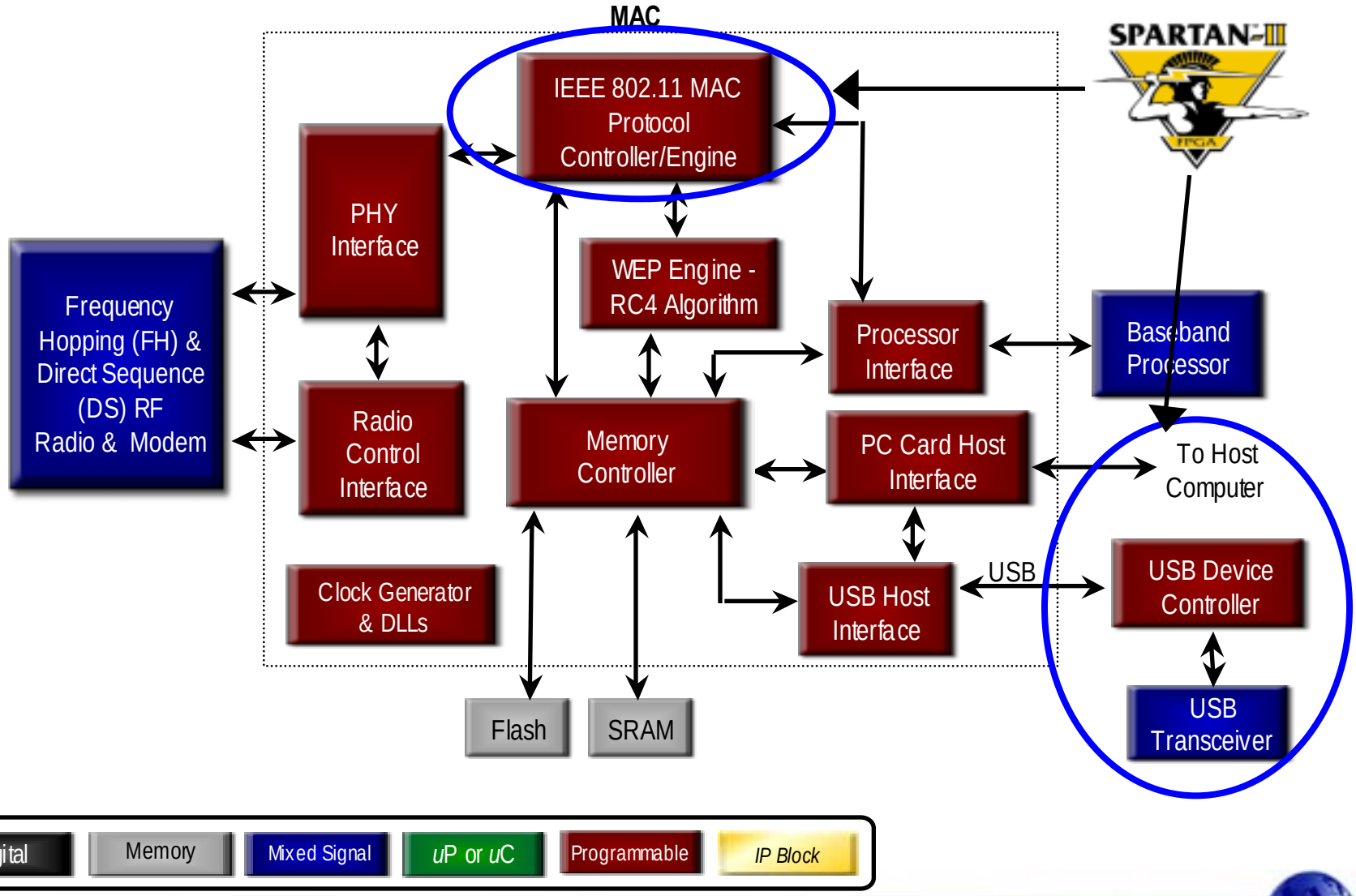
DSL CPE
(Customer Premise Equipment)



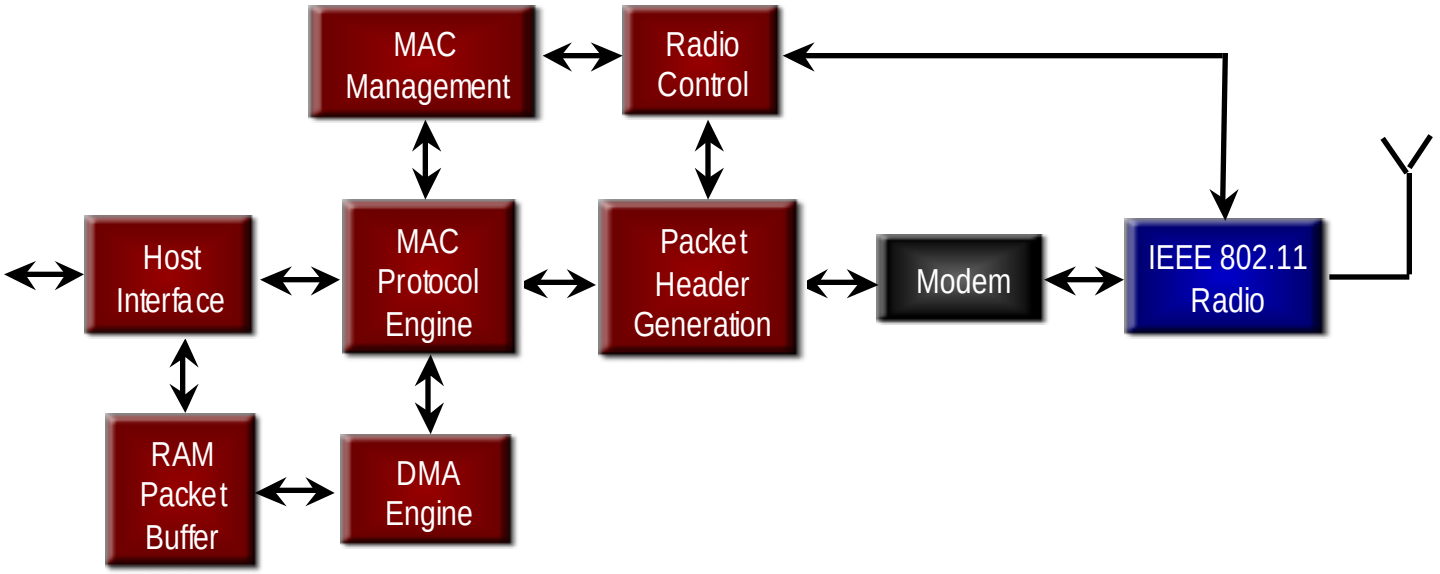
802.11 Wireless Home Networking



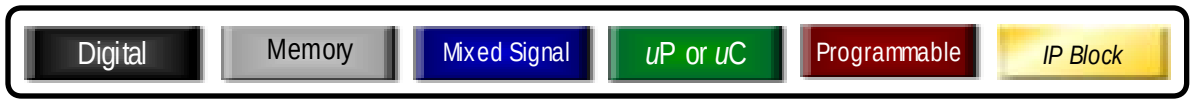
IEEE 802.11b/a MAC



Wireless LAN PC/NIC Card



Cardbus to WLAN (IEEE 802.11b) Baseband Controllers in NIC Cards



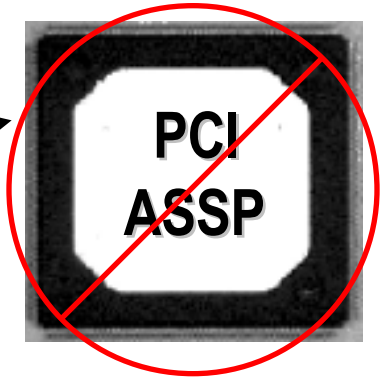
PCI

PCI - Concept

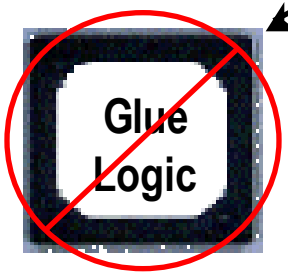
- PCI
  - Peripheral Component Interconnect
  - Originated in the PC industry
  - High performance bus that provides a processor independent data path between the CPU and high-speed peripherals
  - Robust interconnect mechanism developed to relieve the I/O bottlenecks

ASSP Replacement & Integration

System & Memory Controllers,
DLLs, Level Translators ($20)

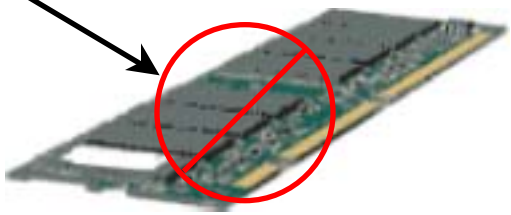


Standard Chip
PCI Master I/F ($15)



External PLD
PCI Master I/F ($5)

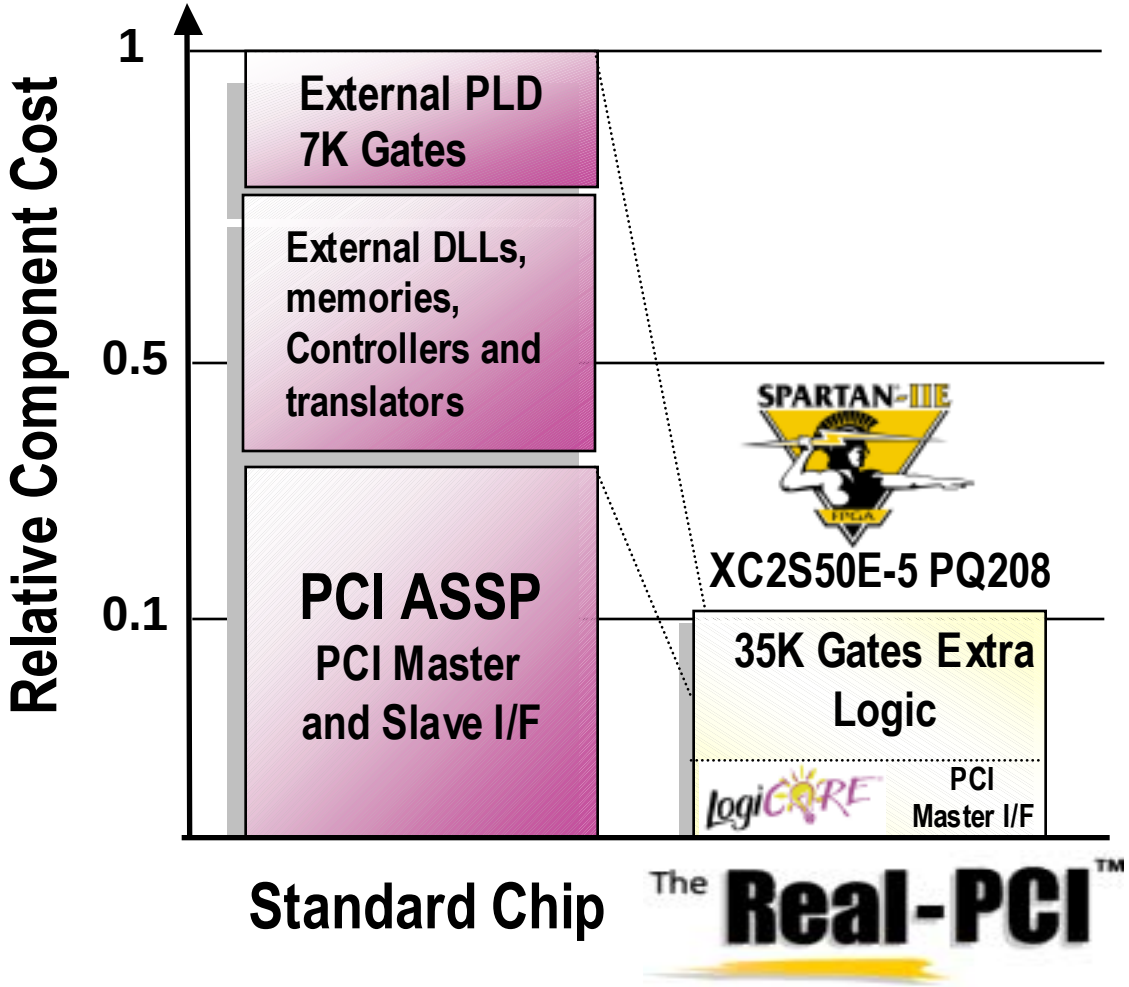
The **Real-PCI**™



Memory ($9)

*Supported Devices
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E

PCI - A Successful Programmable Solution



Xilinx PCI

Spartan-IIE FPGAs Lower Overall System Cost

Spartan-IIE PCI Solutions

Spartan-IIE Device	PCI Core	Speed	Available User Logic (system gates)	Available BlockRAM bits
2S50E	PCI32	33 MHz 66 MHz*	30-35K	32,768
2S100E	PCI32	33 MHz 66 MHz*	70-75K	40,960
2S150E	PCI32 PCI64	33 MHz 66 MHz	130-135K	49,152
2S200E	PCI32 PCI64	33 MHz 66 MHz	180-185K	57,344
2S300E	PCI32 PCI64	33 MHz 66 MHz	280-285K	65,536

* PCI32: 66 MHz design available using Xilinx XPERTs or Design Services

Customer Benefits

- Reduces cost over PCI ASSPs
  - Cost savings of more than 50%
- Integrate and replace system functions
  - PLL/DLL clock management devices
  - SSTL-3/HSTL translators
  - Backplane logic and drivers
  - External memory devices
  - System & cache controllers
- Significant time-to-market advantage

LVDS

Spartan-IIE LVDS Support

- All IOBs have LVDS/BLVDS/LVPECL capability
- IOBs configured as LVDS can be
  - Synchronous or asynchronous
  - Input or output
- Two IOBs (pair) form one LVDS signal
  - One IOB will function as + or P
  - The other IOB will function as - or N.
- LVDS pin pairs are indicated in the datasheet
- Maximum number of LVDS pin-pairs: 120

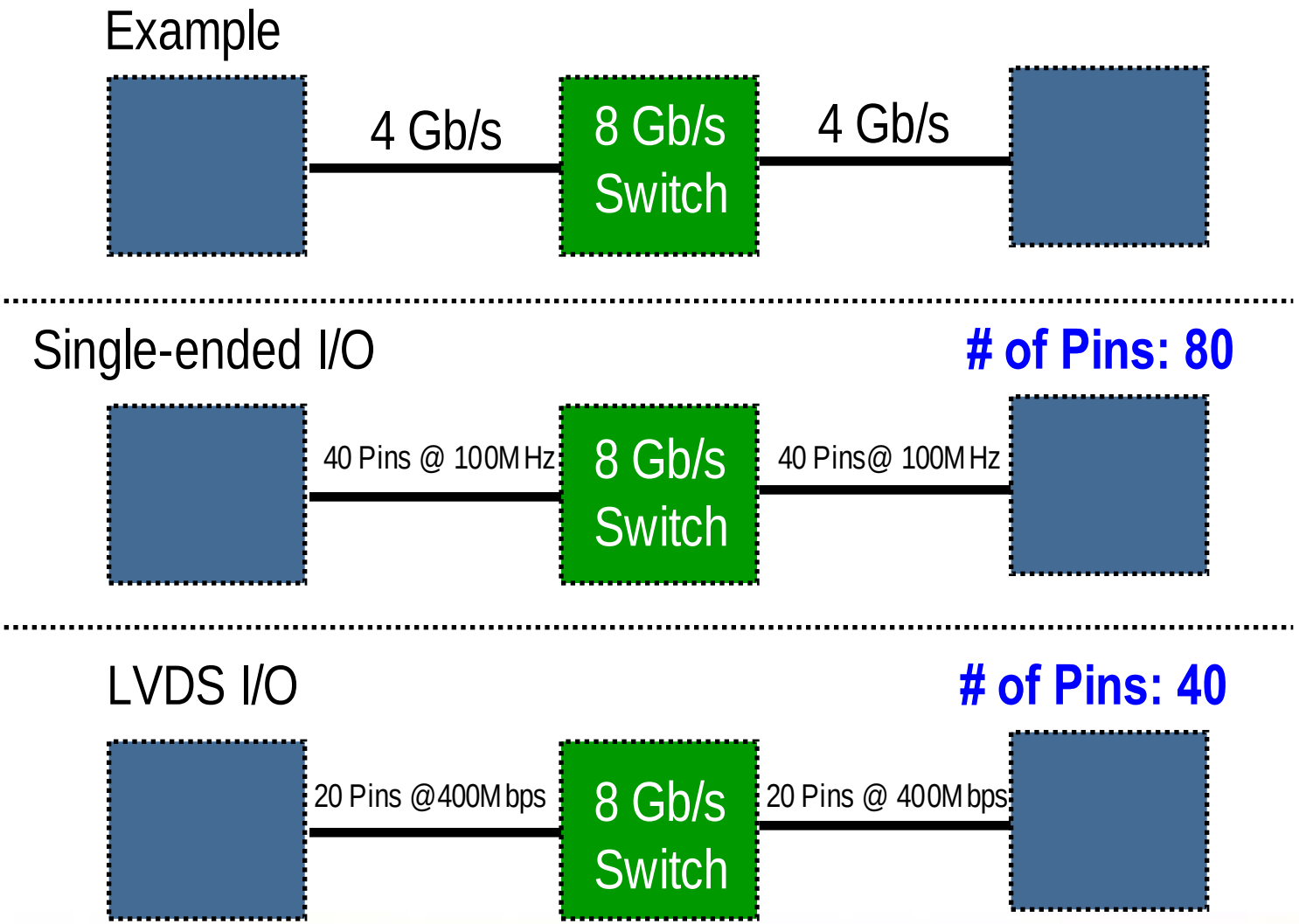
What is LVDS?

- LVDS - Low Voltage Differential Signaling
- LVDS is a differential signaling interconnect technology
  - Requires two pins per channel
- LVDS was first used as a interconnectivity technology in laptops and displays to alleviate EMI issues
- Technology is now widely used
  - A broad spectrum of telecom and networking applications
  - Mainstream consumer applications like digital video and displays

LVDS benefits - Low EMI

- Low voltage swing (~350mV)
- Slow edge rates compared to other technologies (1V/ns)
- Current mode of operation ensures low ICC spikes
- High noise immunity
  - Switching noise cancels between the two lines
  - Data is not affected by the noise
    - External noise affects both lines, but the voltage difference stays about the same

LVDS Benefits - Save # of Pins



LVDS Advantages - Low Power

- LVDS technology saves power in several important ways
- Power dissipation at the terminator is ~1.2 mW
  - RS-422 driver delivers 3 V across a termination of 100 Ω, for 90mW power consumption... 75 times more than LVDS!
- Due to the current mode driver design, the frequency component of ICC is greatly reduced
  - Compared to TTL / CMOS transceivers where the dynamic power consumption increases exponentially with the frequency

LVDS Benefits - Low Cost

- LVDS does not need specialized board and connectors to achieve high performance
  - Standard off-the-shelf components and FR-4 material
- Low power technology
  - Savings in fans, power supplies etc.
  - Less components, hence higher system reliability
- EMI Compliance
  - Significantly lower EMI issues compared to other technologies
  - Cost savings in obtaining EMI compliance for products

LVDS Mux/Demux Benefits - Lowers Cost Even More

- Mux/Demux multiple TTL signals into a high data rate LVDS channel
- Significant cost benefits
  - less # of pins to achieve certain bandwidth requirement
  - Less number of traces on PCB = Lower board cost
    - Less number of PCB layers required to route signals
    - Less board area required
  - Lower connector cost
  - Lower EMI, crosstalk, reflection, noise issues
    - EMI compliance and signal integrity issues are less of a problem

LVDS Advantages

Advantages	LVDS	PECL	Optics	RS-422	GTL	TTL
Data rate up to 1Gbps	+	+	+	-	-	-
Very low skew	+	+	+	-	+	-
Low dynamic power	+	-	+	-	-	-
Cost effective	+	-	-	+	+	+
Low noise/EMI	+	+	+	-	-	-
Single power supply/reference	+	-	+	+	-	+
Migration path to low voltage	+	-	+	-	+	+
Simple termination	+	-	-	+	-	+
Wide common-mode range	-	+	+	+	-	-
Process independent	+	-	+	+	+	+
Allows integration w/digital	+	-	-	-	+	+
Cable breakage/splicing issues	+	+	-	+	+	+
Long distance transmission	-	+	+	+	-	-
Industrial temp/voltage range	+	+	+	+	+	+

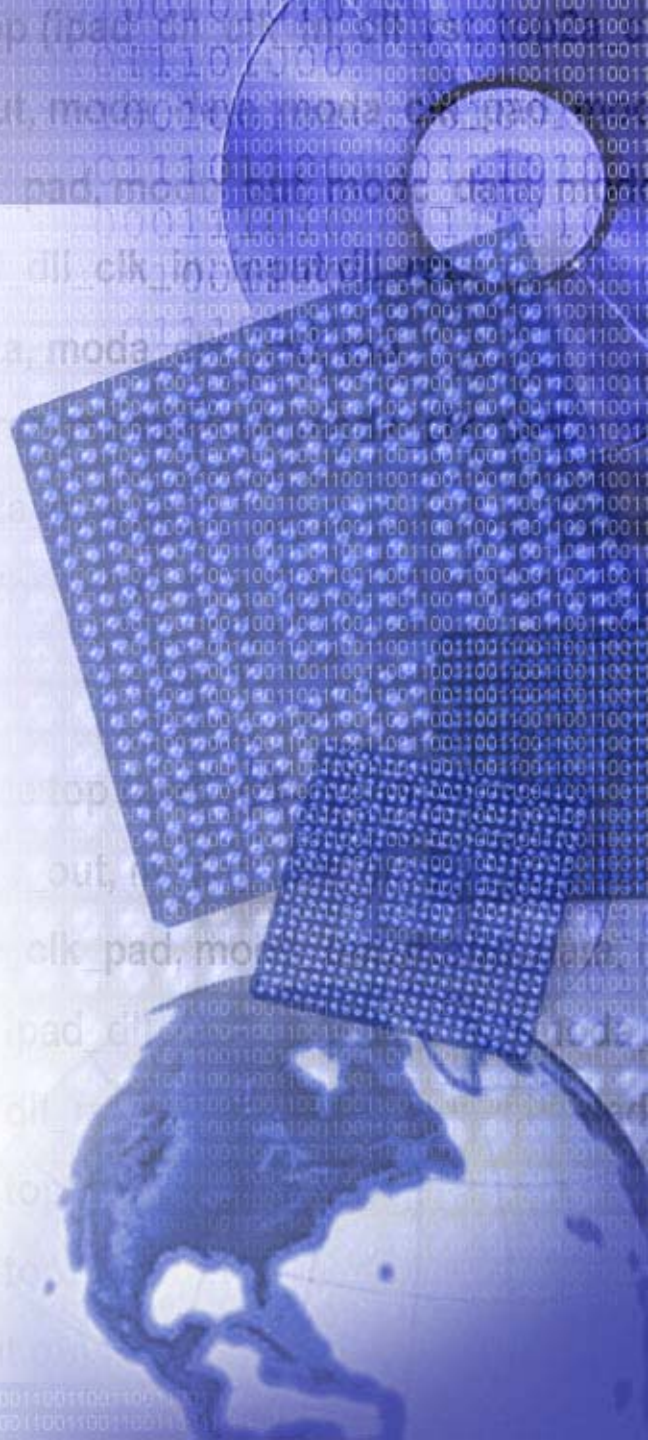
Courtesy: National Semiconductor

Spartan-IIE Differential I/O Counts

	TQ144		PQ208		FT256		FG456	
Device	User	Diff	User	Diff	User	Diff	User	Diff
XC2S50E	102	28	146	50	182	84		
XC2S100E	102	28	146	50	182	84	202	86
XC2S150E			146	50	182	84	263	114
XC2S200E			146	50	182	84	289	120
XC2S300E			146	50	182	84	329	120

User = Maximum number of user I/Os available
Diff = Maximum number of differential paired I/Os available

Forward Error Correction



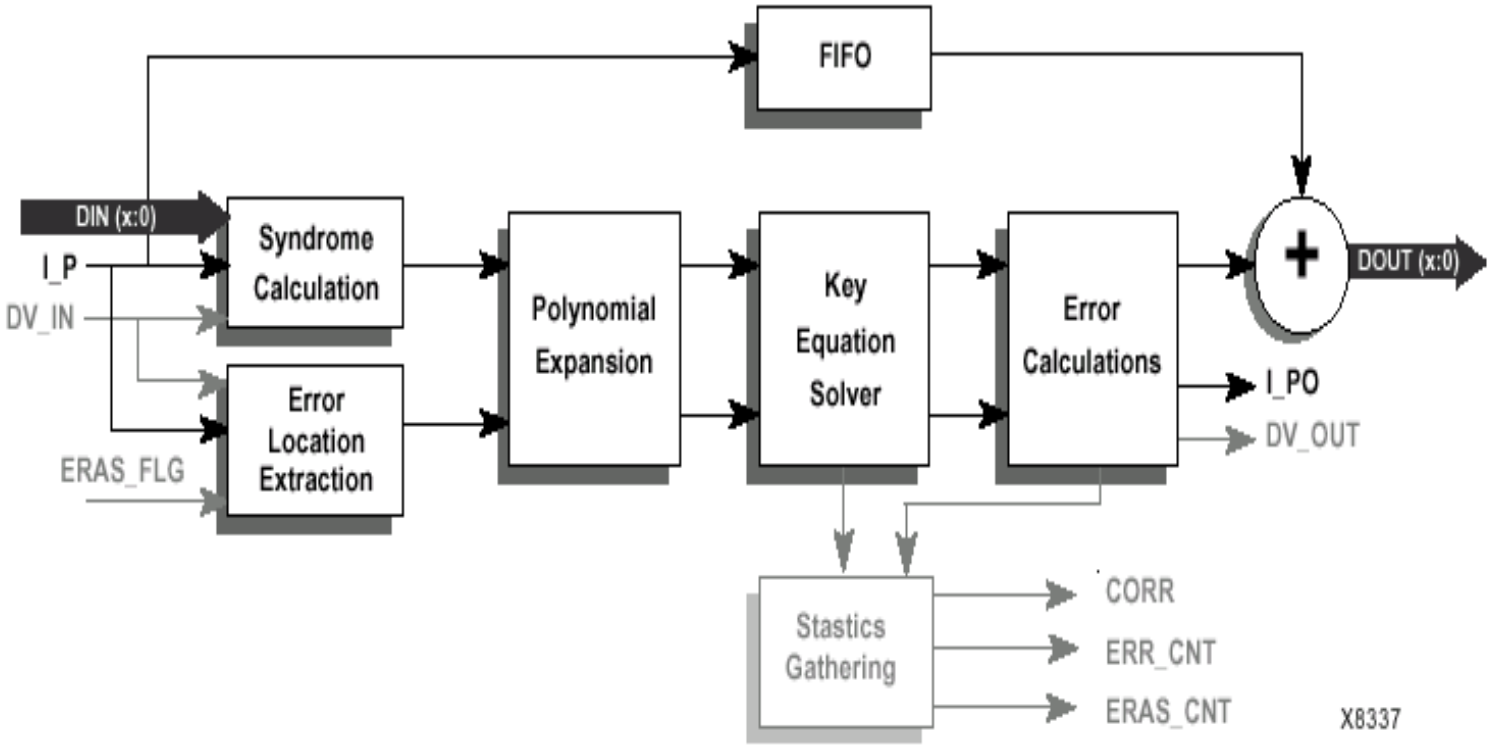
What Does FEC Do?

- Enables the receiver to detect and correct errors automatically without requesting retransmission
- Based on the addition of redundant parity information to the data being transmitted
- One metric of the quality of the communication link is measured in terms of Bit Error Rate (BER)
- Widely used in real-time systems for the transmission of audio and video data

Reed-Solomon Encoder / Decoder

- Reed-Solomon
  - An error-correcting coding system that corrects multiple errors, especially burst-type errors in communication systems
  - Transmitter (encoder)
    - Data is encoded to be corrected in the event it acquires errors
  - Receiver (decoder)
    - Uses the appended encoded bits to determine errors
    - Corrects the errors upon reception of the transmitted signal

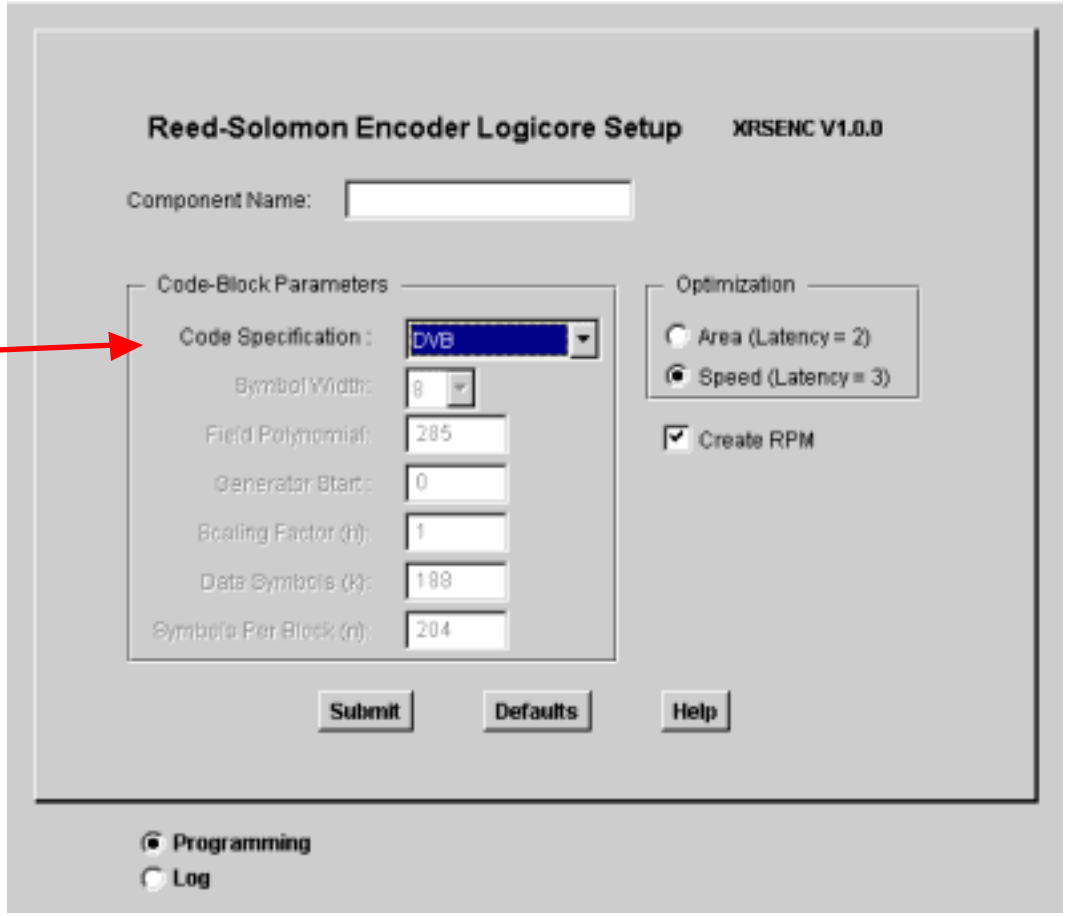
Reed-Solomon Decoder Block Diagram for iDTV



Xilinx Reed-Solomon

Reed-Solomon GUIs

- Parameterisable encoder and decoder cores available from Xilinx
- Simply select DVB/ATSC from the *Code Specification* menu
- Reed-Solomon tutorials online at Xilinx IP Centre



LogiCORE™

XILINX®

Reed-Solomon Decoder DVT Examples

Features	ATSC 1	ATSC 2	ATSC 3	ATSC 4	DVB 1	DBV 2	DBV 3	DBV 4
Generator Start	0	0	0	0	0	0	0	0
k	1	1	1	1	1	1	1	1
k	187	187	187	187	188	188	188	188
n	207	207	207	207	204	204	204	204
Polynomial	285	285	285	285	285	285	285	285
Symbol Width	8	8	8	8	8	8	8	8
Sync Mode	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse
Clock Enable	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Synochronous Reset	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Delayed Original Data	No	No	Yes	Yes	No	No	Yes	Yes
Erasure Decoding	No	No	No	Yes	No	No	No	Yes
Clock Periods Per Symbol	1	1	1	1	1	1	1	1
Memory Style	Automatic	Automatic	Automatic	Automatic	Automatic	Automatic	Automatic	Automatic
Processing Delay	294	294	294	525	204	204	204	357
Latency	507	507	507	738	414	414	414	567
Xilinx Device	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V500 -FG256-5	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V500 -FG256-5
Area (Slices)	754	785	785	1793	619	646	646	1476
Slices Remaining	782	751	751	1279	917	890	890	1596
Maximum Clock Frequency	100 MHz	98 MHz	100 MHz	87 MHz	98 MHz	98 MHz	92 MHz	89 MHz

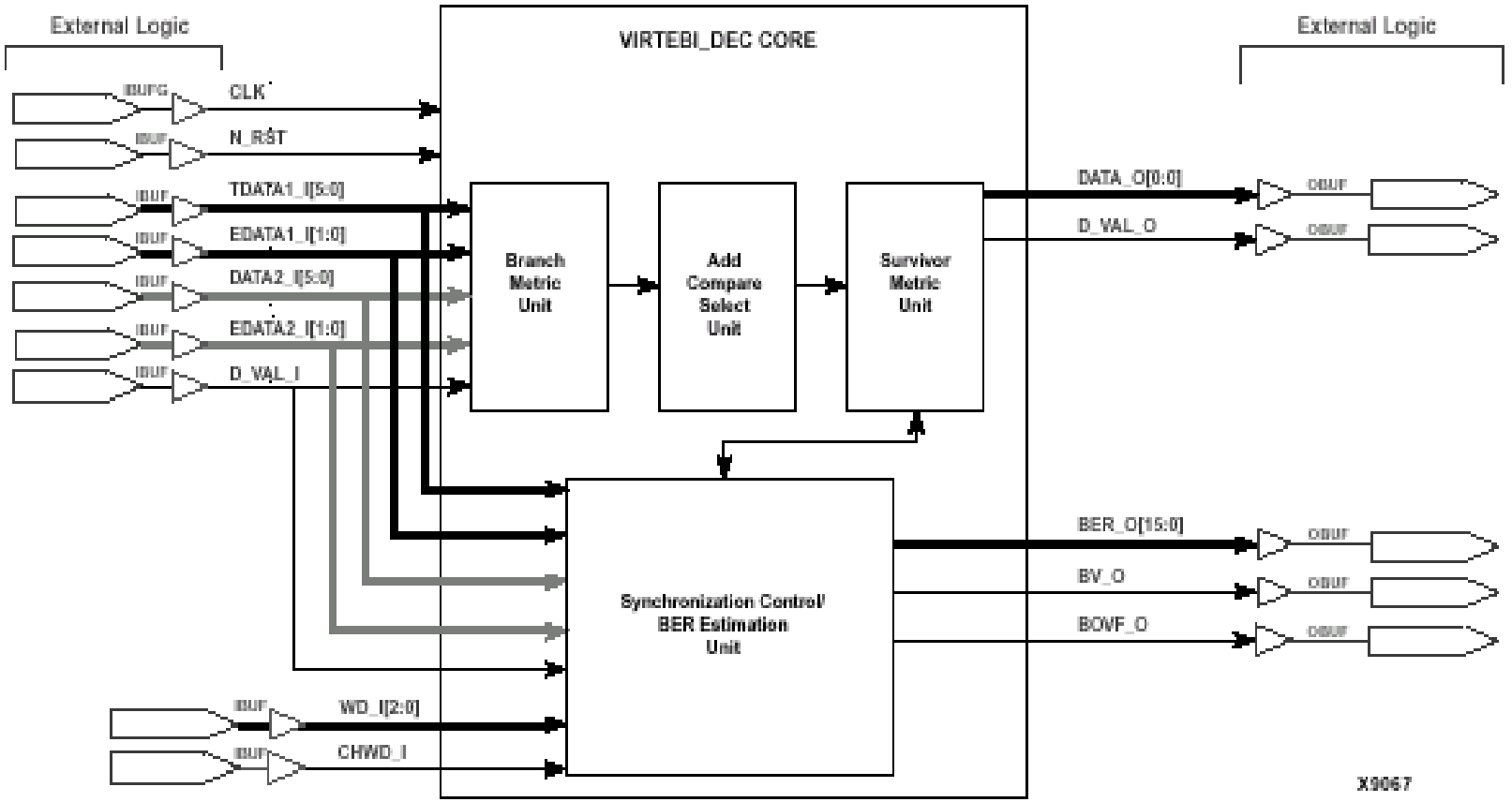
Reed-Solomon IP Solutions - Advantages

- The Xilinx decoder core is half the size of any competitor's offering
- Automatically configured from user parameters
  - Supports all major coding standards and custom implementations
- Can be optimized for area or speed
- Incorporates Xilinx Smart-IP technology for design predictability

Viterbi

- Viterbi algorithm
  - It is a convolutional code to correct random errors
  - It minimizes the number of sequences in the trellis search as new data is received by the demodulator
  - Developed by Dr. Andrew J. Viterbi
    - Co-founder, Retired Vice chairman, Board of Directors of QUALCOMM

Viterbi Decoder Block Diagram

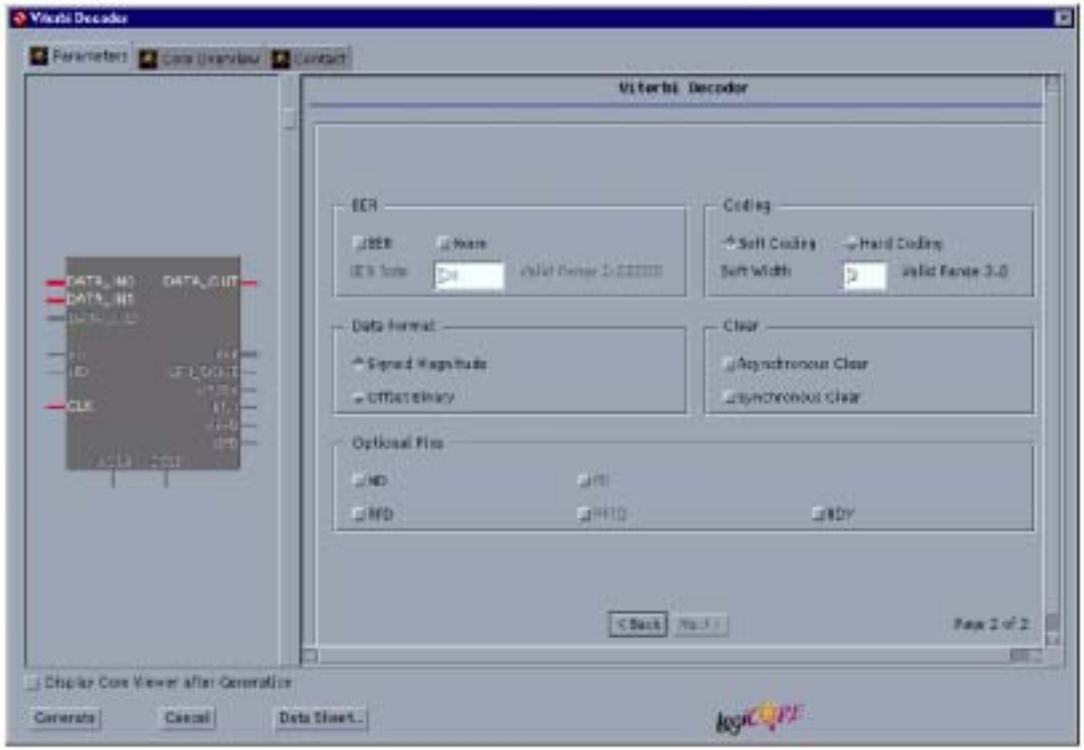


Viterbi Decoder IP

- Decoder of convolutional codes
- Customized VHDL source code available, allowing generation of different netlist versions
- Customized testbench for pre- and post-synthesis verification supplied with the module

Viterbi LogiCore GUI

- Fully parameterizable - includes parallel, serial & puncturing options
- Order DO-DI-VITERBI
- More info at http://www.xilinx.com/ipcenter

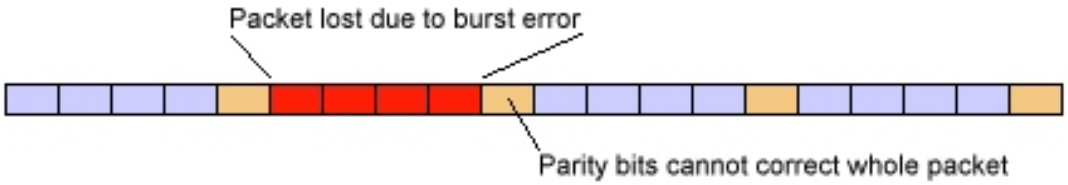


Spartan-II Based Viterbi Decoder

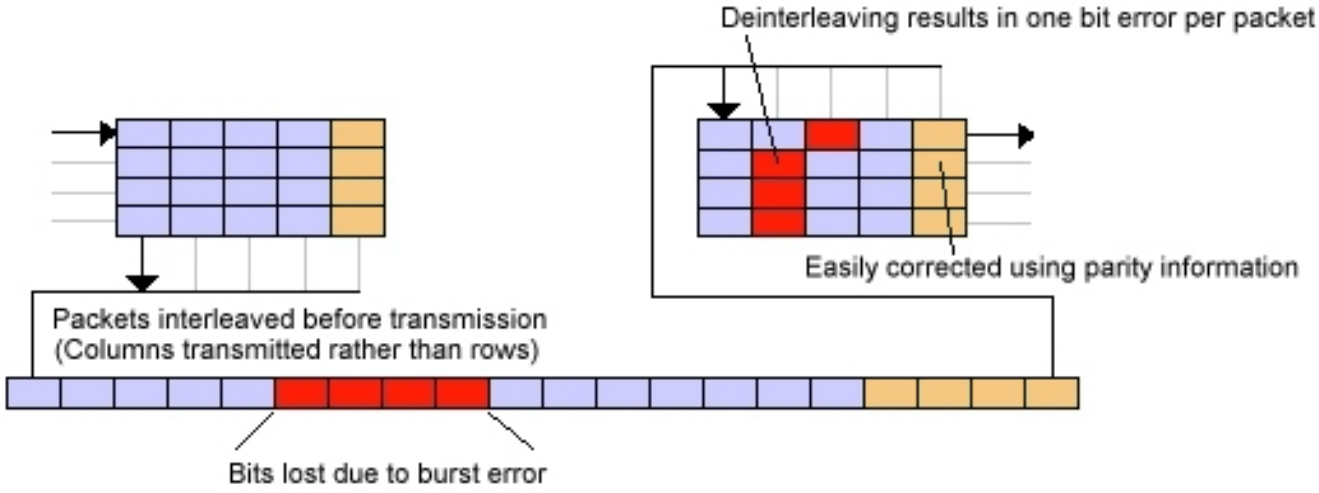
Spartan-II FPGAs Based Viterbi Decoder Specifics	
Product Families Supported	Spartan, Spartan-II, Virtex, Virtex-E
Device Tested	XC2S50-6
CLBs	495
Clock IOBs	1
IOBs	34
Performance (MHz)	56
Special Features	4 BlockRAMs

Outer Interleaver

RS decoder can only correct a limited amount of errors per packet:

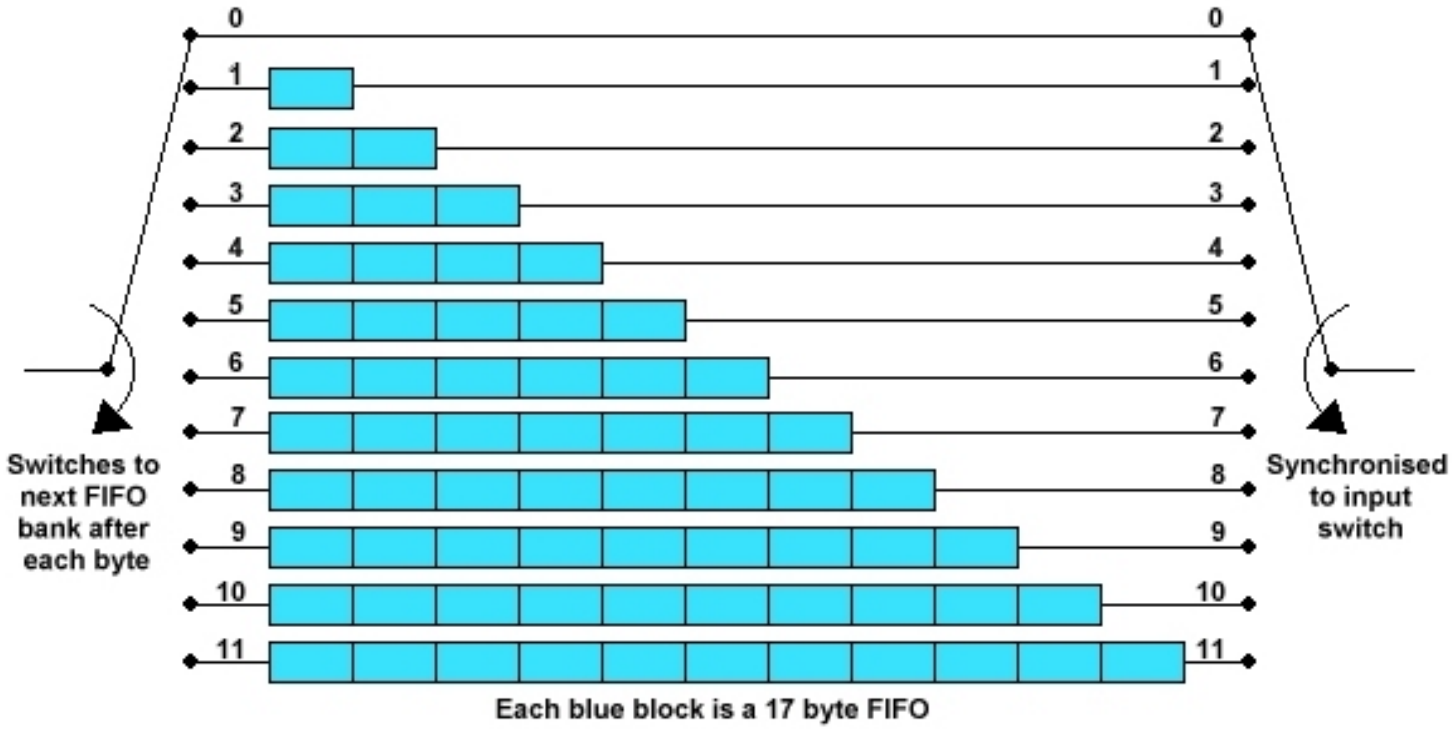


Interleaving spreads burst errors across several packets:



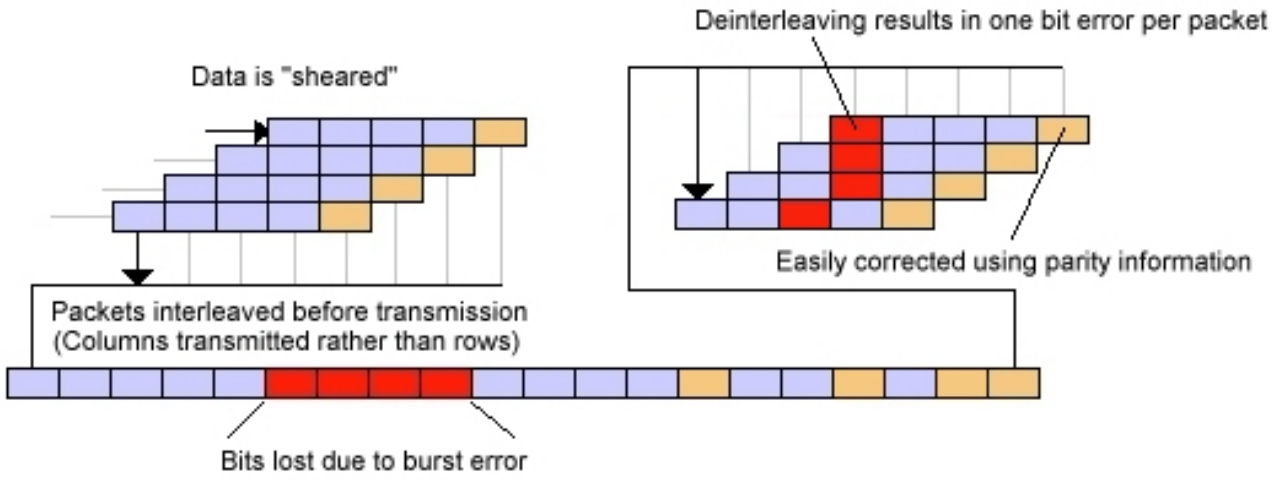
DVB Outer Interleaver

Previous interleaver example was actually *block* based whereas DVB version is *convolutional (Forney algorithm)*
Error dispersion idea is basically the same



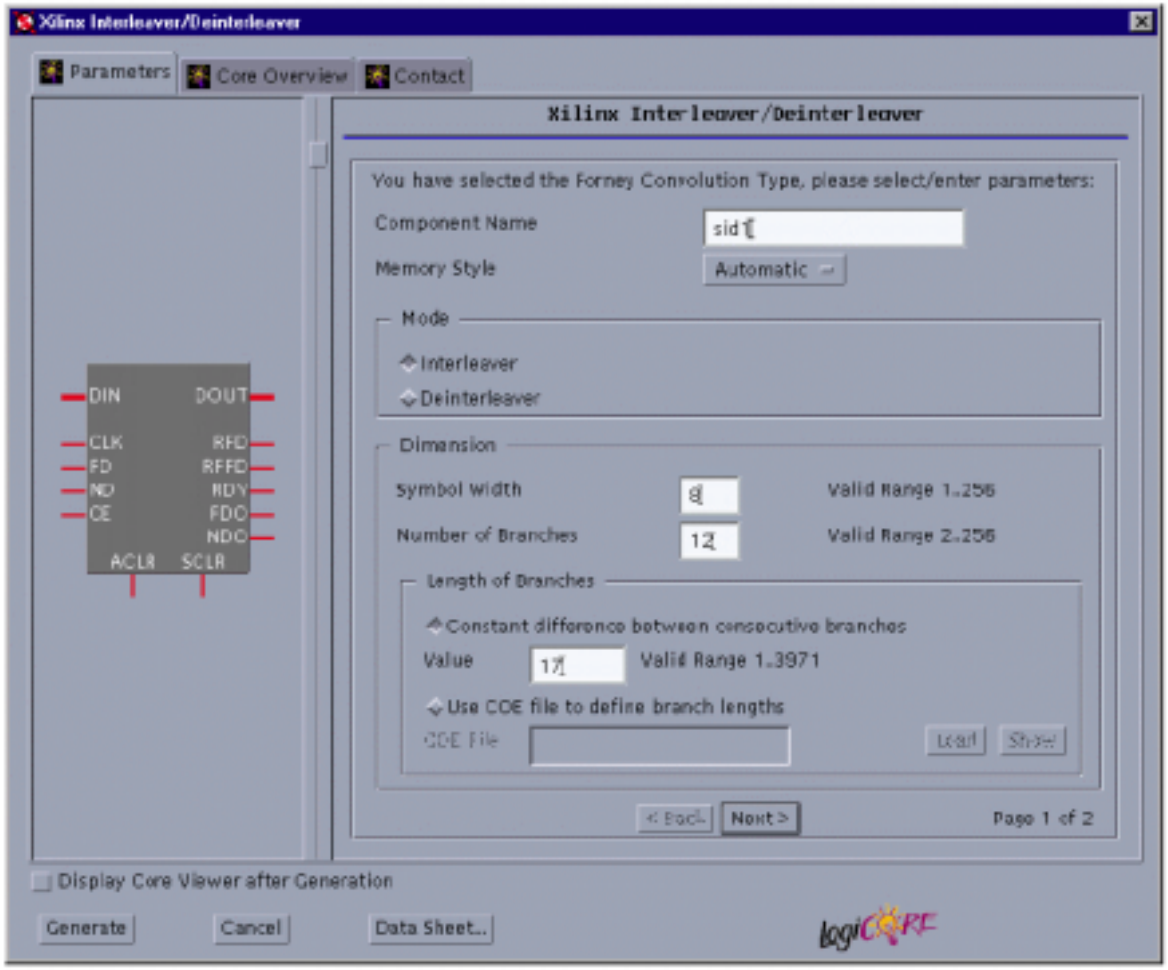
Convolutional Interleaver

Data is effectively *sheared* in a DVB interleaver



This has the advantage of needing less memory for implementation

Xilinx Interleaver/Deinterleaver GUI



Interleaver/Deinterleaver iDTV Example

Options	DVB 1	DVB 2
Mode	Interleaver	De-interleaver
Number of Branches	12	12
Branch Length Constant	17	17
Symbol Width	8	8
Pipelining	Maximum	Maximum
Optional Pins	FDO, RDY, RFFD	FDO, RDY, RFFD
Memory Style	Automatic	Automatic
Create RPM	No	No
Xilinx Device	XC2V40-5	XC2V40-5
Use IOB Flip-Flops	No	No
Area (slices)	79	110
Number of Block RAMs	1	2
Maximum Clock Frequency	187 MHz	183 MHz

FEC Summary

- Range of parameterizable cores available
  - Reed-Solomon encoder/decoder
  - Convolutional encoder
  - Viterbi decoder
  - Interleaver/de-interleaver
  - Turbo codecs
- Intuitive generator GUI enables fast core production
- Tutorials and core details available at:

http://www.xilinx.com/ipcenter/fec_index.html

Content Protection

Copy Protection and Data Encryption

- Motivation for data encryption & cryptography
  - Data privacy (Integrity & Secrecy)
  - Authenticating the source of the information
- Several methods of data encryption exist
  - RSA (Rivest-Shamir-Adleman), Diffie-Hellman, RC4/RC5
  - Secure Hashing Algorithm (SHA), Blowfish
  - Elliptic Curves, ElGamal, LUC (Lucas Sequence)
  - DES (Data Encryption Standard) & Triple-DES (TDES)
- Xilinx Spartan-IIE + IP Cores today provide
  - AES, DES, Triple DES, proprietary

Copy Protection Efforts

Copy-protection efforts at a glance

- CPTWG (a cross-industry forum among the movie, PC and consumer electronics industries): Five-year-old group meets regularly to propose and discuss technology issues related to DVD, including copy protection, encryption and watermarking.

- 5C (formed by Intel Corp., Hitachi Ltd., Sony Corp, Toshiba Corp. and Matsushita Electric Industrial Co.): Worked to develop Digital Transmission Content Protection (DTCP) to define a cryptographic protocol copy protection.

- 4C (initiated by Intel, IBM, Matsushita and Toshiba): Working on a Content Protection for Recordable Media and Pre-Recorded Media (CPRM/CPPM) specification that defines a renewable cryptographic method to protect entertainment content recorded on physical media.

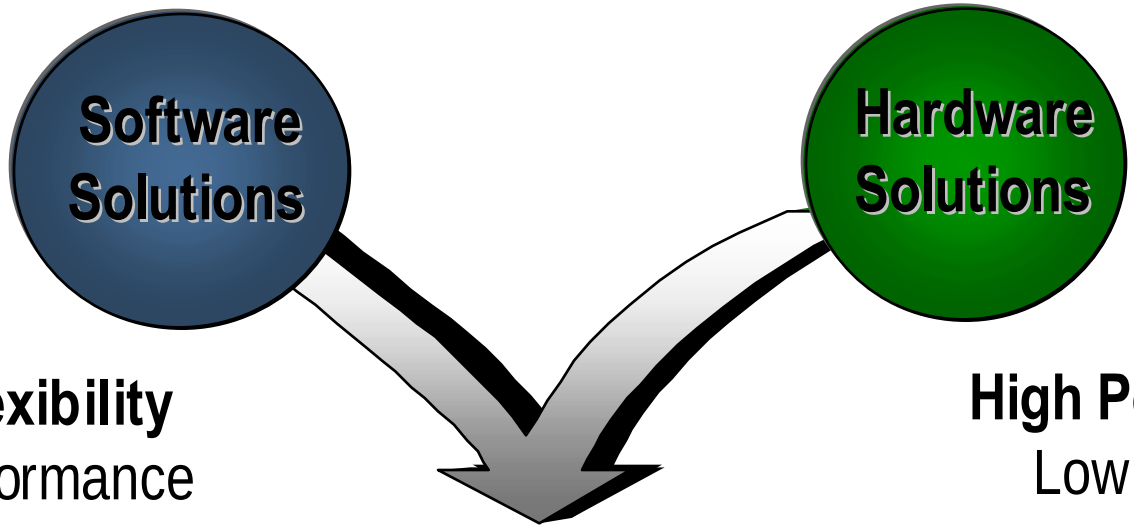
- TCPA (formed by Compaq, HP, IBM, Intel and Microsoft): Focuses on developing a specification to deliver a set of hardware and operating-system security capabilities that customers can use to "enhance the trust and security in their computing environments," the group said.

Courtesy: EETimes

Copy Protection - FPGAs Add Significant Value

- Security Systems Standards and Certification Act (Draft)
  - Calls for interactive digital devices to include security technologies certified by the U.S. Secretary of Commerce
- The bill becoming a law will prevent companies from shipping products without appropriate security
  - There is however no guidance on security schemes
  - A hardware based security implementation is preferred
- Lack of consensus between companies on the encryption schemes and their implementation is leading to chaos
- Copy protection for digital video products is in it's infancy and will be a significant area of focus

Spartan-IIE Advantages Over Hardware & Software Solutions



High Flexibility
Low Performance

High Performance
Low Flexibility

High Performance
High Flexibility

Enhanced Security & Performance

DES Concept

- The Data Encryption Standard (DES) algorithm
  - Developed by IBM Corporation
  - Most prevalent encryption algorithm
  - Adopted by the US government in 1977, as the federal standard for encryption of commercial and sensitive-yet-unclassified data
  - Is a Block cipher
    - Encryption algorithm that encrypts block of data all at once, and then goes on to the next block
  - Divides 64-bit plaintext into blocks of fixed length (ciphertext)
  - Enciphers using a 56-bit secret internal key

Triple-DES Concept

- Triple-DES concept
  - More powerful & more secure
  - Equivalent to performing DES 3 times on plaintext with 3 different keys
  - TDES use 2 or 3 56-bit keys
  - With one key, TDES performs the same as DES
  - TDES implementation: serial and parallel
    - Parallel improves performance and reduces gate count

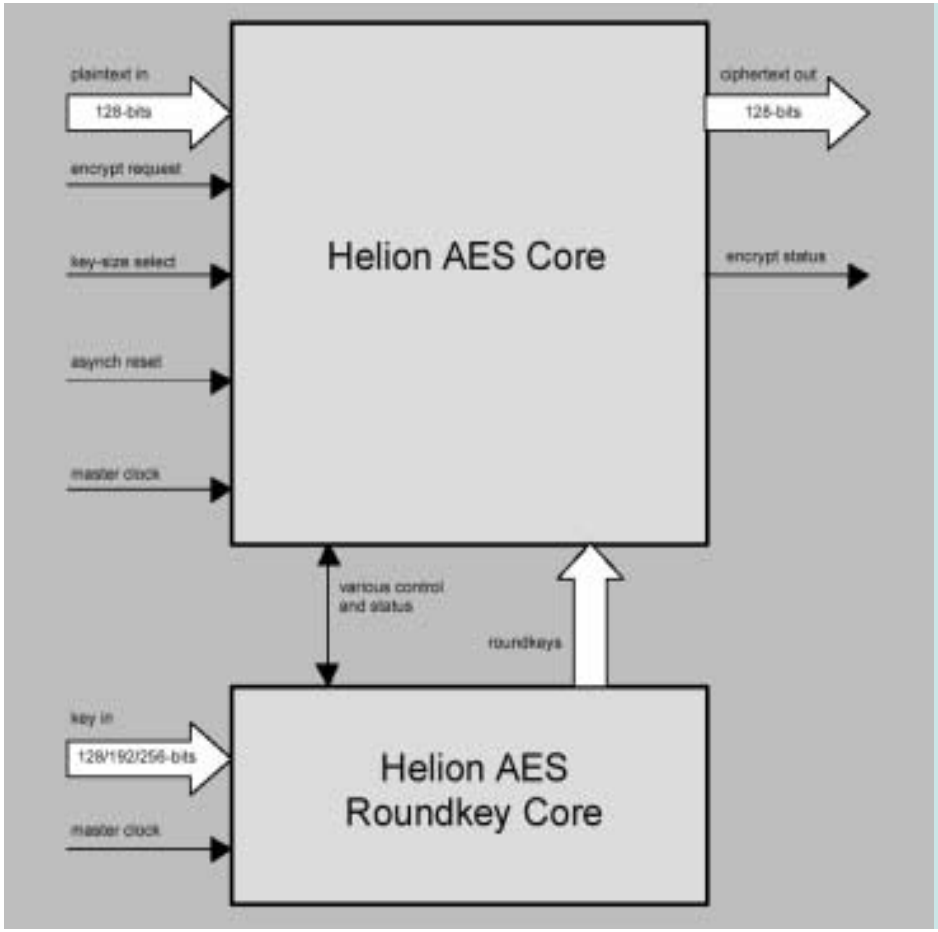
Value Proposition in DES and Triple DES

- High performance, many features and cost effective
- High scalability and flexibility
  - Reconfigurable fabric and Internet Reconfigurable Logic
- Embedded solutions
  - FPGA logic not used for DES/Triple-DES soft IP can be used for other IP solutions
    - DCT/IDCT and DES/TDES soft IP in a Spartan-IIE FPGA can be used in multimedia and imaging applications
  - Increase the value proposition and reduce solution cost
- Spartan-IIE can be programmed with broadcaster proprietary conditional access algorithms

AES (Rijndael)

- AES (Rijndael) chosen by the National Institute of Standards and Technology (NIST) as the cryptographic algorithm for use by U.S. government organizations to protect sensitive (unclassified) information
  - Rijndael block cipher named after its Dutch developers Vincent Rijmen and Joan Daemen
- Aimed to replace DES over the long term
  - DES has been successfully attacked using dedicated hardware and parallel computer networks
  - DES to be phased out
- Triple-DES expected to remain for foreseeable future

AES (Rijndael)
IP Solutions - Helion Technology



Features

- Implements AES (Rijndael) to latest NIST FIPS proposal
- 128-bit block-size, option of 128, 192 or 256-bit key-size (can be changed dynamically)
- Very fast operation – completes one AES round per master clock
- Supports data rates in excess of 10Gbps
- Separate encrypt and decrypt cores available
- Supports optional real-time roundkey generation
- All AES operating modes easily implemented (eg. ECB, CBC, OFB, CFB, MAC)
- Simple external interface
- Highly optimised for use in Xilinx FPGA technologies

Deliverables

- Target specific netlist or fully synthesisable RTL VHDL
- VHDL simulation model and testbench with FIPS test vectors
- User documentation

HELION

XILINX

Content Protection Solutions

- Xilinx encryption solutions are NIST approved
- The programmable nature of these solutions allows easy customization based on end application requirement

Spartan-IIE Implementation Examples				
	DES	Triple-DES	AES	AES
Device	2S100E-6	2S150E-6	2S100E-6	2S100E-6
CLB Slices	235	1611	358*	231**
Performance	94 MHz	48 MHz	82 MHz	82 MHz
Area Utilization	19.58%	93.22%	29.83%	19.25%
Key Size	56-bit	128-bit or two 64-bit	128/192/ 256-bit	128/192/ 256-bit

Note: Solution includes encryption, decryption and key generation

* 128-bit key implementation

** Key Generation offloaded to embedded µC/ µP


XILINX®
Enabling Digital
Signal Processing

Spartan-IIE DSP Advantages

- Off-the-shelf devices
- Faster time-to-market
- Rapid adoption of standards
- Real time prototyping

Flexibility of DSP Processors

- Parallel processing
- Support high data rates
- Optimal bit widths
- No real-time software coding

Performance of Custom ICs

Spartan-IIE DSP Solutions Offer the Best of Both Worlds With Low Cost!

Spartan-IIE - The DSP Solution

- Performance
  - Billions of MACs per second
  - Tremendous parallel processing capability
    - Distributed DSP resources, segmented routing and flexible architecture allow optimized implementation of algorithms
    - No instruction flow overhead
  - High-memory bandwidth
    - Distributed RAM to store DSP coefficients and FIR filters
    - True dual-port BlockRAM
      - Optimized data buffering and storage
      - Applications like FFT for next generation HDTV, video line buffers
  - DLL for multi-rate clocks
  - High I/O bandwidth and flexible interfaces
    - Supports 19 high-speed signal & memory interface standards
      - LVDS, LVTTL, SSTL, HSTL, GTL+, PECL ...
- Low cost, flexibility and time-to-market through reprogrammability

DSP IP for FPGAs

- Error Correction
  - Reed-Solomon
  - Viterbi Encoder/Decoder
- FIR Filter Generator
  - Polyphase decimator
  - Polyphase interpolator
  - Half-band filters
  - Hilbert transform
- FFTs
- Direct Digital Synthesizer
  - Includes quadrature output
- Voice Coding
- Enhanced Direct Digital Synthesizer
- Turbo Convolutional Encoder/Decoder
- 3GPP Interleaver/ De-interleaver
- Digital Down Converter
- PN Sequence Generator
  - Gold code support
- Correlators
- Echo Cancellation

System Generator for Simulink

- Bridges gap between FPGA and DSP design flows
  - Used with Simulink®/MATLAB® from The MathWorks
- Automatically generates HDL/optimized algorithms
  - Shortens learning curve
  - HW redesign eliminated
  - Optimal implementation

XtremeDSP

- Industry first System Generator for Simulink® bridges gap between FPGA and conventional DSP design flows
- Unique constraint-driven Filter Generator allows optimization between performance and cost
- Power estimator tool (Xpower™) for power-sensitive DSP implementations
- 11 optimized DSP algorithms/cores that cut development time by weeks
- DSP features added to ChipScope ILA tool dramatically accelerate hardware debugging time

Video/Image Processing IP

- DCT/IDCT
  - Inverse Discrete Cosine Transform (IDCT)
  - 1-D Discrete Cosine Transform
  - 2-D DCT/IDCT Forward & Inverse Discrete Cosine Transform
- JPEG CODEC
  - Fast JPEG Color Decoder
  - Fast JPEG B/W Decoder
- logiCVC - Compact Video Controller
- Color Space Converter
  - RGB2YCrCb
  - YCrCb2RGB
  - RGB2YUV
  - YUV2RGB

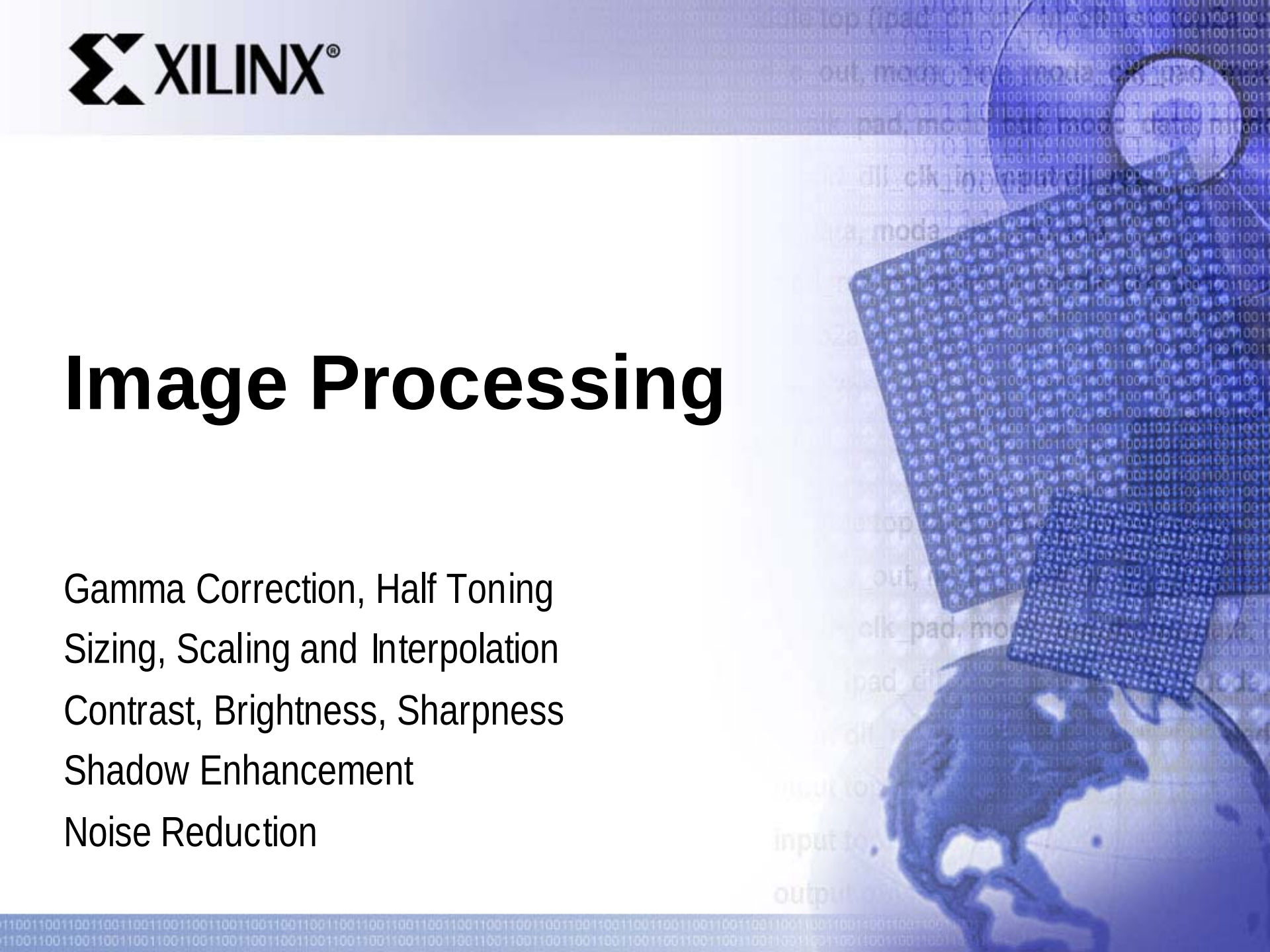


Image Processing

Gamma Correction, Half Toning

Sizing, Scaling and Interpolation

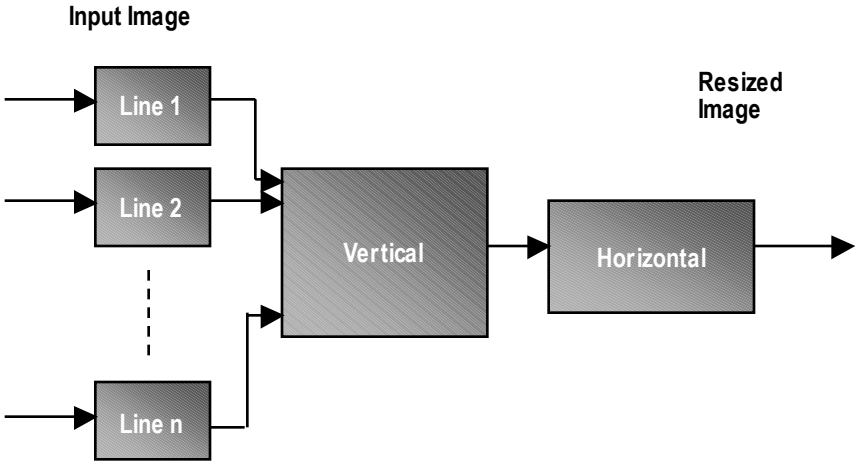
Contrast, Brightness, Sharpness

Shadow Enhancement

Noise Reduction

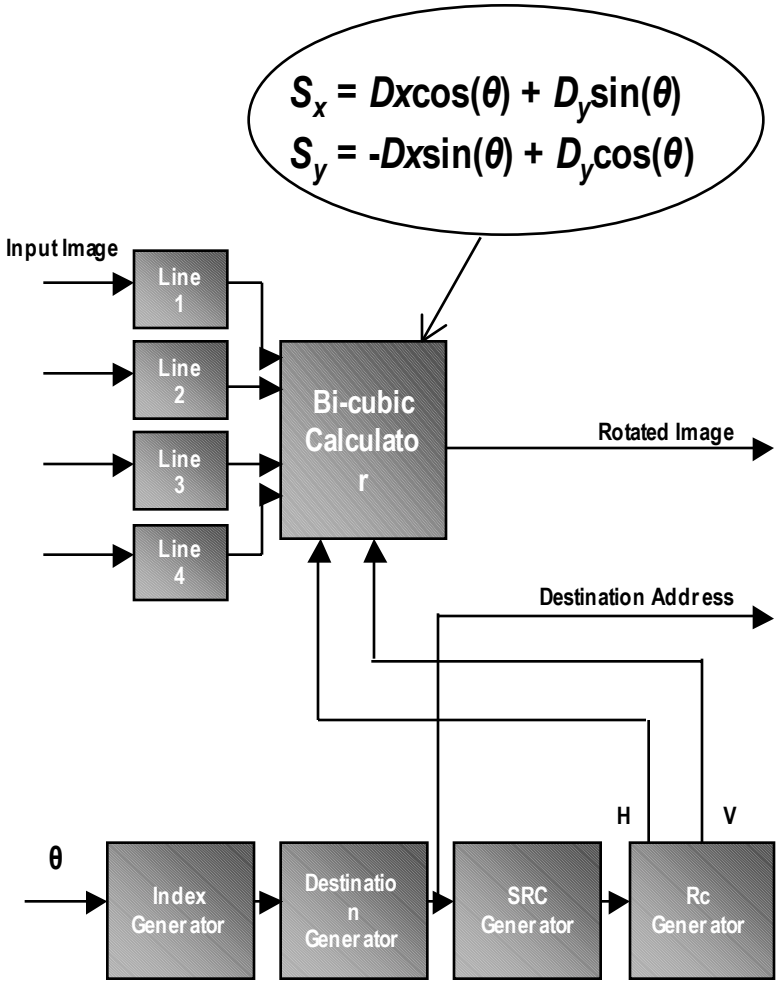
Real-Time Image Resizing With Low Memory Requirements 2 Dimensional Architecture Upscaling by 2, Downscaling by 4

- Example: 512 x 512 x 8 60 f/s
  - Upscaling by 2, Downscaling by 4
  - 16 pixel resolution
  - 8 Block RAMs for Line Buffers and Coefficient Bank
  - 4 vertical multipliers
  - 4 horizontal multipliers
  - Adder trees
  - Control

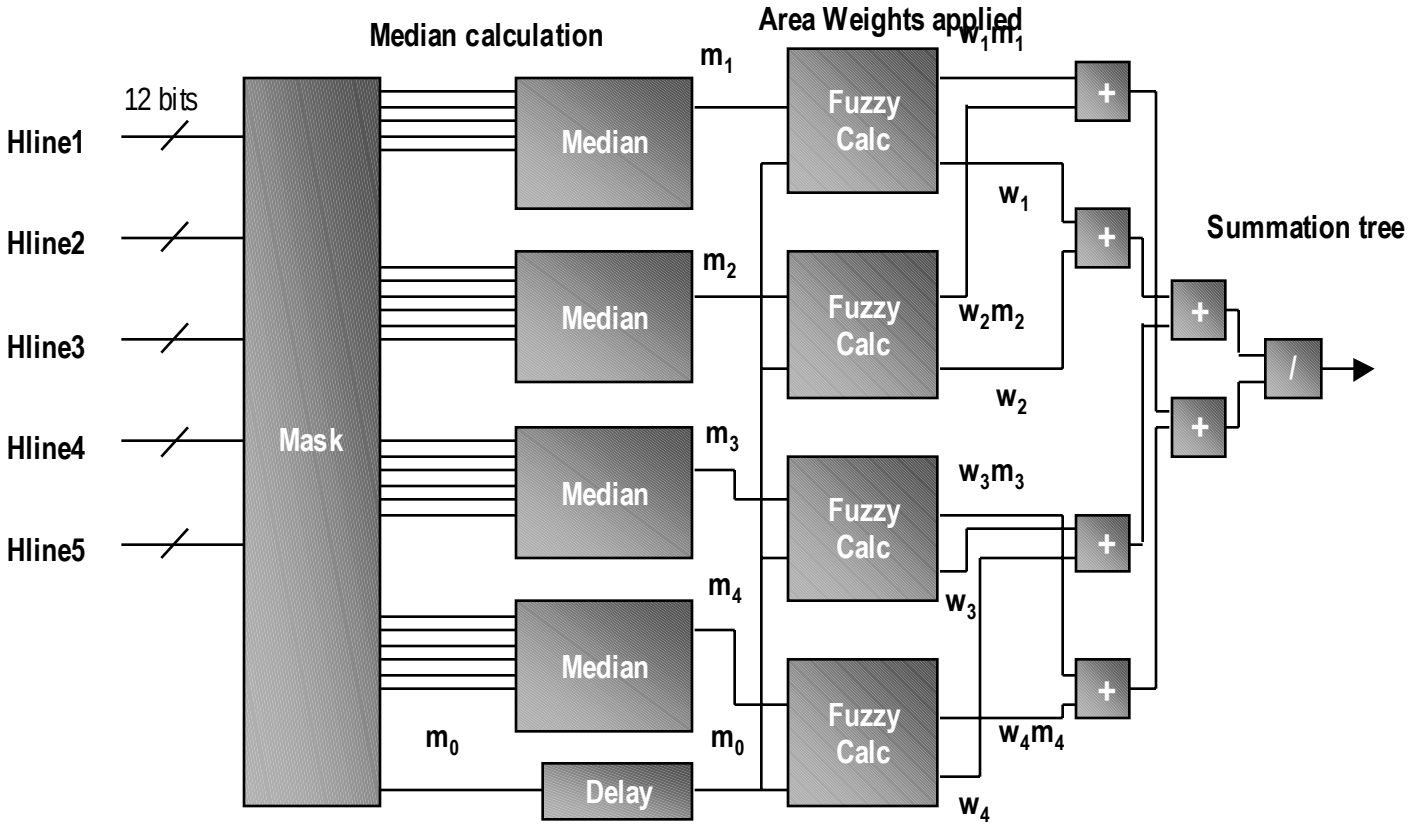


Real-Time Image Rotation

- Example:
  - Medical Imaging System
    - 1024 x 1024 x 12 @ 30 f/s
    - 40MHz Pixel Clock
    - 160MHz Core Clock
  - Xilinx XC2S300E FPGA
    - 12 Block RAMs for line buffers
    - 2 Block RAMs for RC lookup tab
    - 5 multiplier pixel calculation
    - Sine/Cosine, 2 Block RAMs
    - Dx, Dy calculation
    - Sx, Sy calculation
    - Control



2D Non-Linear Filter Block Diagram

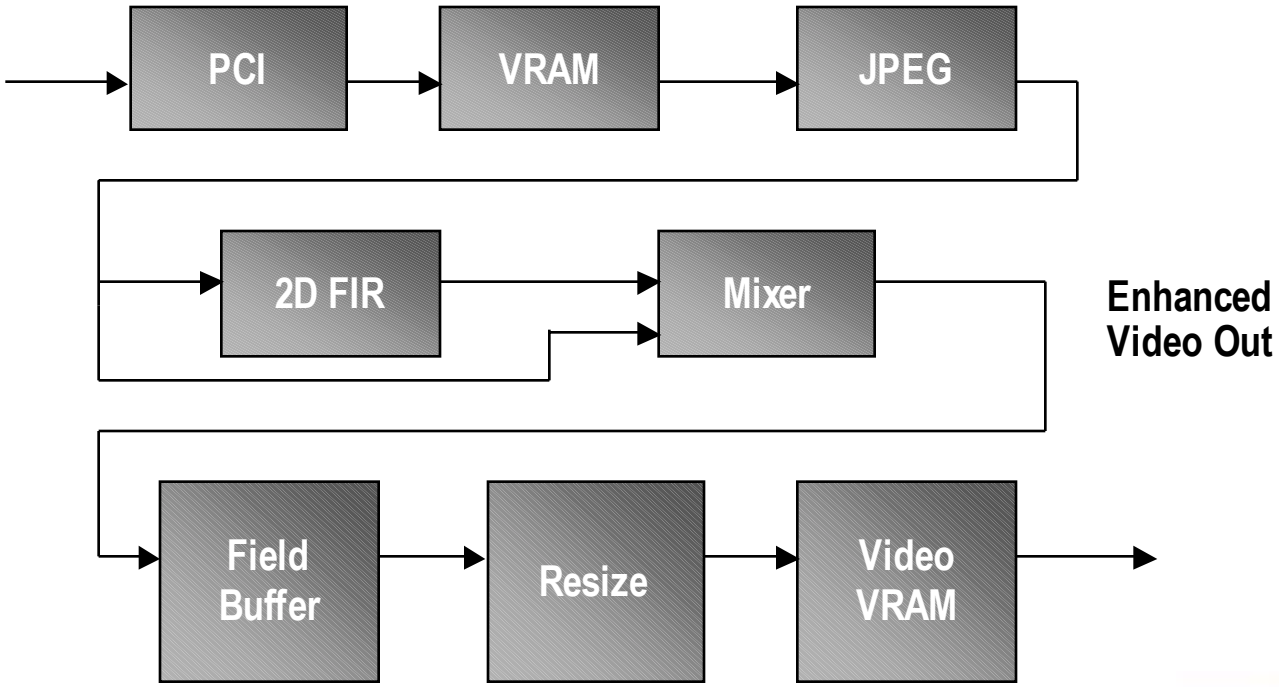


2D FIR Example

- 2D FIR
  - 1Kx1K image size
  - 8-12 bit pixel data
  - 64x64 kernel size
  - 128 multipliers
  - 64 line buffers (1024 in length)
  - Summation tree in distributed logic
- Single-chip solution

Spatial Enhancement Implementation

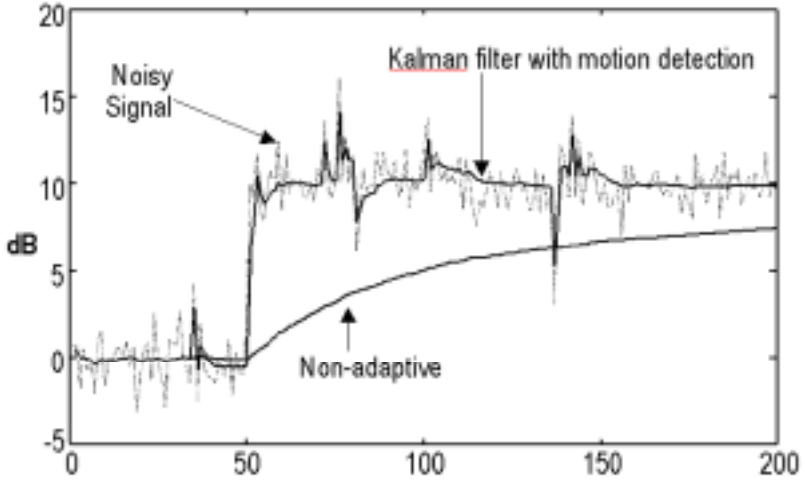
- PCI, Line Buffers, 2D FIR and Mixer
- Field Buffers, JPEG, Resizing



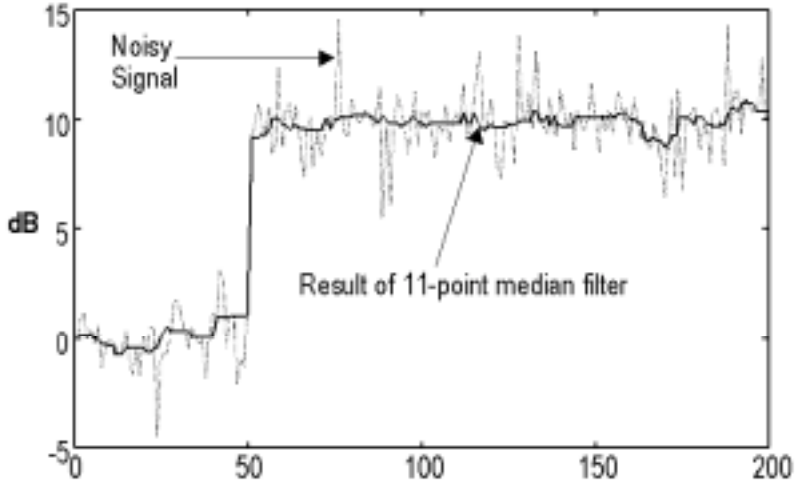
Noise Reduction

- Noise reduction using temporal filtering across multiple video frames

Kalman Filter

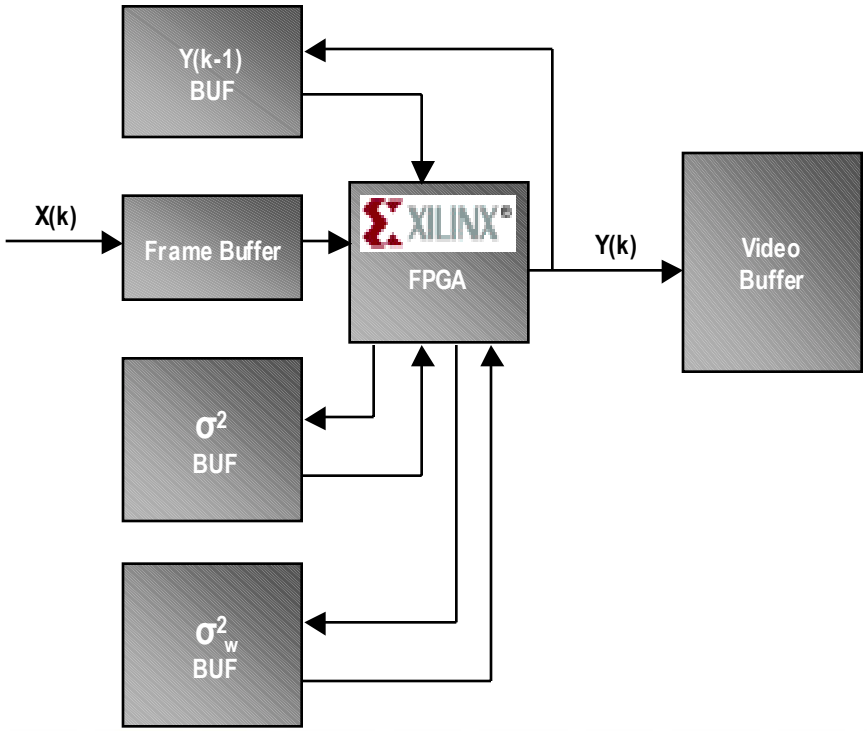


Median Filter



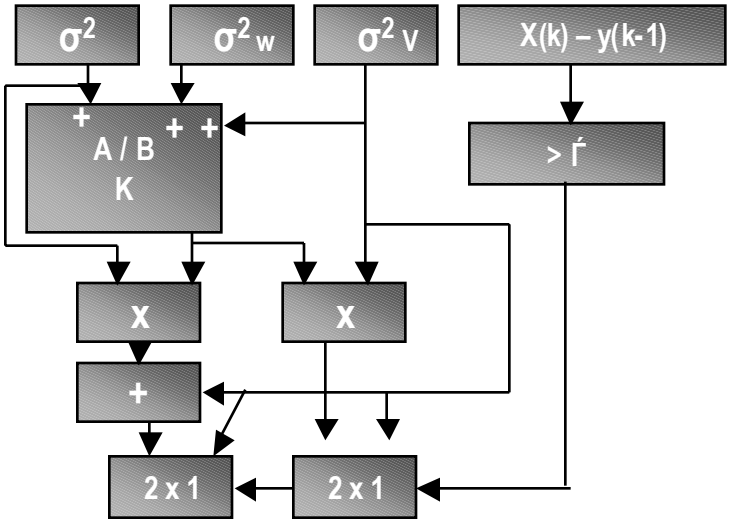
Temporal Filter

System Block Diagram

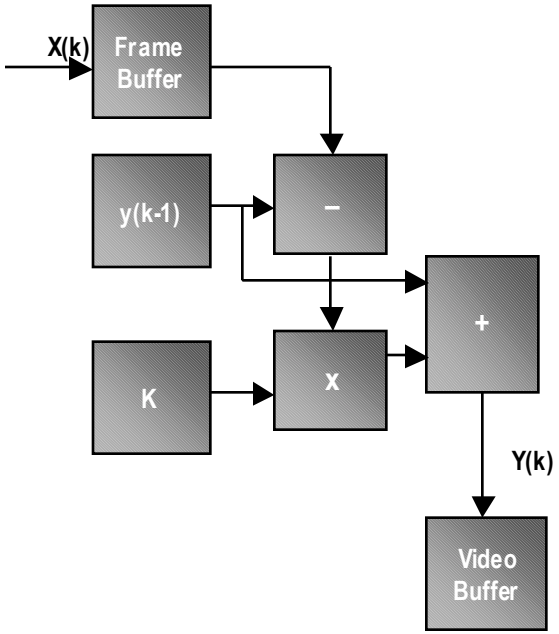


Temporal Filter - Sub Blocks

Filter Parameter Calculation



Pixel Calculation



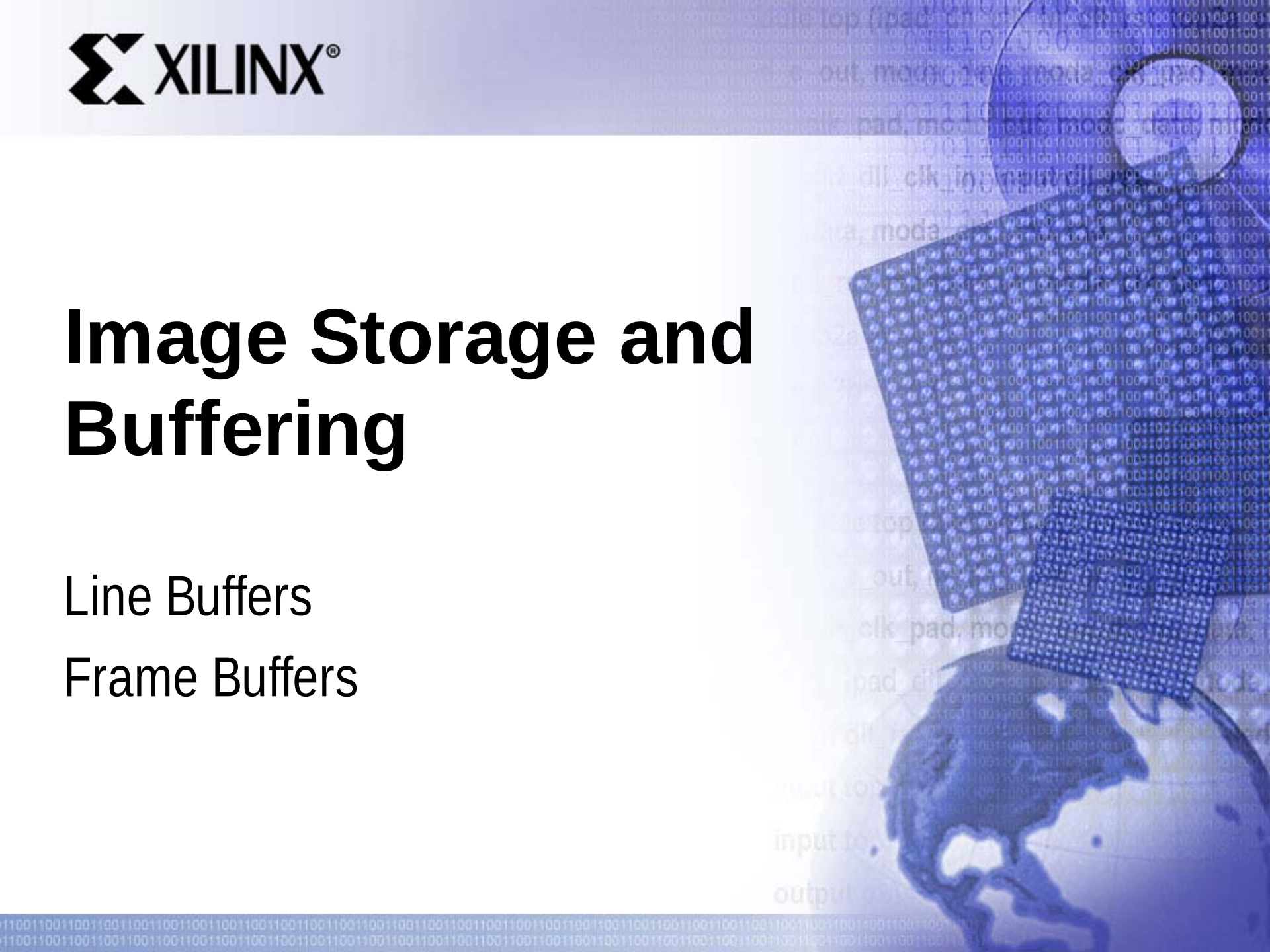


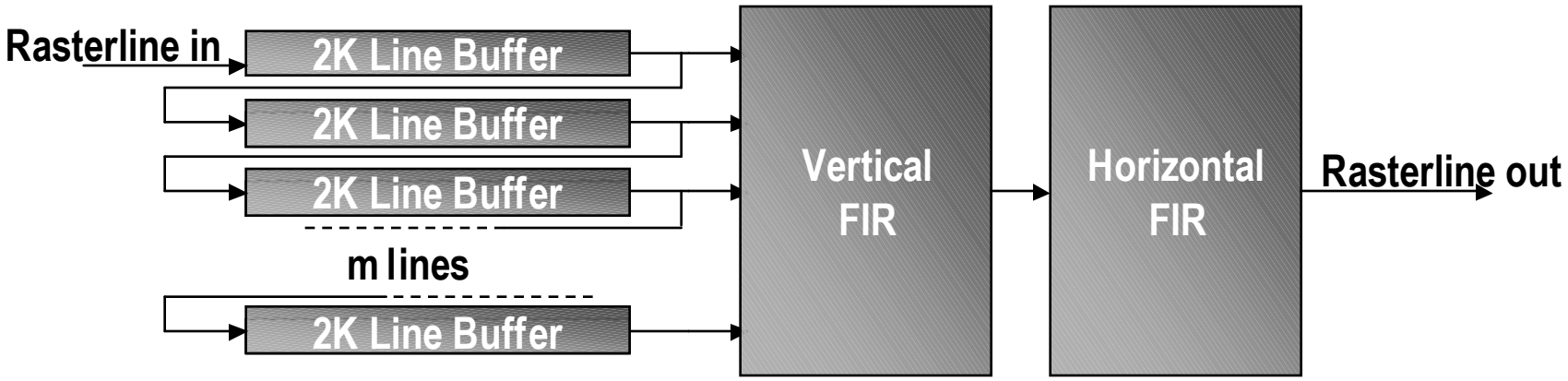
Image Storage and Buffering

Line Buffers

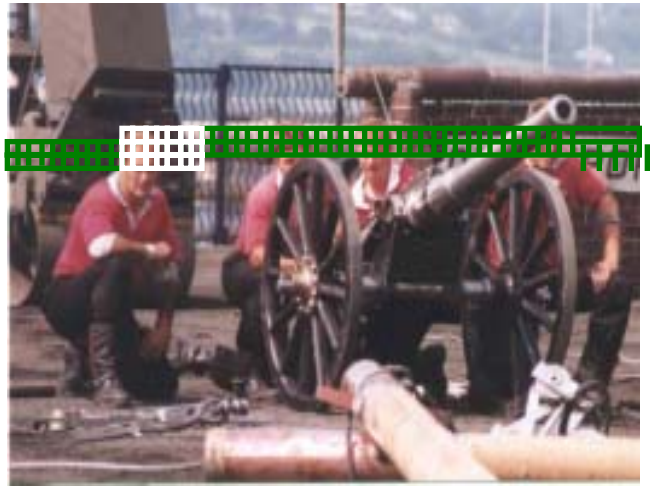
Frame Buffers

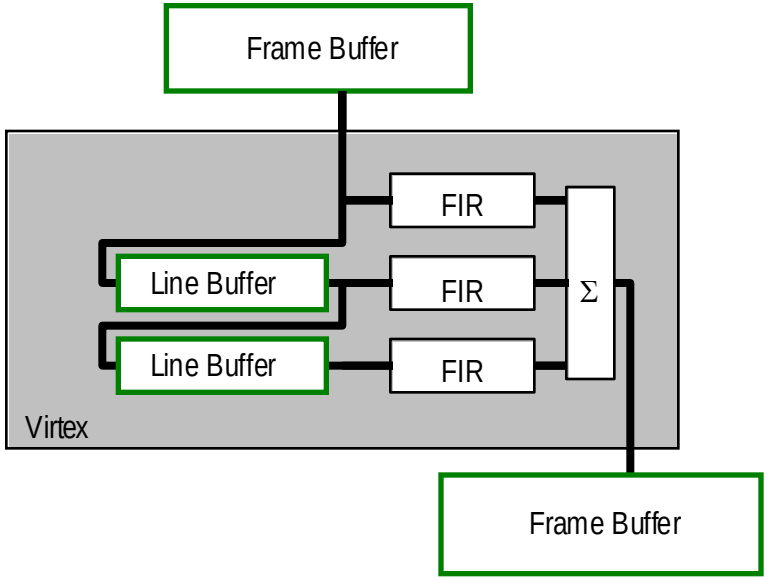
Line Buffering

- Line Buffers feed Horizontal and Vertical FIR filters to do real-time image processing without frames store



2D Image Processing Using BlockRAM Line Buffers





- Line Buffers provided by Block RAM using cyclic buffer technique
- 768 Pixel Line Buffers (8-bit)
  - 576 per Device
- 1920 Pixel Line Buffers (36-bit = 12-bit RED + 12-bit GREEN + 12-bit BLUE)
  - 51 per Device

MPEG

The MPEG Algorithm

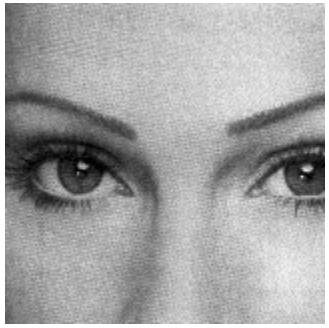
- The MPEG Encoder is composed of a number of discrete algorithmic sections
- Temporal Processing
  - Seeking out and removing temporal redundancy
    - Involves storing several successive images and performing motion estimation, compensation and simple algorithmic processing to derive a pixel-by-pixel difference signal
- Spatial Processing
  - Uses DCT to remove the high frequencies not discernable by the human eye
- Statistical or Variable Length Encoding (VLC) to remove redundancy in the output from the DCT

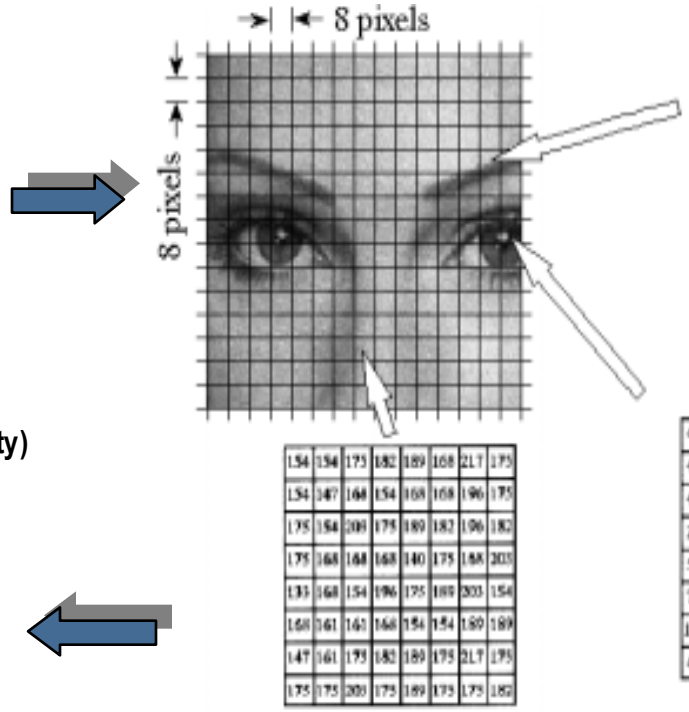
DCT/IDCT Concept

- What is DCT?
  - Returns the discrete cosine transform of ‘video/audio input’
  - Can be referred to as the even part of the Fourier series
  - Converts an image or audio block into it’s equivalent frequency coefficients
- What is IDCT?
  - The IDCT function is the inverse of the DCT function
  - The IDCT reconstructs a sequence from its discrete cosine transform (DCT) coefficients

DCT/IDCT Concept

Original Image





DCT

Frequency Coefficients Compared to Magnitude Thresholds, Resulting in Compressed Data Stream

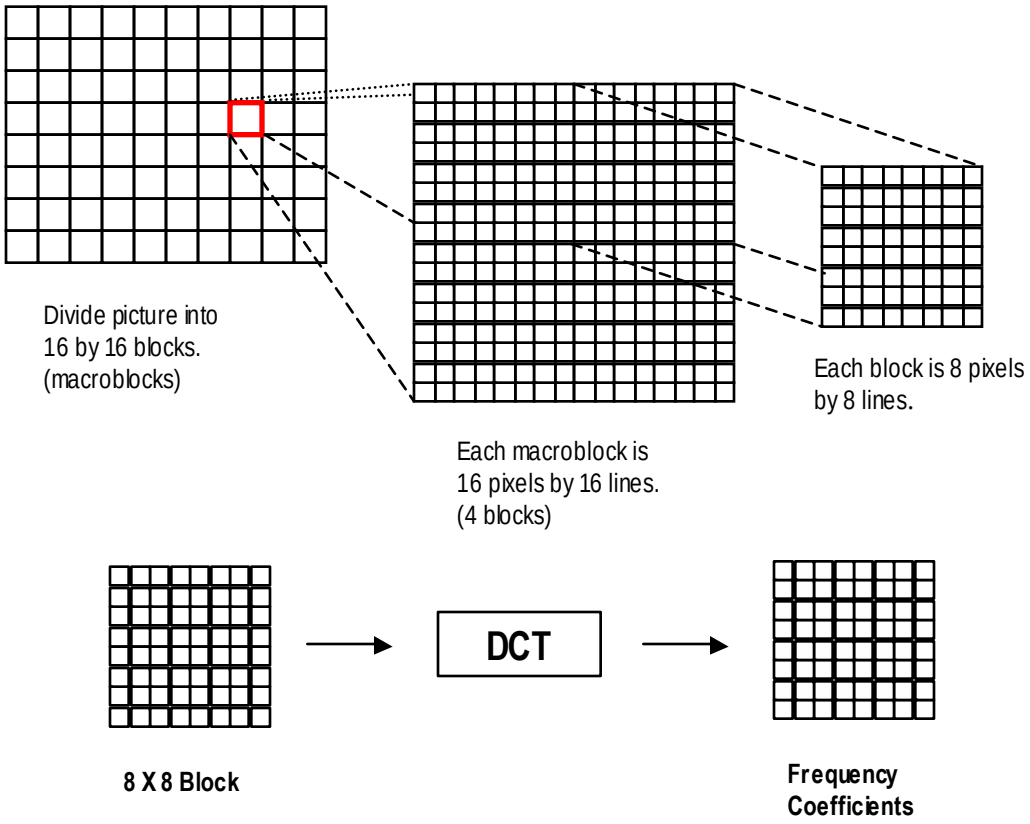
IDCT

Restored Image
(Notice Lesser Image Quality)

The image is broken into 8x8 groups, each containing 64 pixels. Three of these 8x8 groups are enlarged in this figure, showing the values of the individual pixels, a single byte value between 0 and 255.

Courtesy: The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith

DCT-IDCT Concept



Detailed steps in dissecting a typical digital still image prior to being DCT transformed

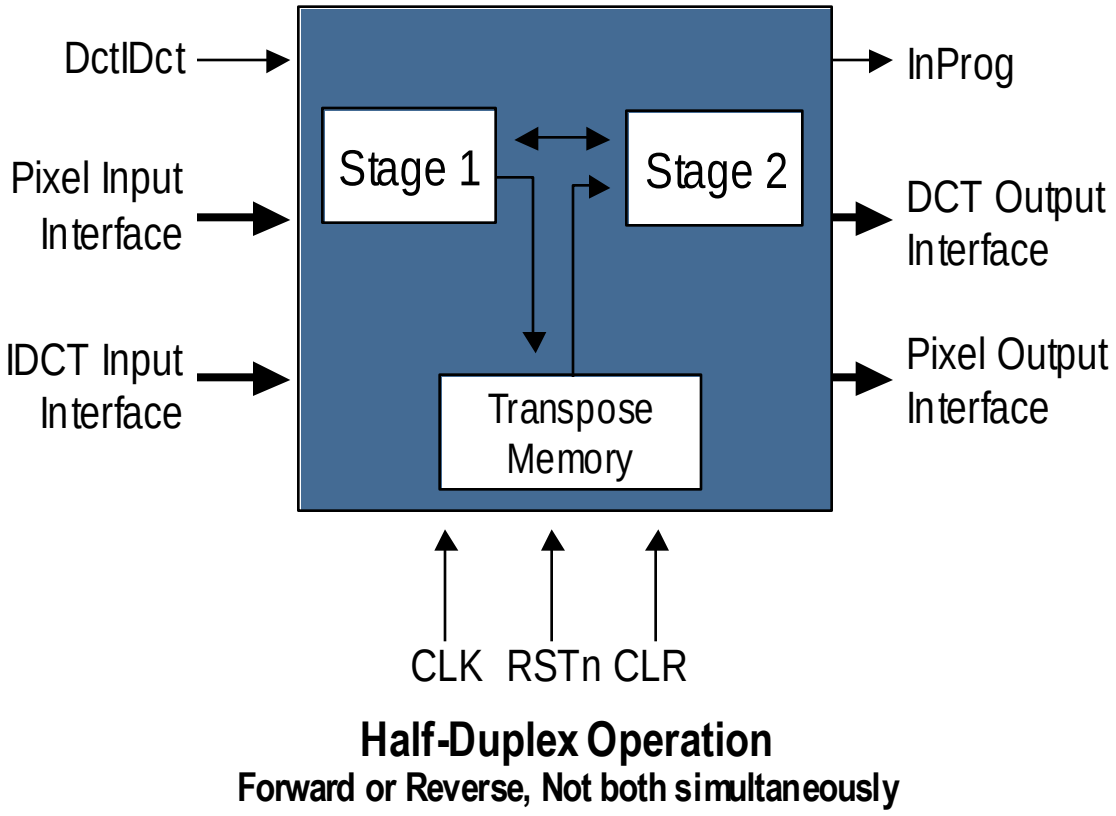
DCT/IDCT Compression

- Compression allows increased throughput through transmission medium
  - Video & audio compression makes multimedia systems very efficient
    - Increases CPU bandwidth
    - Higher video frame rates
    - Better audio quality
    - Enables multimedia interactivity
- DCT/IDCT are widely used in video & audio compression

Spartan-IIE DCT/IDCT LogiCore Features

- Combined DCT/IDCT core
- Continuous one symbol per cycle processing capability
- Internal precision:
- 14 bit cosine coefficients
- 15 bit transpose memory
- Optimized for specific Xilinx architecture
- Fully compliant with the JPEG standard (ISO/IEC10918-1)
- Supplied with Verilog and VHDL test benches

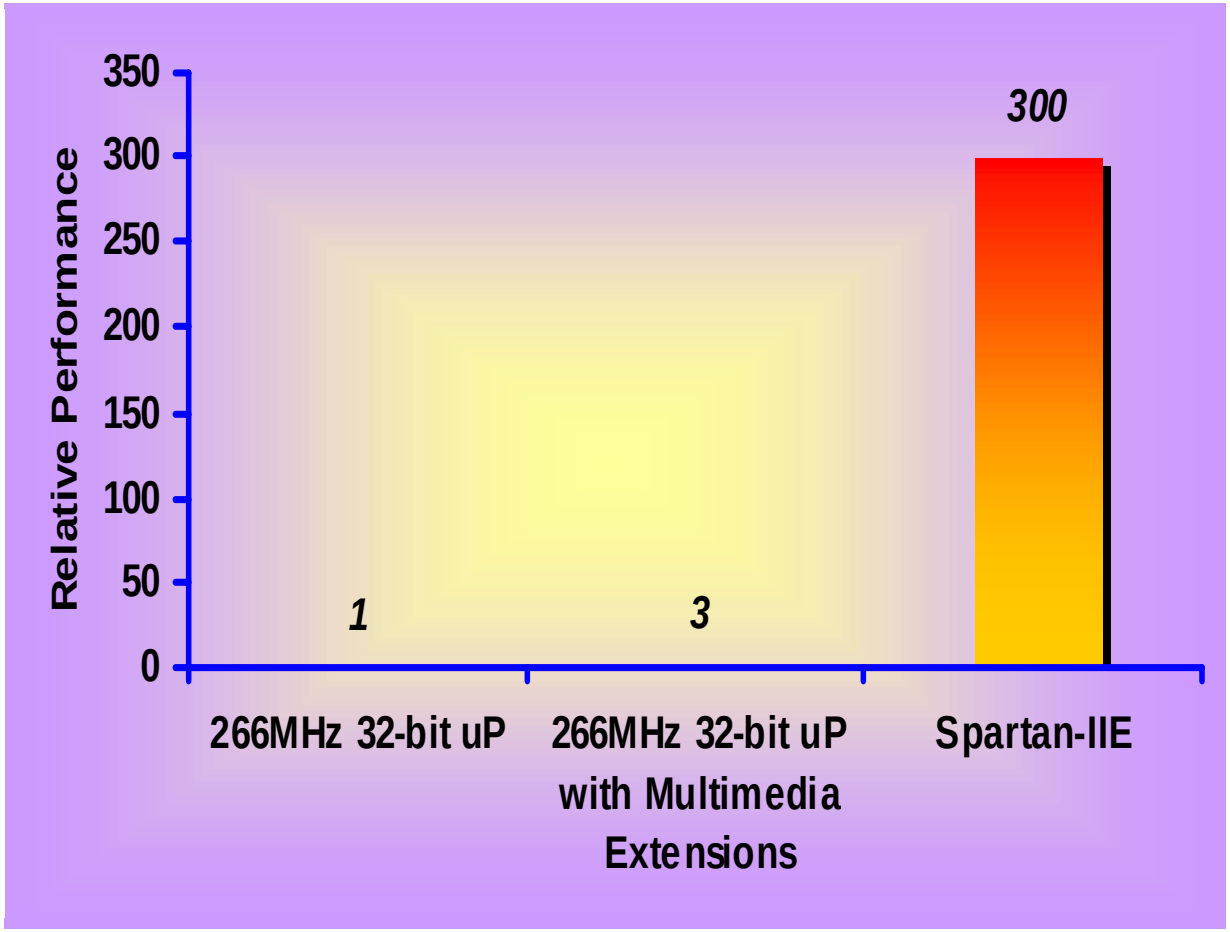
DCT/iDCT Core Overview



Half-Duplex Operation
Forward or Reverse, Not both simultaneously

- 2D transform decomposed into 2 1D - operations (Stage 1 and Stage 2)
- Intermediate results stored in Transpose Memory
- Forward DCT - 8-bit unsigned input, 11-bit signed output
- Inverse DCT - 11-bit signed input, 8-bit unsigned output
- Continuous streaming - one sample per cycle processing capability

Spartan-IIE DCT/IDCT Solution - Performance



LogiCore Implementation

Target Device	Spartan-IIE xc2s200E-7	Virtex-E xcv200e-8	Spartan II xc2s150-6
Speed	75 MHz (est.)	80 MHz	71.4 MHz
SDTV (27 MHz) Time Multiplexed Channels	3	3	2
HDTV (75 MHz) Time Multiplexed Channels	1	1	N/A
Size (Slices)	1759	1759	1728

Innovation by AMPHION

XILINX

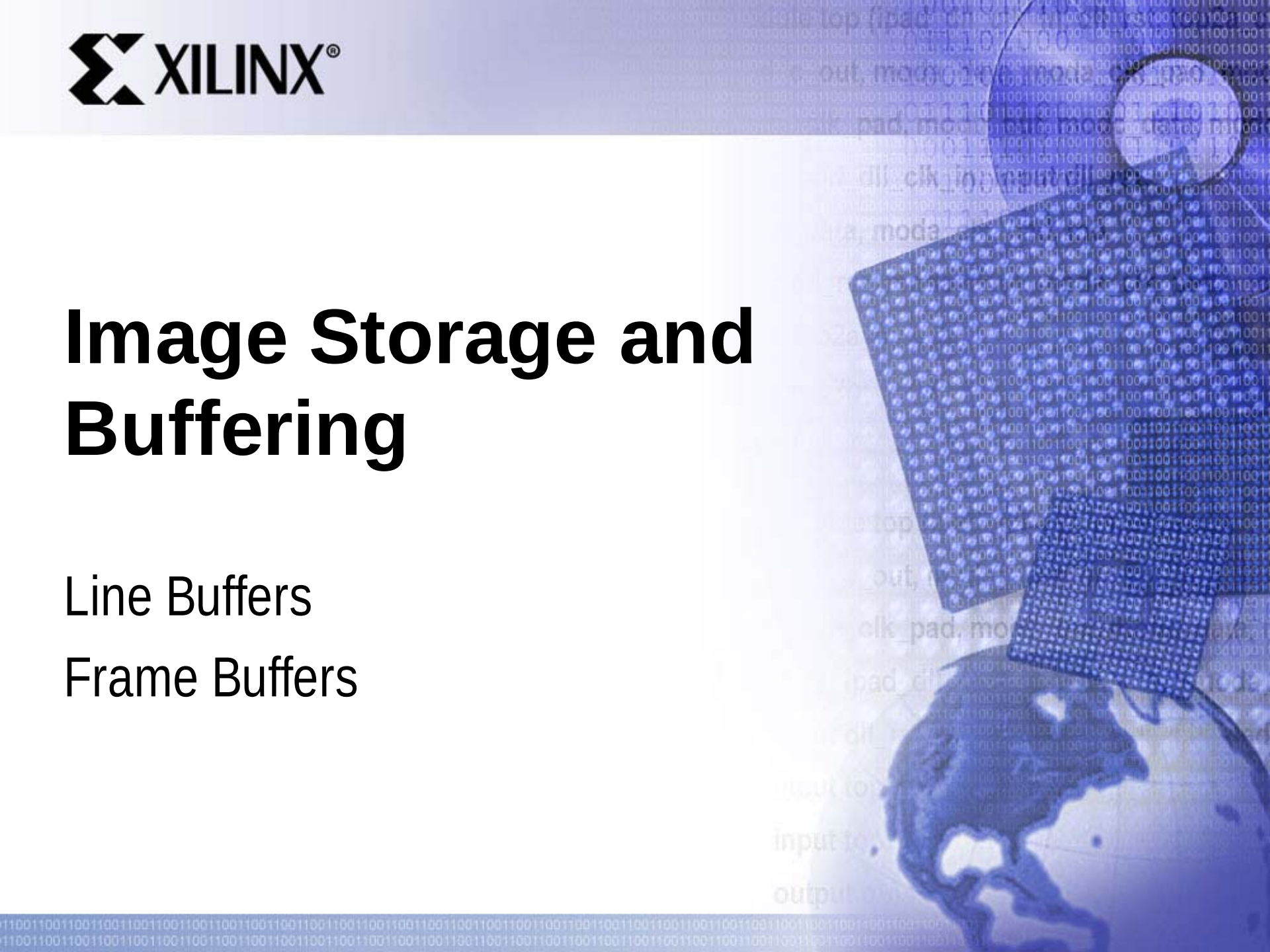


Image Storage and Buffering

Line Buffers

Frame Buffers

Line Buffering

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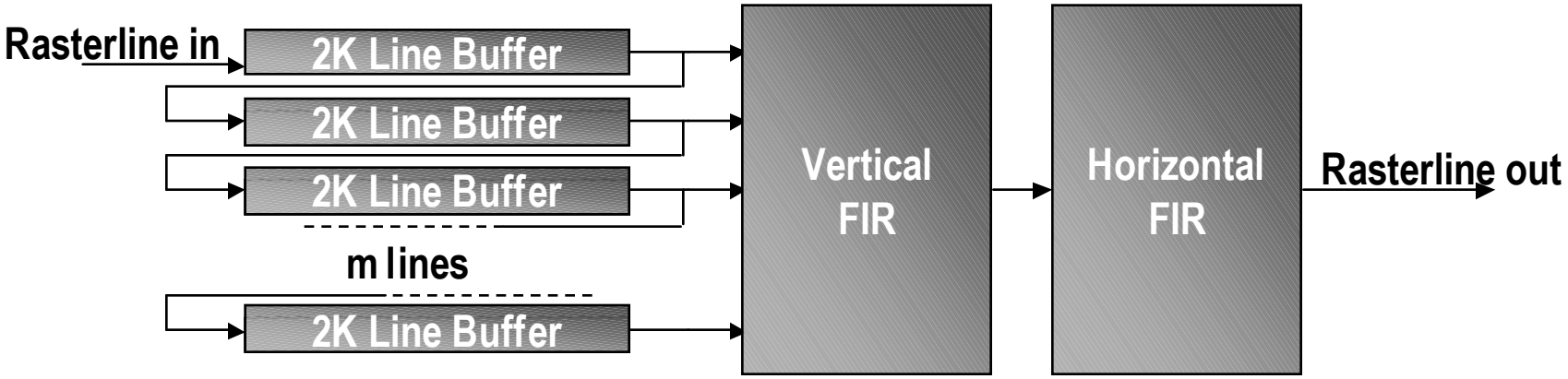
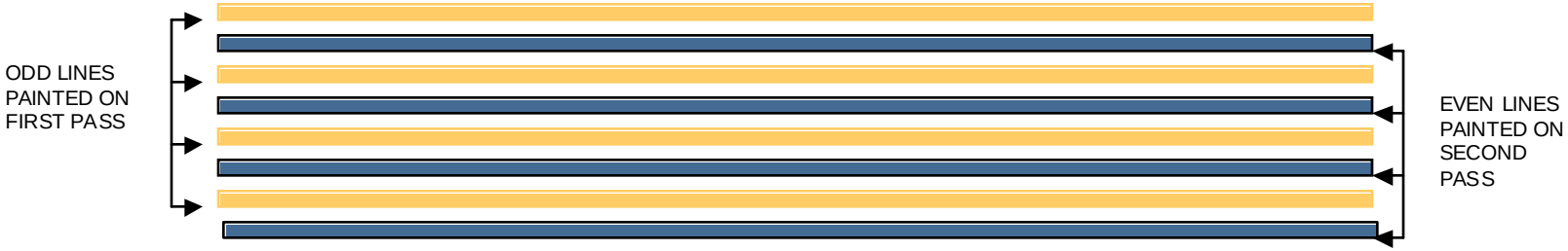


Scan Line Conversion

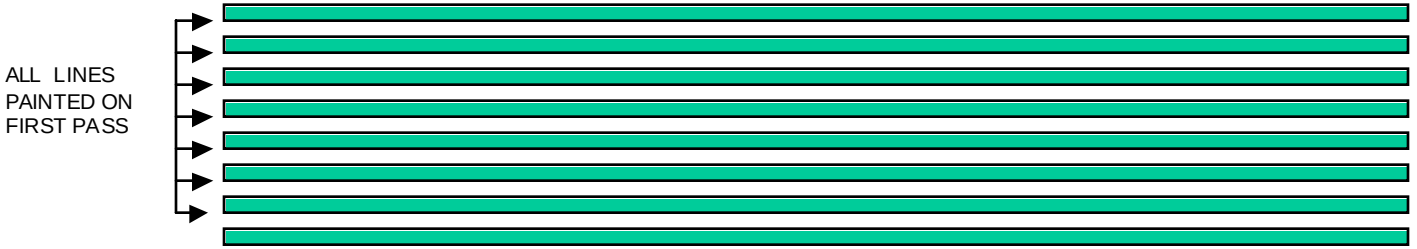
Interlacing/De-interlacing

Scan Line De-interlacing

- INTERLACE VIDEO (broadcast video)
  - Half the lines of a frame in a single pass (242 lines @ 30Hz)



PROGRESSIVE SCAN VIDEO (computer monitors)
All lines of a frame in a single pass (484 lines @ 60Hz)
MPEG works on progressive scanned images

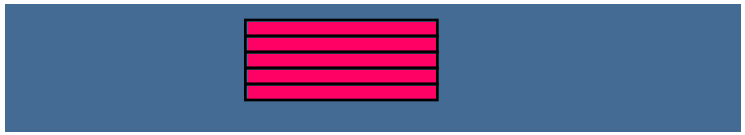


Scan Line De-interlacing

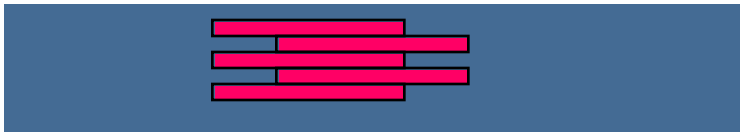
- De-interlacing (line doubling) is the process of converting interlaced video into progressive scan video.
  - 1. Scan Line Duplication from a single field
  - 2. Field Merge (2x resolution but motion problems)
  - 3. Scan Line Interpolation from a single field (only 1x resolution)
  - 4. Combination approach, field merge (non-moving), interpolate moving objects but difficult motion detection problem
  - 5. Scan Line Interpolation from a single frame

Scan Line De-interlacing

Field Merge Problems (Object in motion will have “double image”)

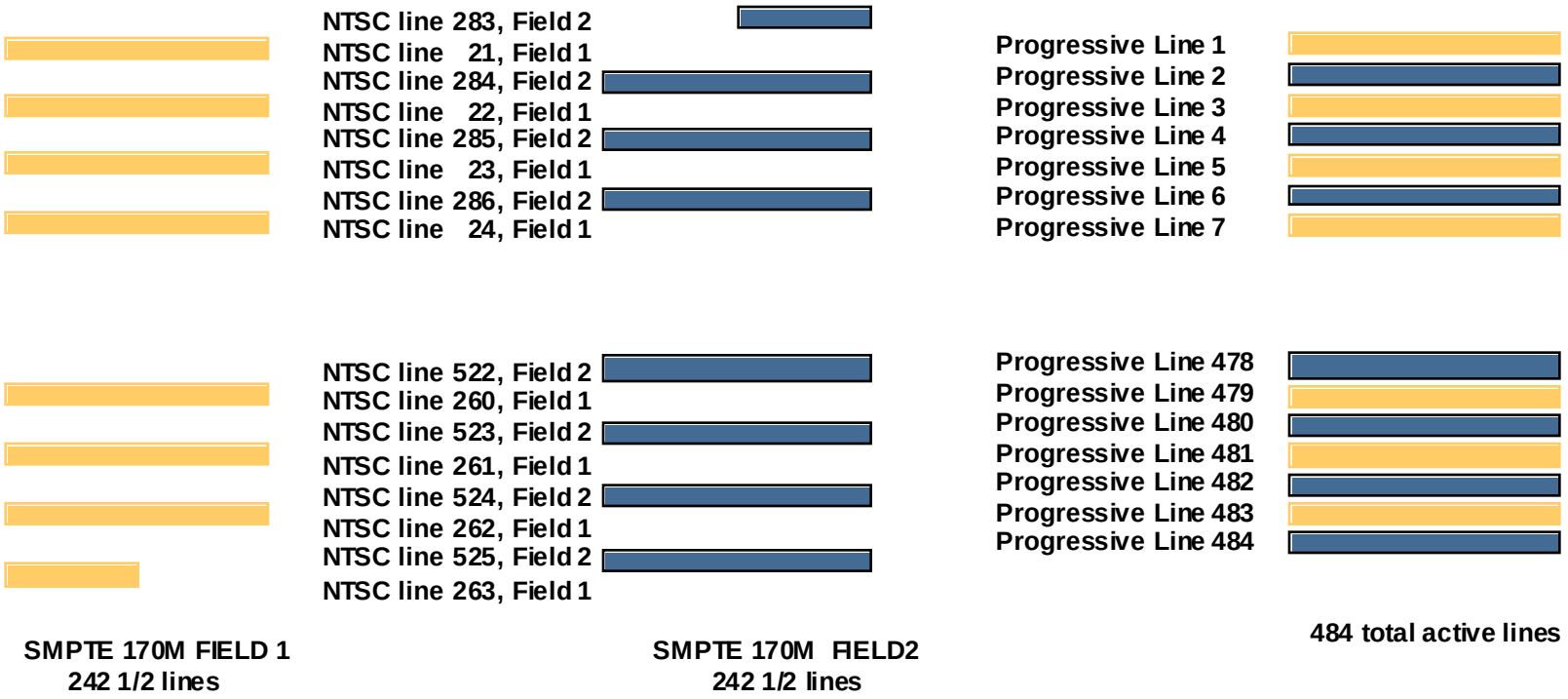


Object with no motion

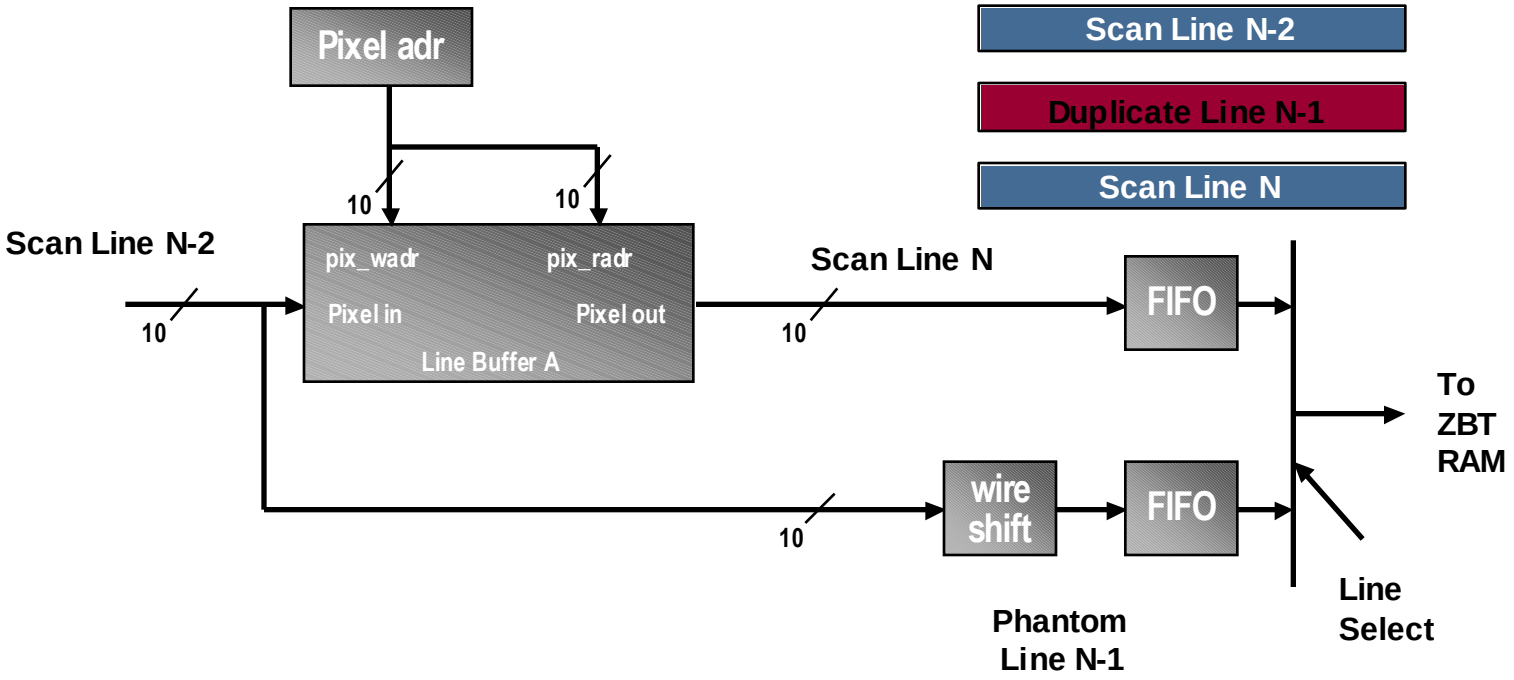


Object in motion alternate lines are displaced by horizontal motion

Scan Line De-interlacing (Blue = Field 2, Yellow = Field 1)

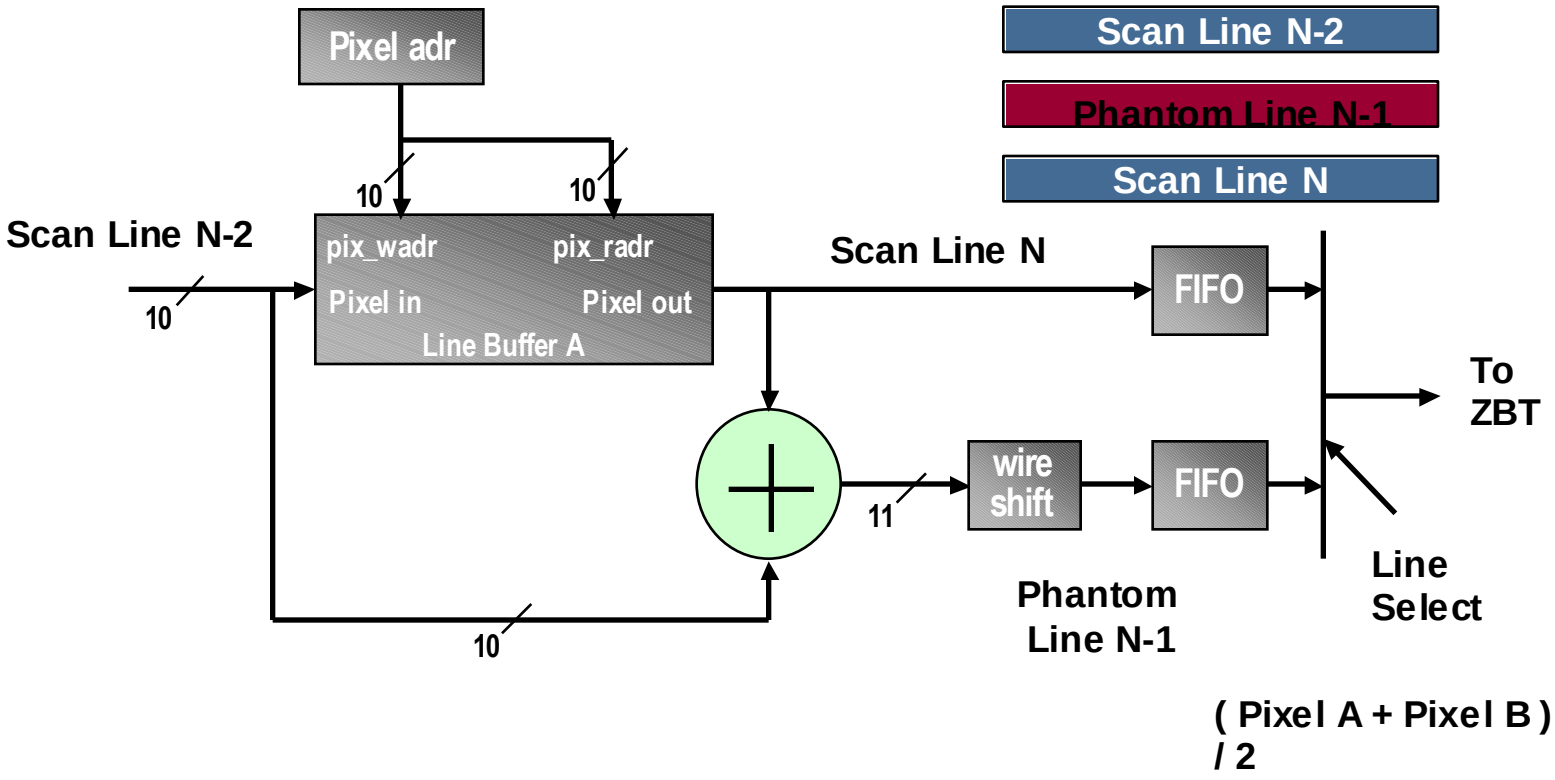


Scan Line De-interlacing Using Scan Line Duplication



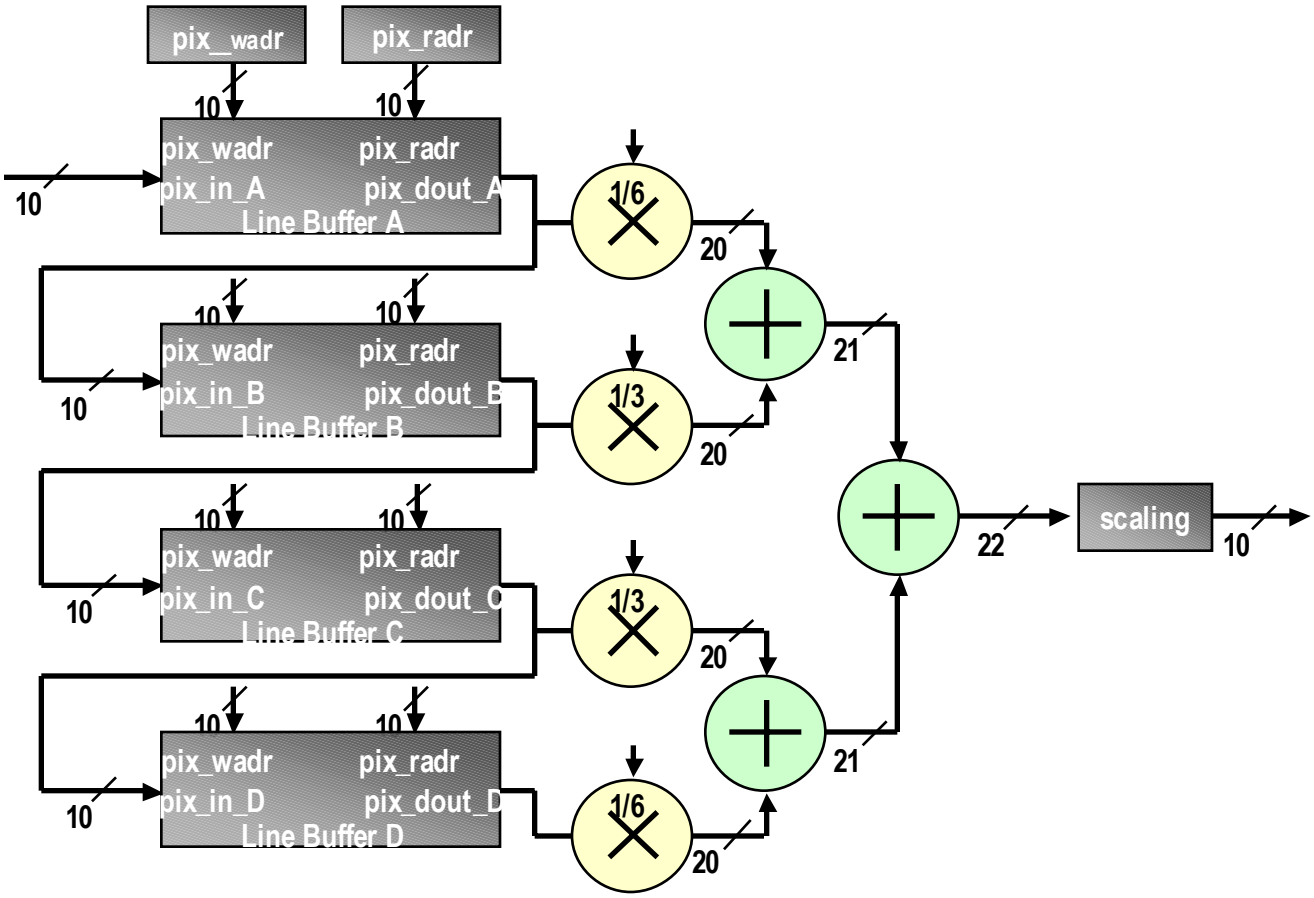
Block Diagram of a design to create a progressive image from duplicating lines from field lines

Scan Line De-interlacing Interpolating From 2 Field Lines



Block Diagram of a design to create a progressive image from interpolating 2 lines from field lines

Scan Line De-interlacing Interpolating From 4 Field Lines

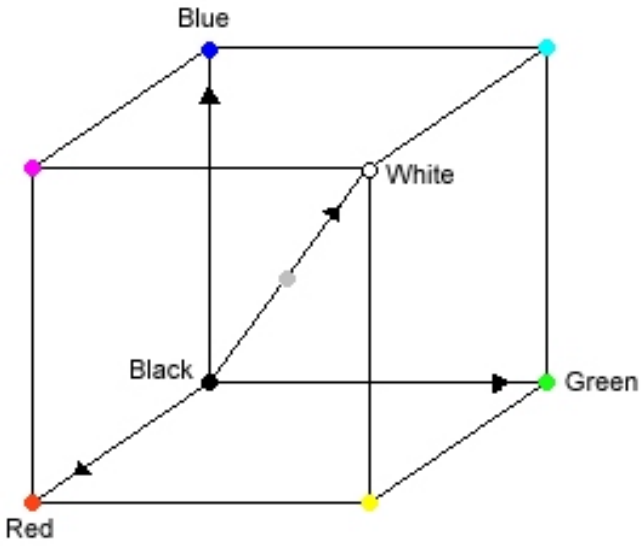


Block Diagram of a design to create a progressive image by interpolating 4 lines from field lines.

Color Space Conversion

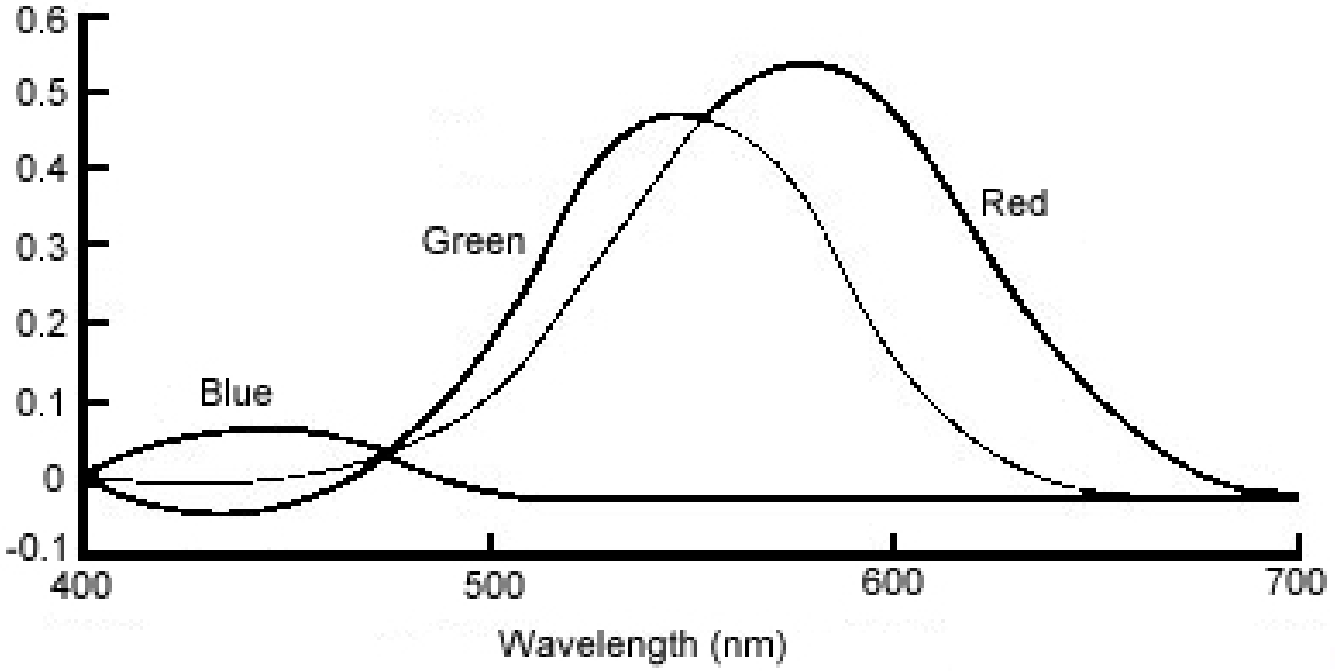
RGB Unity Color Space

- Mixtures of color components can be mapped into an RGB color space covering all variations from black (0xR + 0xG + 0xB) to white (1xR + 1xG + 1xB)



Spectral Response of Human Eye

- Green sensing cones in the human eye respond to most wavelengths in the light spectrum

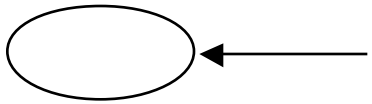


Luminance and Color Difference

- Pictures almost always represented as pixels on final medium
  - whether printed paper or TFT, PDP & CRT displays
- Pixels can be represented with 3 full bandwidth analog RGB components
  - Huge storage and transmission bandwidth requirements for high resolution, large format displays (up to 200 terabytes during post-production)
- Human eye is more receptive to brightness than it is to color
  - Full resolution of human vision is restricted to brightness variations
  - Color detail resolution is about a quarter that of brightness variations
  - Green objects will produce more stimulus than red objects of the same brightness, with blue objects producing the least
- A brightness/luma signal (Y) can be obtained by adding RGB values together which are weighted by relative eye response

Luminance and Color Difference

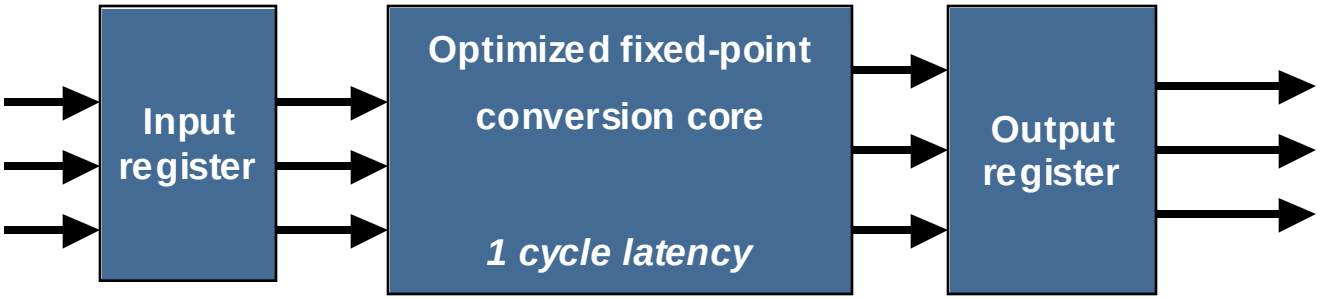
- ITU CCR 601 says Y = 0.299R + 0.587G + 0.114B
- To save bandwidth, color difference signals sent with luma rather than RGB
- Color difference possibilities
  - R-Y
  - B-Y
  - G-Y



As G contributes most to Y, this signal would be small and most susceptible to noise

- Simple maths can be used to reconstruct signals at the display

Color Space Converter Structure



- Fully synchronous
- Registered input and output, 1 internal pipeline stage
- Low latency (3 cycles)
- Continuous processing
- One 3-color conversion every clock cycle
- Internal 10-bit precision for accuracy
- Rounded to 8-bit outputs

Cores Available

CCIR 601 Standard

- RGB2YCrCb
- Y = 0.257×R' + 0.504×G' + 0.098×B' + 16
- Cr = 0.439×R' - 0.368×G' - 0.071×B' + 128
- Cb = -0.148×R' - 0.291×G' + 0.439×B' + 128
- YCrCb2RGB
- R'= 1.164×(Y-16) + 1.596×(Cr-128)
- G' = 1.164×(Y-16) - 0.813×(Cr-128) - 0.392×(Cb-128)
- B' = 1.164×(Y-16) + 2.017×(Cb-128)
- RGB2YUV
- Y = 0.299×R' + 0.587×G' + 0.114×B'
- U = -0.147×R' - 0.289×G' + 0.436×B'
- V = 0.615×R' - 0.515×G' - 0.100×B'
- YUV2RGB
- R' = Y + 1.140×V
- G' = Y - 0.394×U - 0.581×V
- B' = Y - 2.032×U

R'G'B' refers to gamma corrected RGB

Xilinx Color Space LogiCore Solutions

Product/Cores	YCrCb2RGB	RGB2YCrCb	YUV2RGB	RGB2YUV
Size: Virtex / Virtex-E	194 Slices	217 Slices	158 Slices	245 Slices
Synchronous	Full	Full	Full	Full
Supported Family	Spartan Spartan-II Spartan-IIE Virtex Virtex-E	Spartan-II Spartan-IIE Virtex Virtex-E	Spartan Spartan-II Spartan-IIE Virtex Virtex-E	Spartan-II Spartan-IIE Virtex Virtex-E
Latency	3 Clock Cycles	3 Clock Cycles	3 Clock Cycles	3 Clock Cycles
Performance: Spartan-IIE	>95 MHz	>90 MHz	>90MHz	>110MHz
SDTV (27 MHz) Time Multiplexed Channels	7 (Spartan-IIE)	3 (Spartan-IIE)	8 (Spartan-IIE)	3 (Spartan-IIE)
HDTV (75 MHz) Time Multiplexed	2 (Spartan-IIE)	1 (Spartan-IIE)	3 (Spartan-IIE)	1 (Spartan-IIE)
Cost	$995	$995	$995	$995

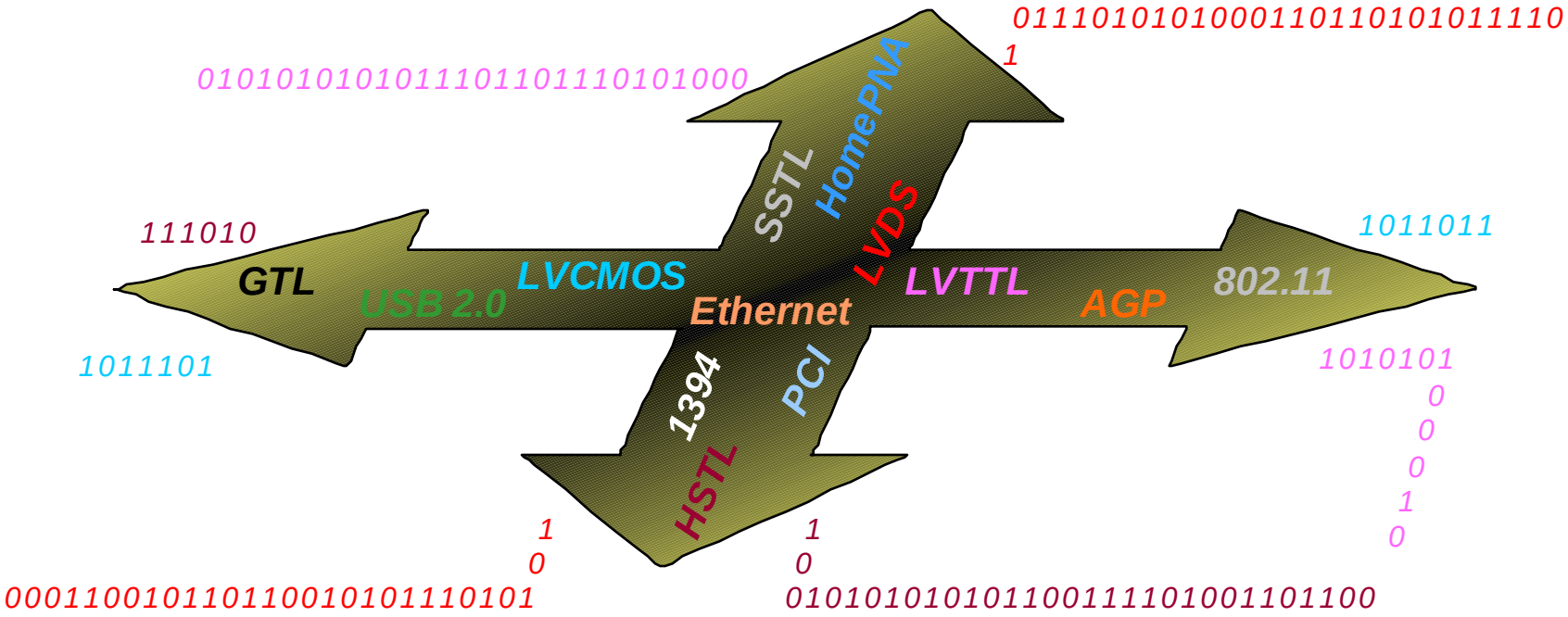
Innovation by AMPHION™

XILINX®

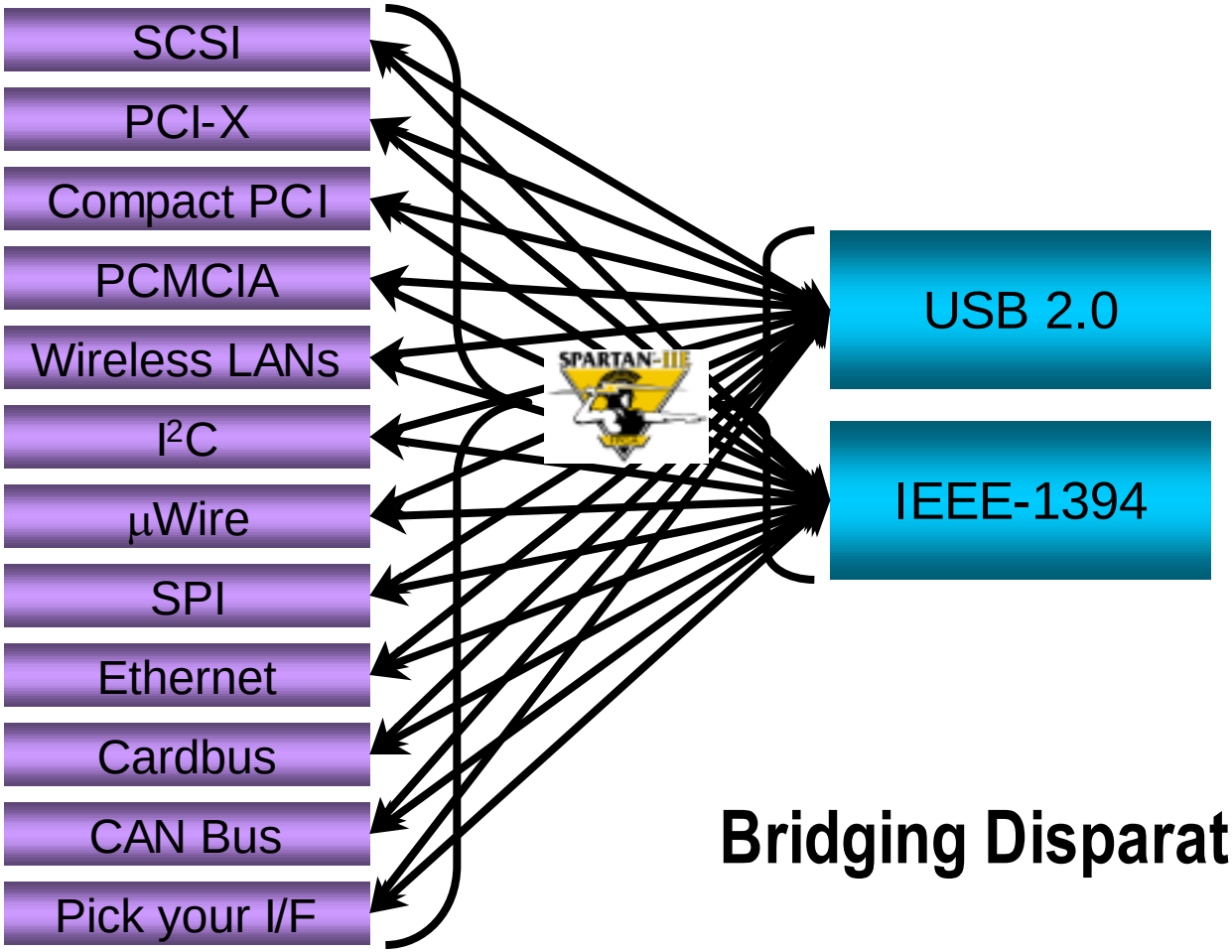
Xilinx Color Space Solutions

- LogiCORE Color Space Converters provide straight forward, accurate high performance conversion usable in a wide range of video/image applications
- More area efficient than existing cores
- Speeds ensure operation in all TV and HDTV applications
- Available through Xilinx Coregen

Component Interconnectivity

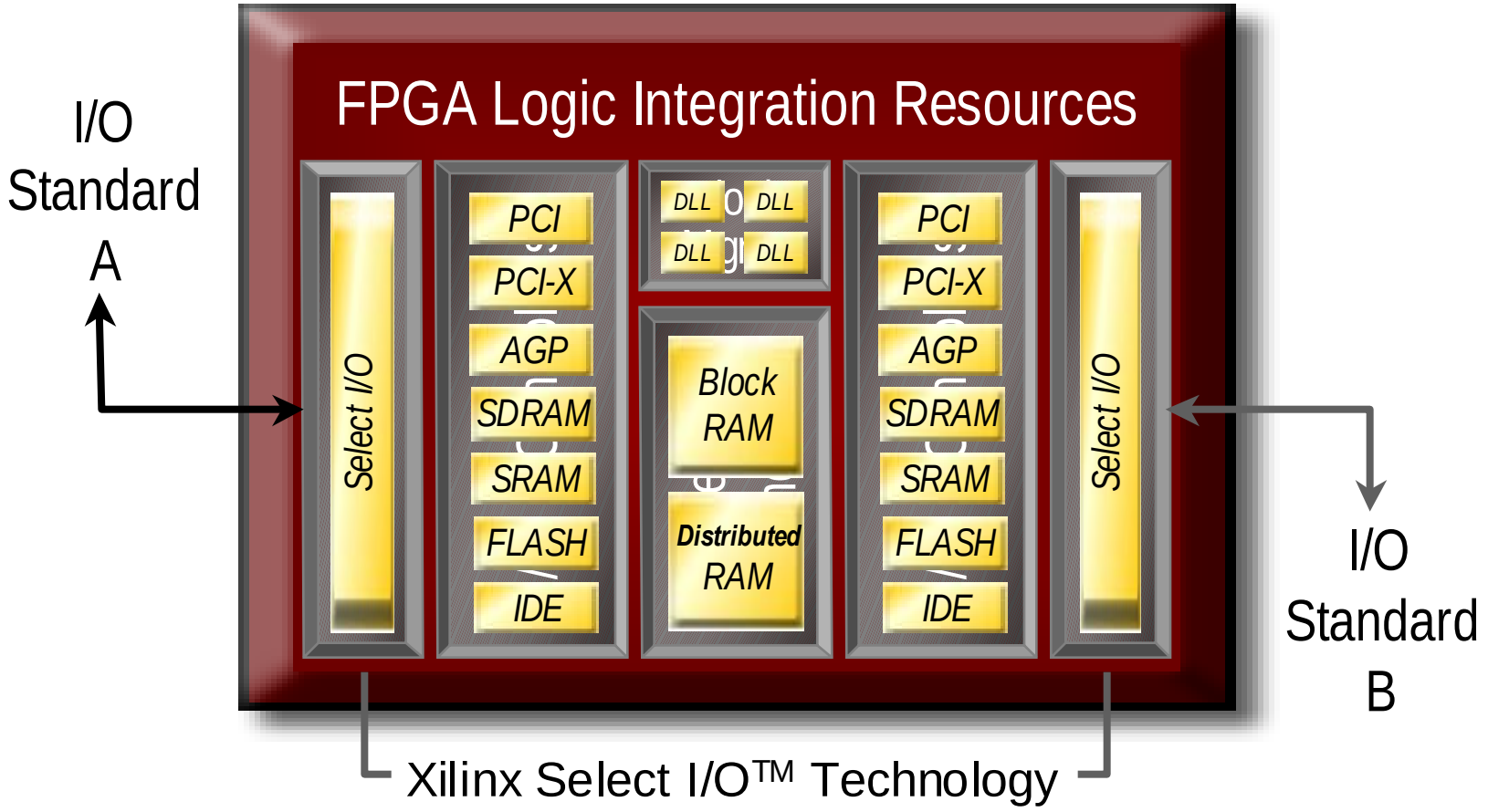


Universal System Interface



Bridging Disparate Protocols

Component Integration
Design Flexibility



Chip to backplane	Chip to Memory	Chip to Chip	LVDS
• PCI 33MHz 3.3V	• HSTL-I, -III, -IV	• LVTTL	• LVDS
• PCI 33MHz 5.0V	• SSTL3-I, -II	• LVCMOS	• BLVDS
• PCI 66MHz 3.3V	• SSTL2-I, -II		• LVPECL
• GTL, GTL+, AGP	• CTT		

Supervisory System Control

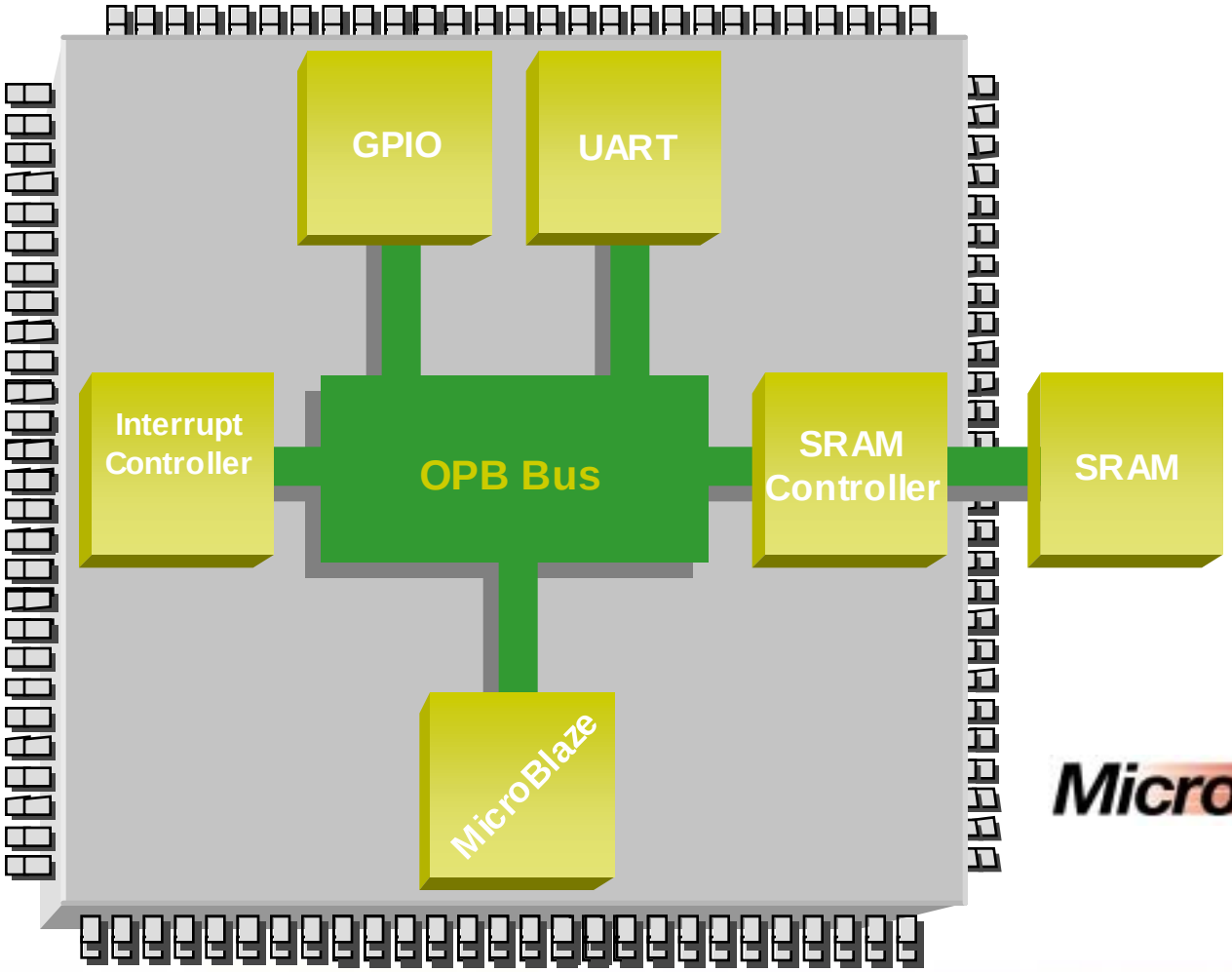
MicroBlaze

- 32-bit fully synthesized RISC processor
- Fast - 70 D-MIPS now
  - Twice the performance at half the logic area vs. competition
- Supported by an integrated IP library
  - Timer/Counter Block
  - Watchdog Timer/Timebase
  - Interrupt Controller
  - 16550/16450/Lite UART
  - ZBT Memory Controller
  - SRAM Controller
  - Flash Memory Controller
  - IIC*
  - SPI*
  - Ethernet 10/100 MAC*
  - More to come

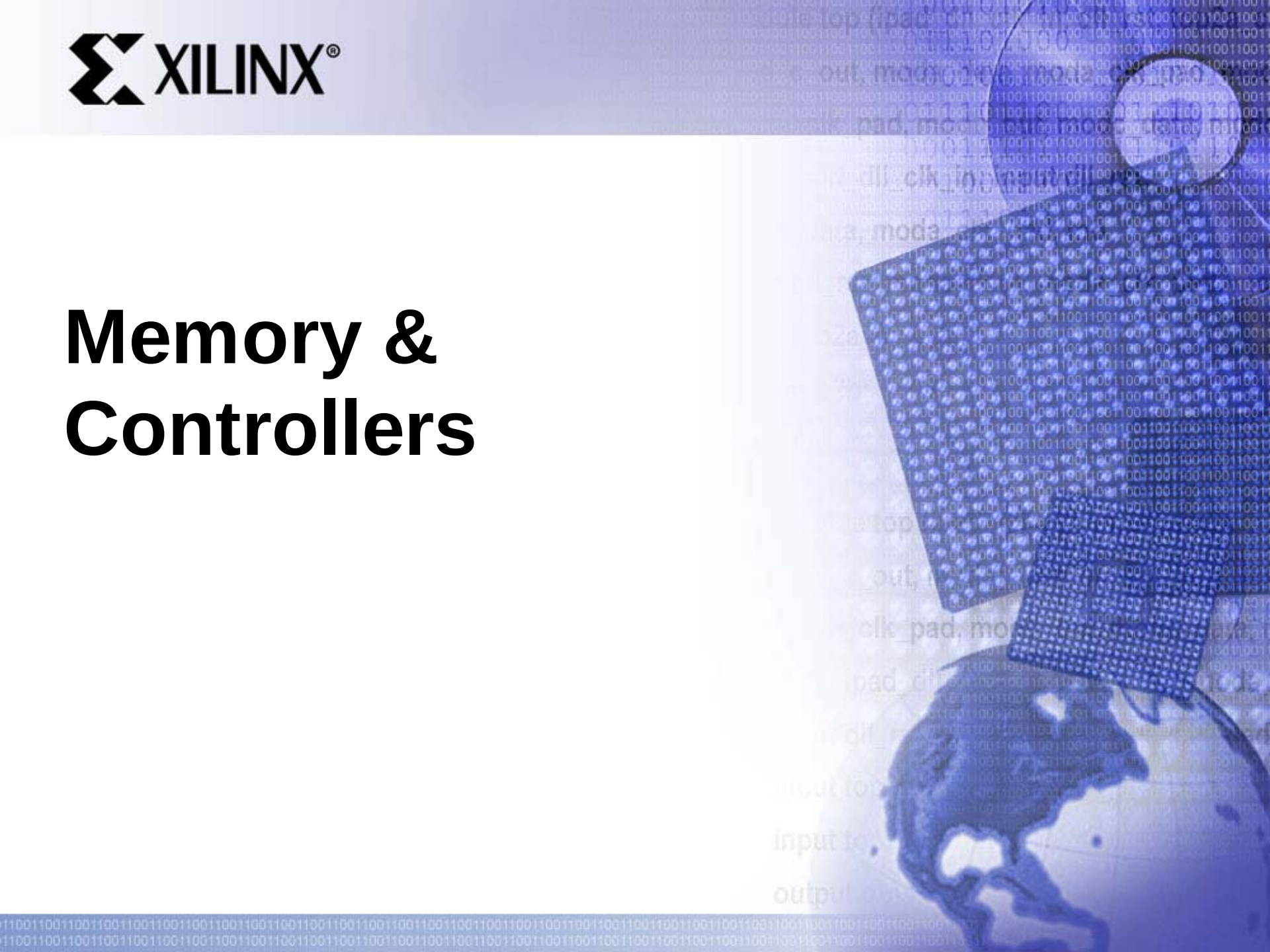
MicroBlaze

* Licensed for a fee

MicroBlaze in Spartan-IIE



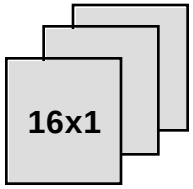
MicroBlaze


XILINX®
Memory &
Controllers

Spartan-IIE Memory Solutions

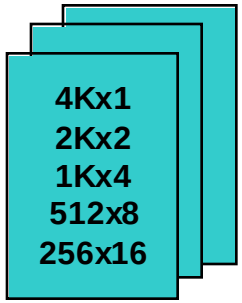
Memory Corner
Free Reference Designs

Distributed RAM



DSP Coefficients
Small FIFOs

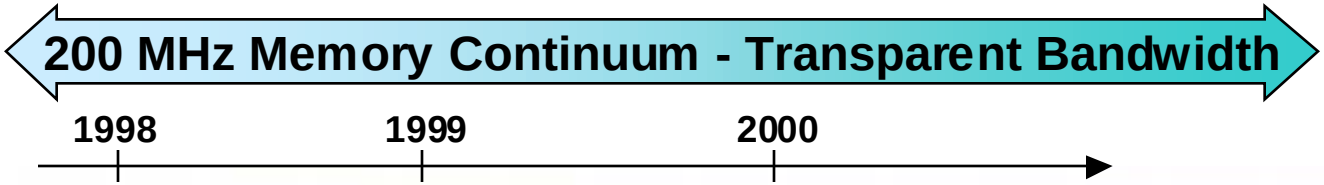
Block RAM



Large FIFOs
Video Line Buffers
Cache Tag Memory

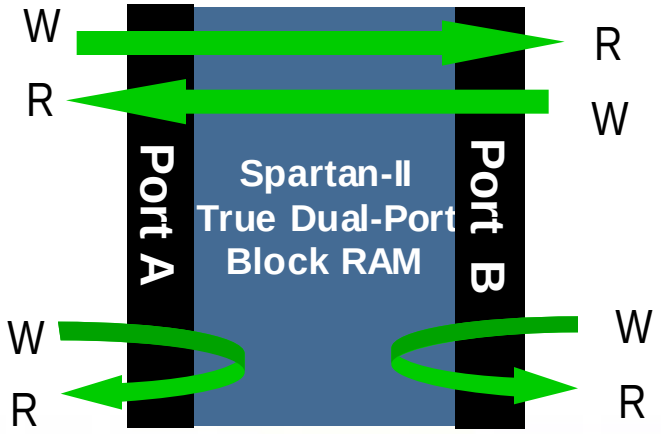
External Memory Interface

SDRAM
SGRAM
PB SRAM
DDR SRAM
ZBT SRAM
QDR SRAM



Spartan-IIE Block RAM

- True Dual-port Static RAM - 4K bits
  - Independently configurable port data width
    - 4K x 1; 2K x 2; 1K x 4; 512 x 8; 256 x 16
  - Fast synchronous read and write
    - 2.5-ns clock-to-output with 1-ns input address/data setup



Data Flow	Spartan-II
A to B	Yes
B to A	Yes
A to A	Yes
B to B	Yes

Spartan-IIE Memory Controllers

- Spartan-IIE FPGAs
  - Unique and extensive features, flexible architecture, low cost
- Memory controller for interface to different types of SRAM, DRAM & Flash memory
  - Xilinx provides FREE VHDL source code for implementing the memory controllers in Spartan-II

Memory Controller Reference Designs

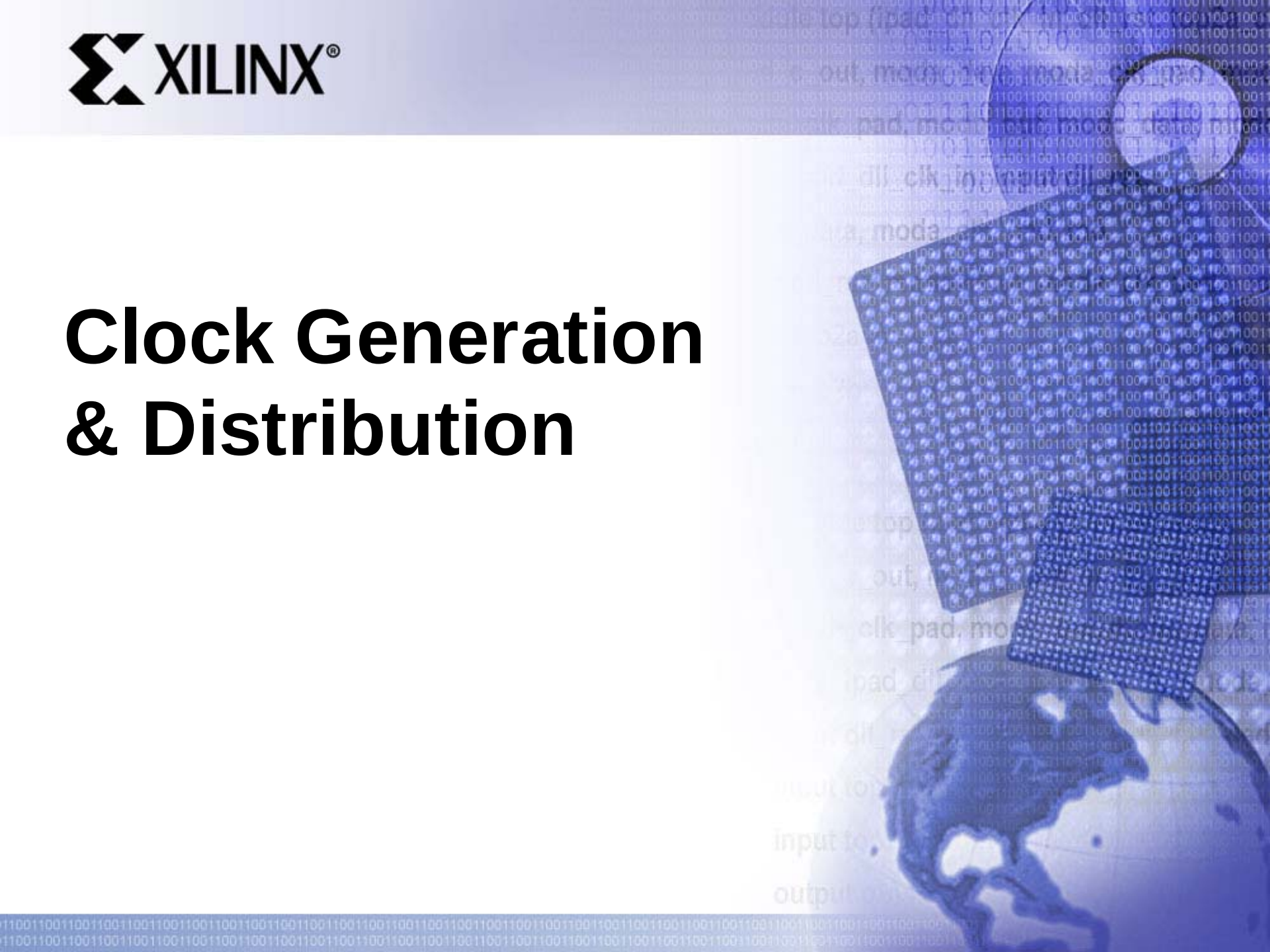
- DRAM reference designs
  - 64-bit DDR DRAM controller
  - 16-bit DDR DRAM controller
  - SDRAM controller
- SRAM reference designs
  - ZBT SRAM controller
  - QDR SRAM controller
- Flash controller
  - NOR / NAND flash controller
- Embedded memory reference designs
  - CAM for ATM applications
  - CAM using shift registers
  - CAM using Block SelectRAM
  - Data-width conversion FIFO
  - 170MHz FIFO for Virtex
  - High speed FIFO for Spartan-II

These Reference Designs are Available for Immediate Download at the Memory Corner

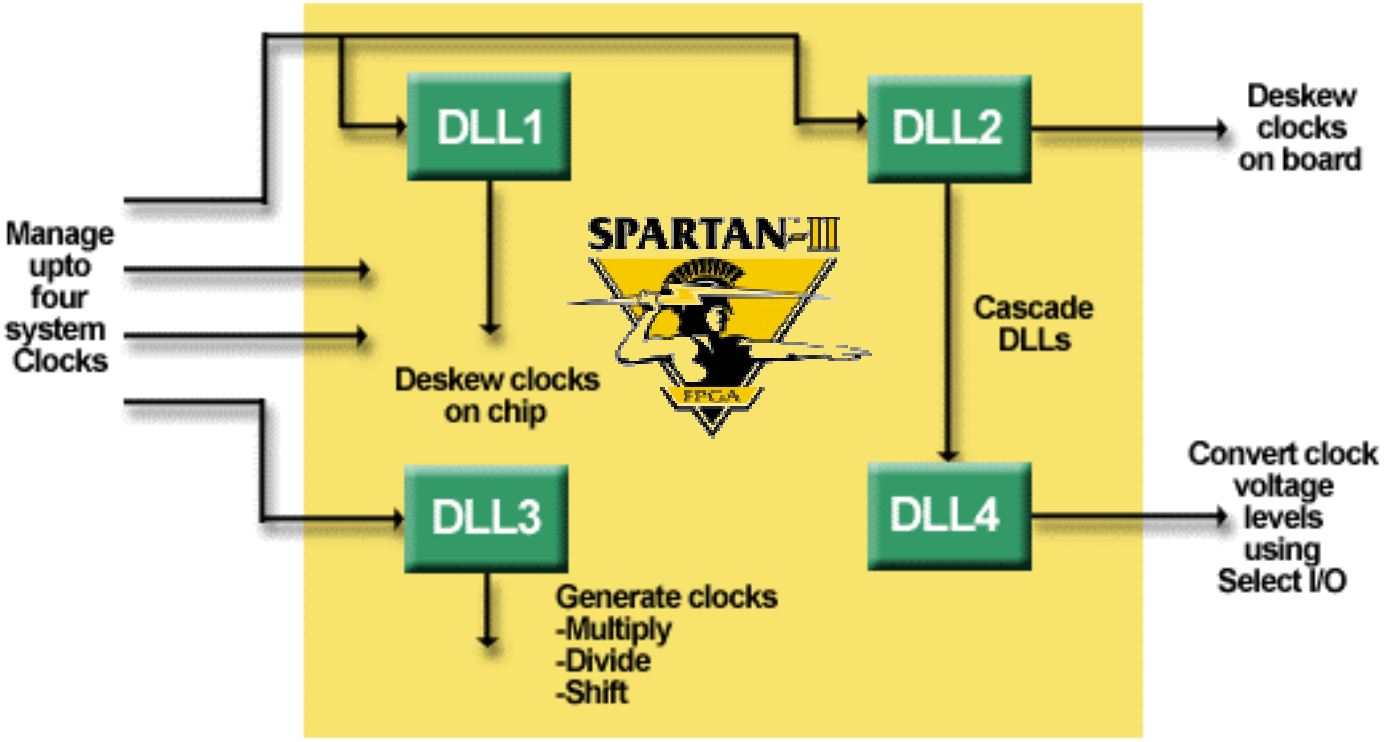
Memory Corner

- Collaboration between Xilinx and major memory vendors to provide comprehensive web-based memory solutions
  - Free reference designs (VHDL/Verilog)
  - SRAM, DRAM & embedded FPGA memory solutions
  - Data sheets, app notes, tutorials, FAQs, design guidelines

Clock Generation & Distribution

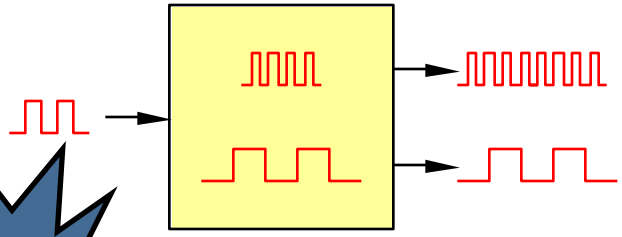


Spartan-II Clock Management



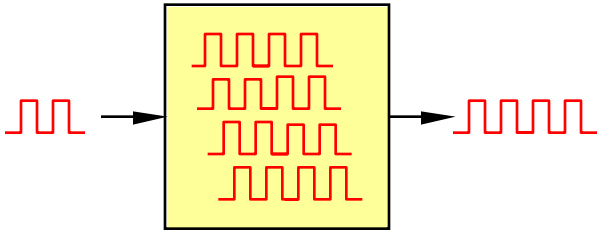
Delay Locked Loops Lower Memory and Board Costs

DLL Capabilities (4 Per Device)



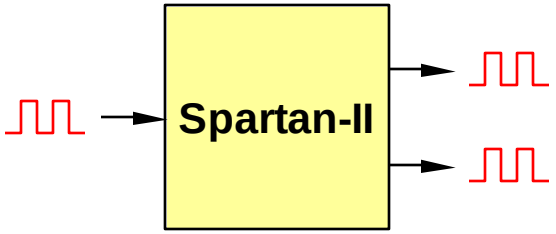
EMI Savings

Clock Multiplication & Division
For Use Internally Or Externally
Value - Slower Clock on PCB
Duty Cycle Correction



Clock Phase Synthesis Internally Or Externally
Value - Faster State Machines, Double edged clocking for DDR/QDR Memories

Speedup T_{c2o}
Zero-Delay Internal Clock Buffer
Value - Allows Use of Cheaper Memory



Clock Mirror
Zero-Delay Board Clock Buffer
Value - Reduce Board Delay, Reconstruct Noisy Backplane Clock

Clock Generation and Distribution

- Spartan-IIE DLL circuits provide full clock management solution
- Clock generation
  - Synthesizing many clocks from a single reference crystal or clock
- Clock buffering and distribution
  - Providing multiple copies of a single clock
  - SDRAM clocks
- Spread spectrum clocks for EMI reduction
  - DLL circuits allow tolerance for ±2.5% variance

Xilinx Programmable Logic Solutions

The Xilinx Product Portfolio

High Performance
High Density

Virtex, Virtex-E,
Virtex-EM, Virtex-II,
Virtex-II Platform FPGA

High Volume
Low Cost

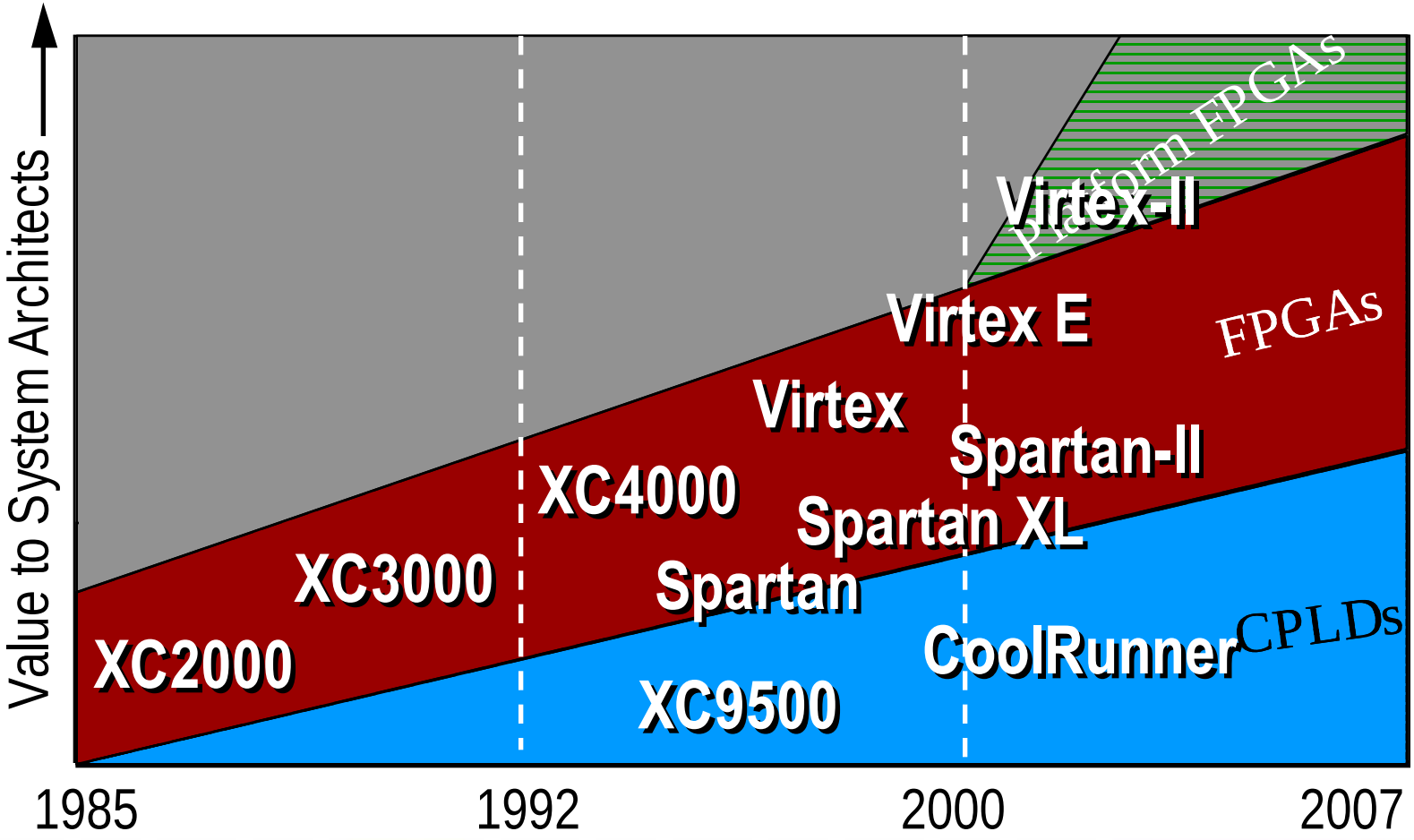
Spartan, Spartan XL,
Spartan-II, Spartan-IIE

Low Power
Low Cost

XC9500, XC9500XV,
XC9500XL, CoolRunner
XPLA3

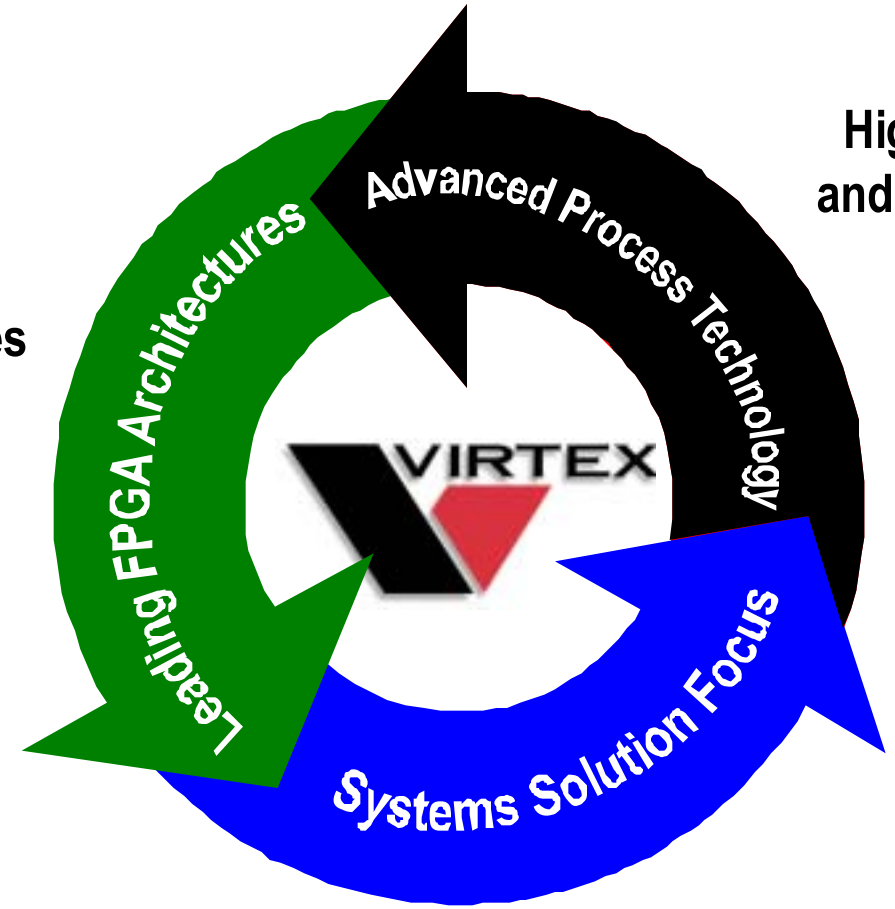
Software and IP Core Solutions

The Evolution of Xilinx Programmable Logic



Xilinx Virtex Series FPGAs

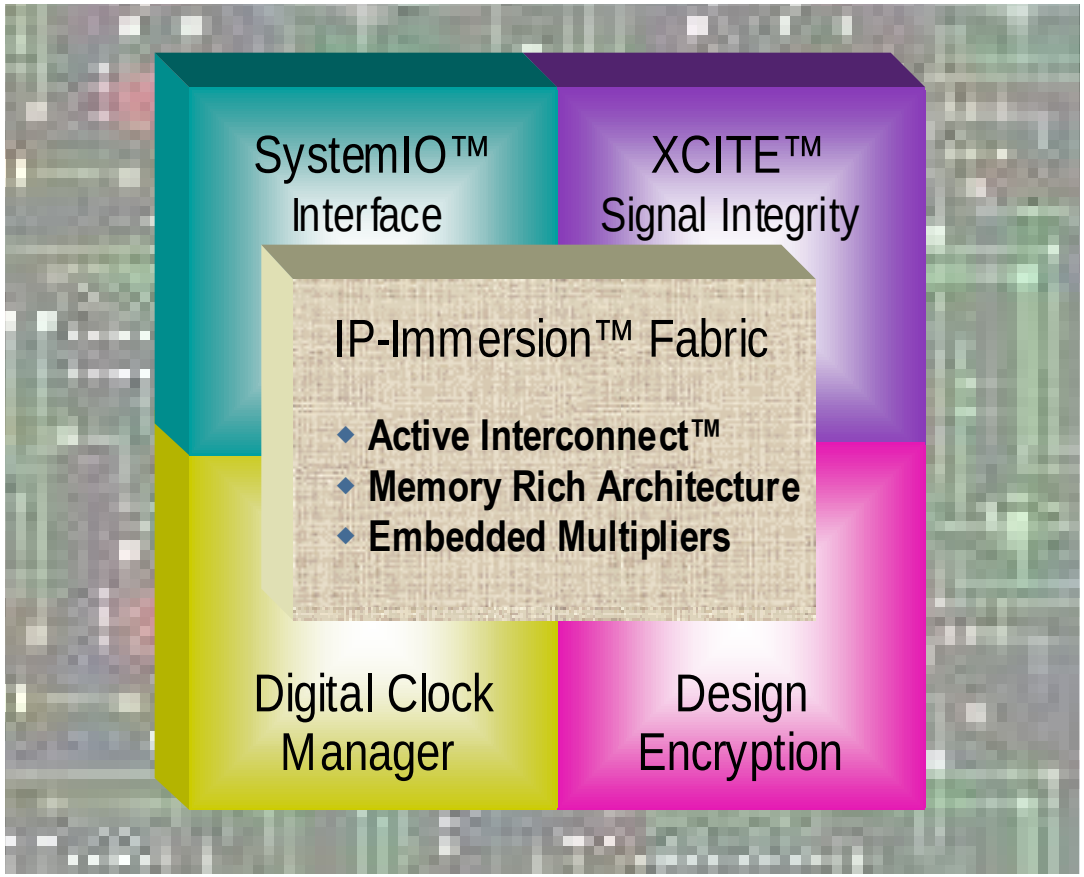
Maximum
Performance
Full Featured
Software and Cores



Highest Density
and Fastest Speed
Grades

Ever Increasing Levels of Integration

Virtex-II First Platform FPGA



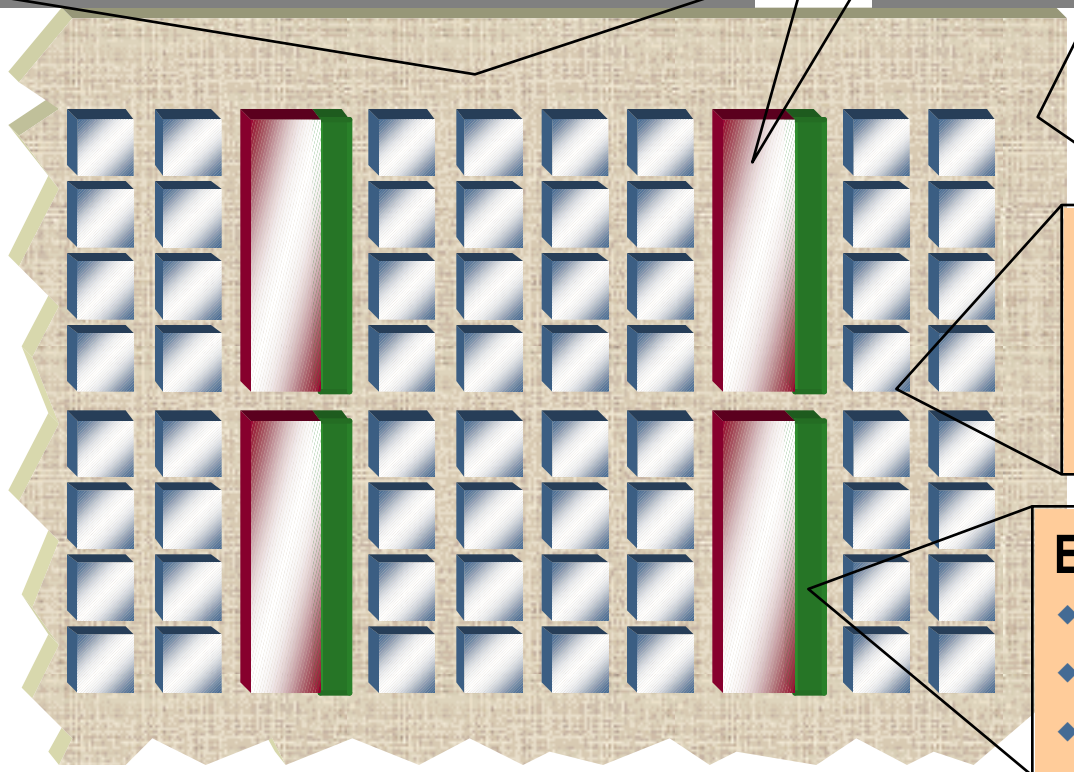
VIRTEX-II

XILINX

Virtex-II Fabric Features

Active Interconnect™ Technology
- Fast, predictable routing delays
- Efficient 4th gen. segmented routing

True Dual-Port™ Block RAM
- Higher capacity 18Kb block
- 2 R/W ports with x1 to x36 widths



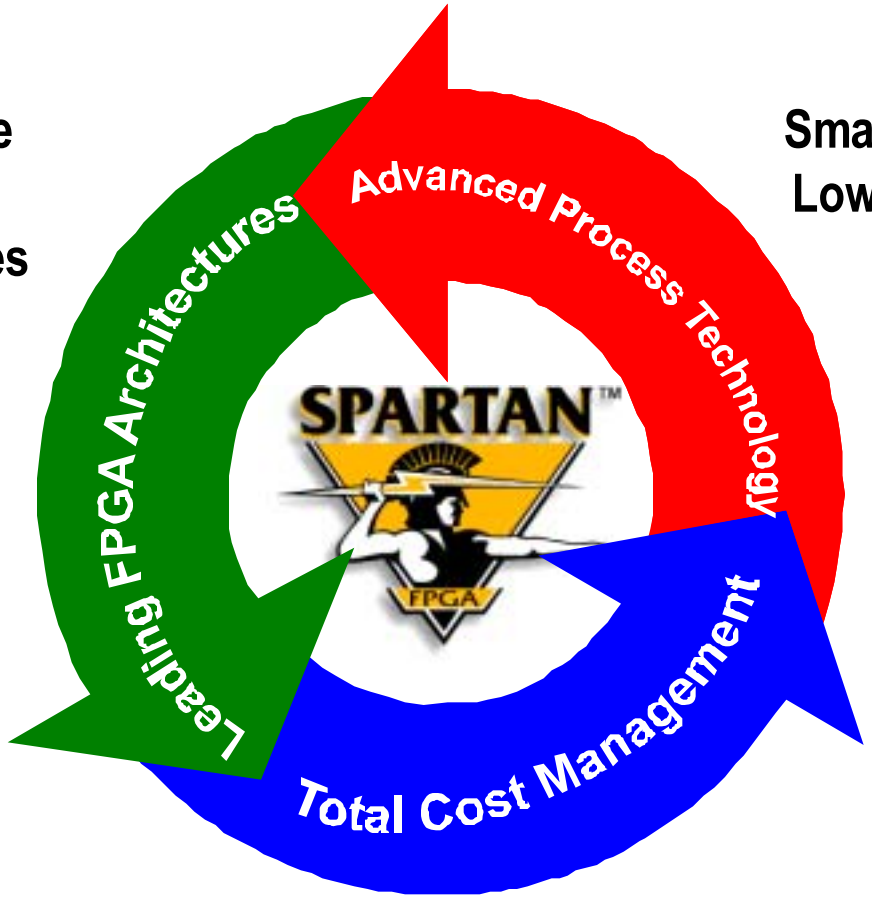
16 Global Clocks

Powerful New CLBs
- 8 LUTs per CLB
- 128b distributed memory
- Wide functions (32:1 mux)

Embedded Multipliers
- 18b x 18b signed multiplier
- 100+MHz registered multiplies
- <1us 1024-point FFT

Xilinx Spartan Series FPGAs

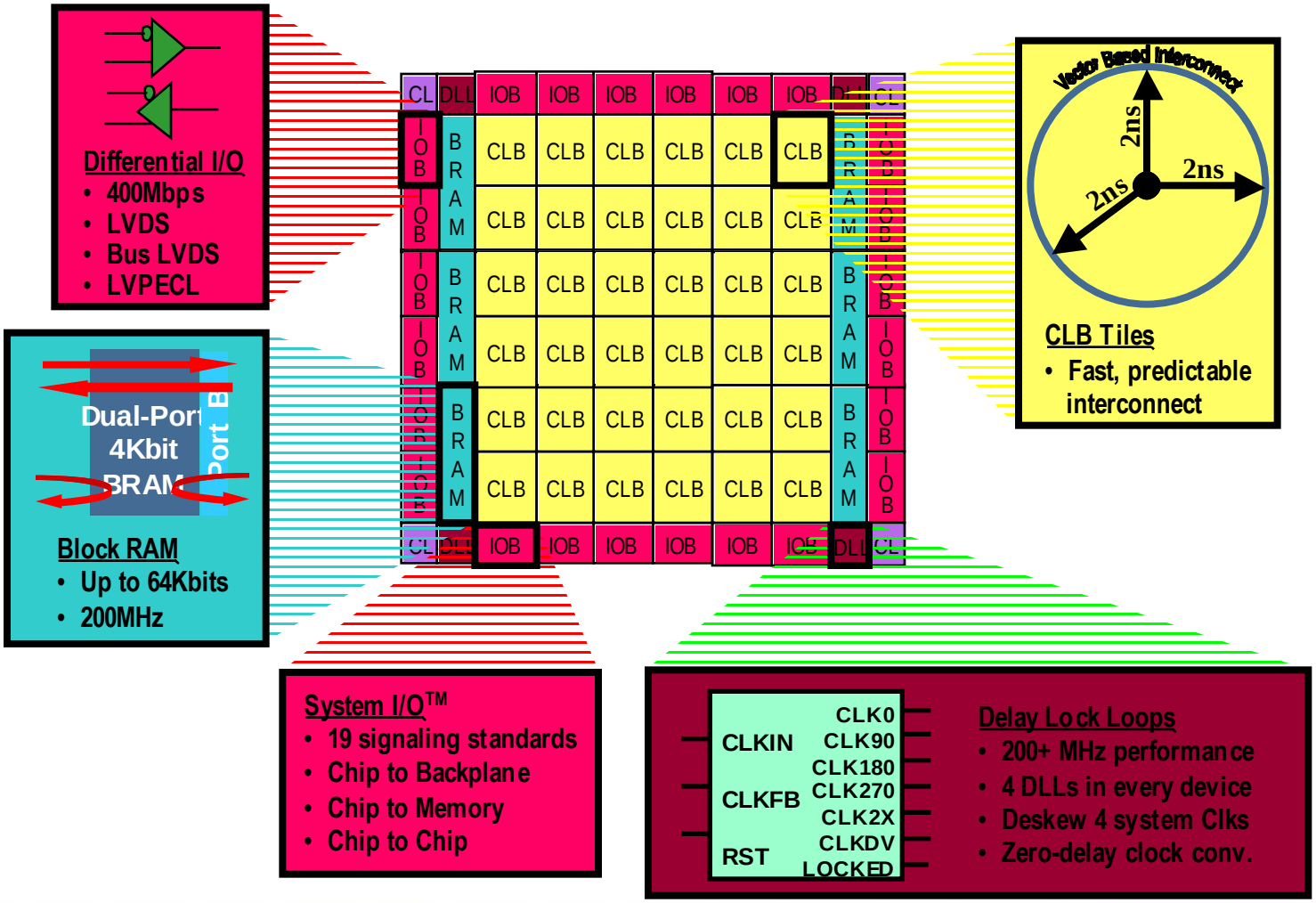
High Performance
System Features
Software and Cores



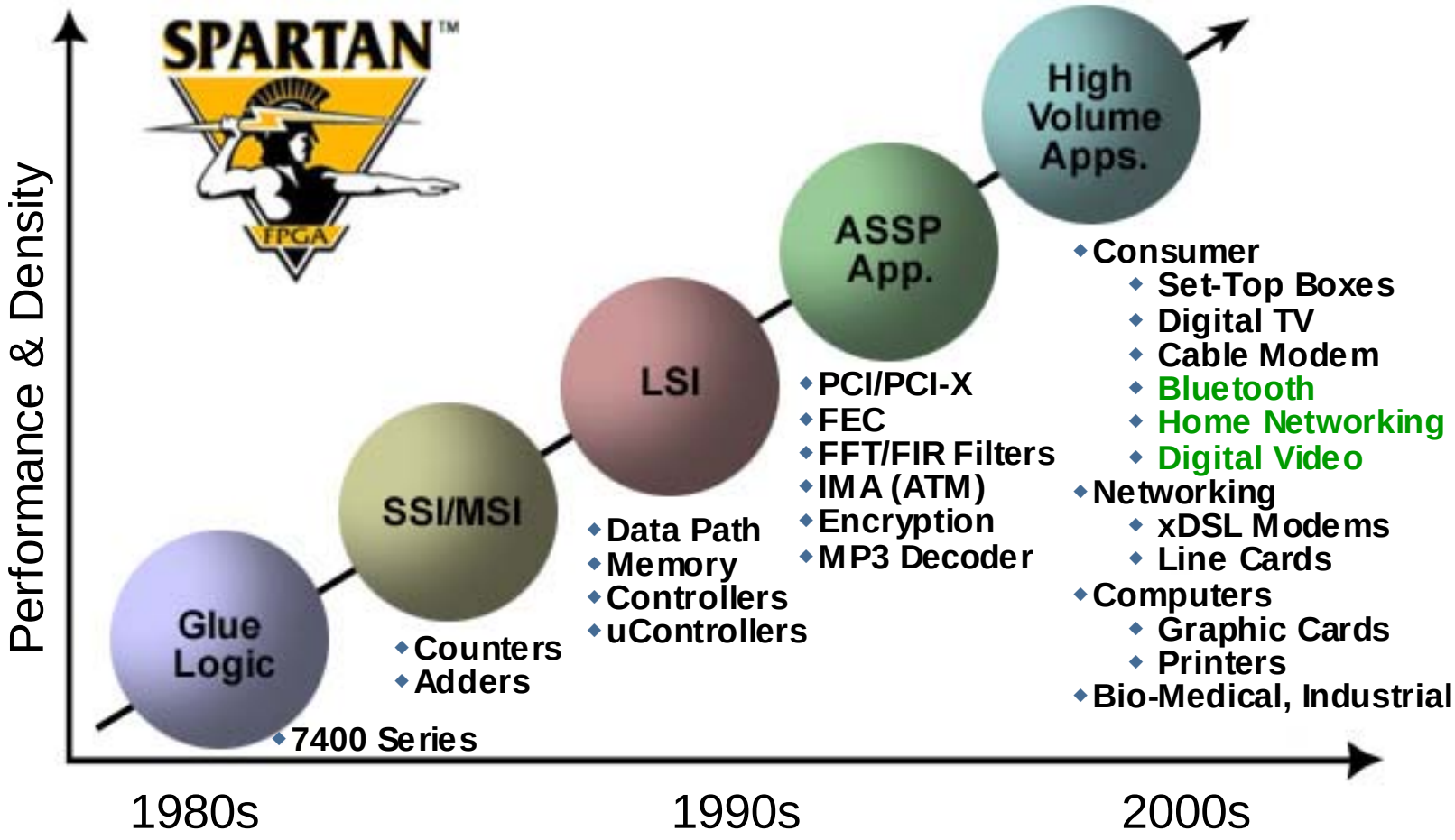
Smallest Die Size
Lowest Possible
Cost

Low Cost Plastic Packages Streamlined Testing

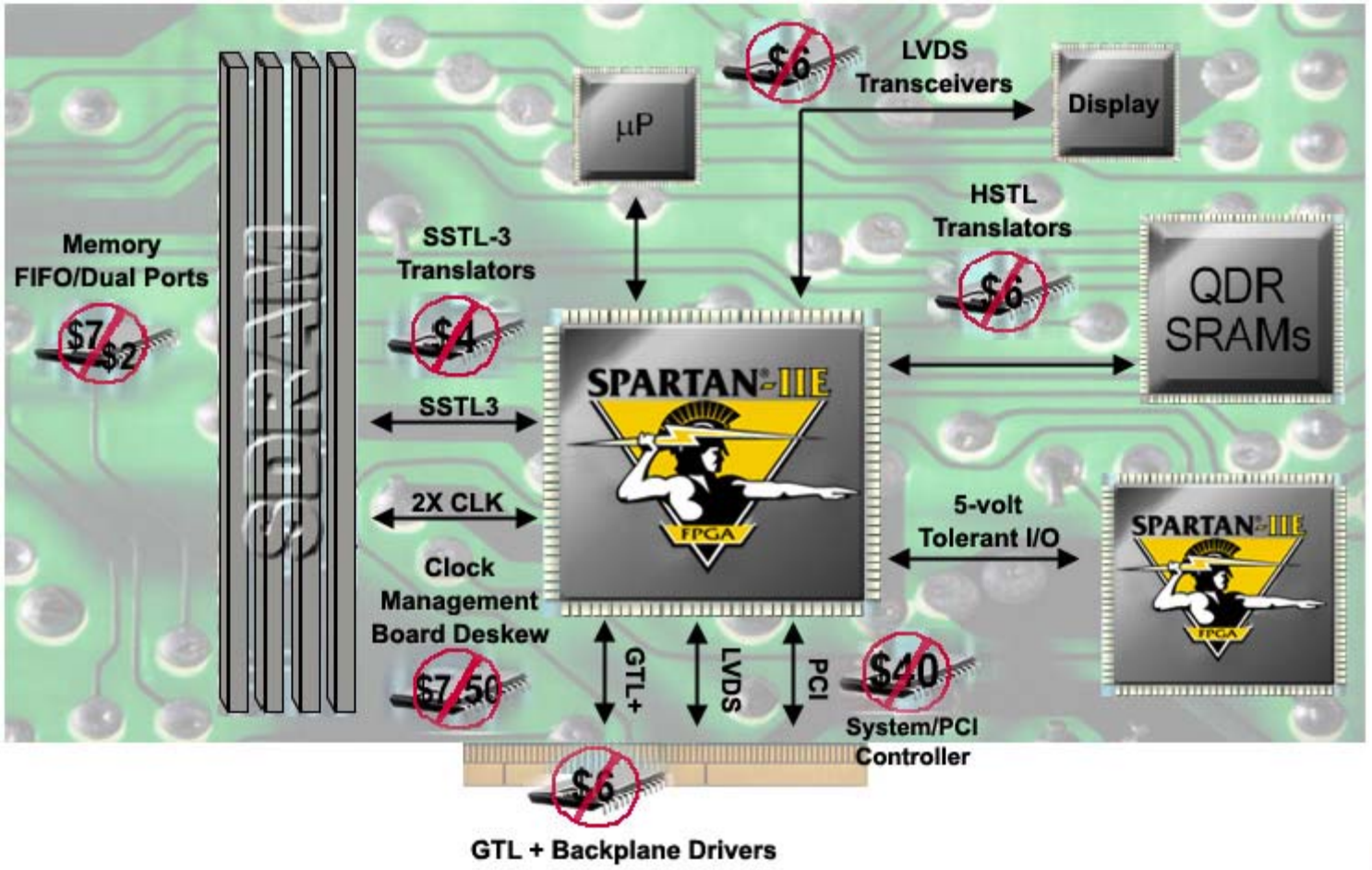
Spartan-IIE Technology



FPGA Application Trends

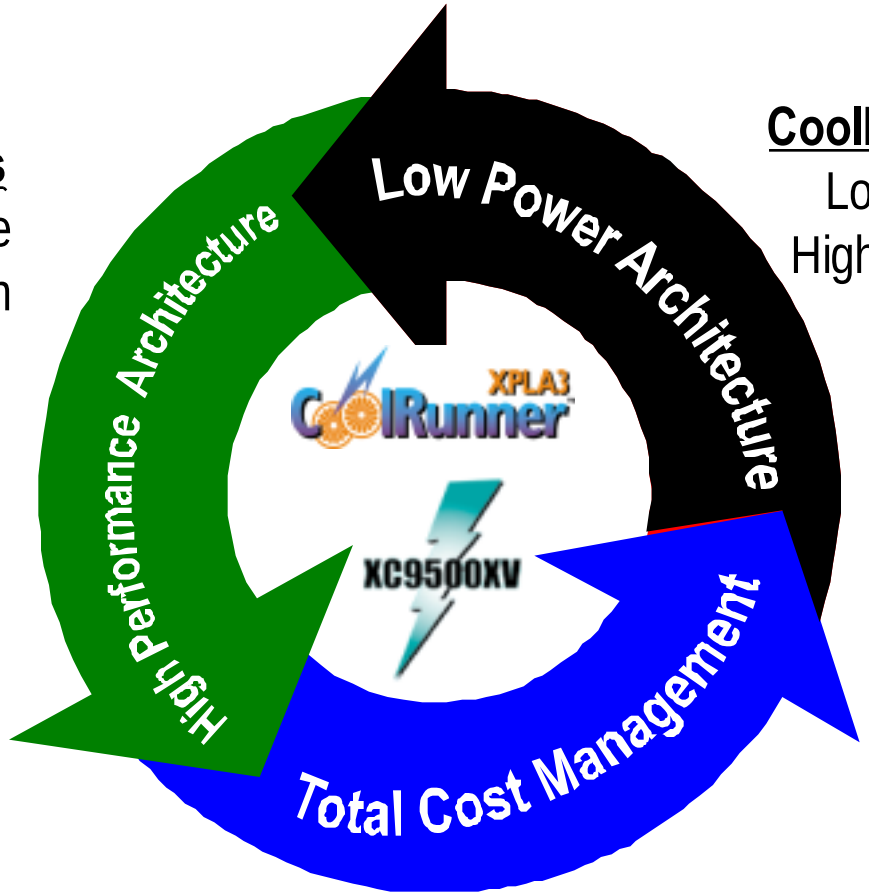


Spartan-II - System Integration



Xilinx CPLDs

XL9500 Families
High Performance
Low Cost Solution



CoolRunner Family
Lowest Power
Highest Reliability

System Integration and Peripheral Interfaces

CPLD Solutions For Every Need

- XC9500 families
- Voltage flexibility
  - 9500 - 5v / 9500XL - 3.3v / 9500XV - 2.5v
- 36-288 macrocell densities
- Ultra-high performance
- Low cost
- Superior pin-locking

- CoolRunner XPLA3 family
- Ultra-low power with high speed
- 3.3V
- 32-512 macrocell densities
- Advanced architecture

Intellectual Property and Software Solutions

World class tools and development environment

Ever expanding IP library and solutions provider community

Exploiting programmability to maximum advantage

Categories of IP

IP Center Smart Search Results (*197 out of 200 IP matches found*)

Building Blocks	Try	Buy	Type	FPGA Family					Related Search
				4K		II		II	
JPEG CODEC *Provider – Xentec_Inc.*	TRY		Alliance CORE				◆		Related Search
YUV2RGB Color Space Converter Core *Provider – Xilinx_Inc.*	TRY	BUY	logiCORE			◆	◆		Related Search
RGB2YUV Color Space Converter Core *Provider – Xilinx_Inc.*	TRY	BUY	logiCORE			◆	◆		Related Search
YCrCb2RGB Color Space Converter Core *Provider – Xilinx_Inc.*	TRY	BUY	logiCORE	◆	◆	◆	◆		Related Search
RGB2YCrCb Color Space Converter Core *Provider – Xilinx_Inc.*	TRY	BUY	logiCORE	◆	◆	◆	◆		Related Search

LogiCORE – IP developed, tested, sold, and supported by Xilinx

AllianceCORE – IP sold and supported by AllianceCORE partners

Reference DESIGN – Implementation examples available “as is”

Additional IP – Non-productized IP from additional sources

XPERTS Program

- Ready access to certified, local design resources for:
  - Optimal Xilinx solution expertise
  - Risk reduction with Xilinx supported consultants
    - Xilinx provides technical & business support to partners
  - Optimal IP core development, customization, integration & vertical market systems design services
    - DSP, communications, networking, video imaging experts
  - Xtreme DSP support
  - Xilinx PCI (LogiCORE) specialty
    - Increased performance, customization & re-targeting services
- Complete solution includes:
  - Devices + software + cores + certified design services
- 100 member companies worldwide, and growing!

Xilinx WebPOWERED Solutions

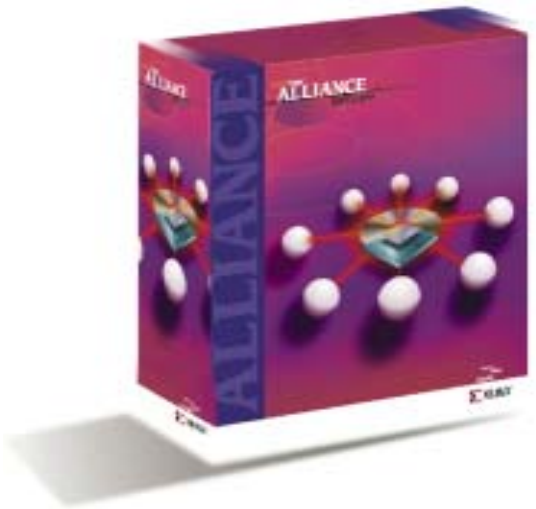
- **WebPOWERED** products are an industry first
  - First online design system
  - First complete downloadable EDA solution
- **WebPOWERED** products deliver ultimate flexibility
  - WebFITTER: Online device evaluation and design system
  - WebPACK: Modular and downloadable design suite
- FREE!
- Supports Spartan FPGA and all CPLD families of products

http://www.xilinx.com/sxpresso/webfitter.htm

http://www.xilinx.com/sxpresso/webpack.htm

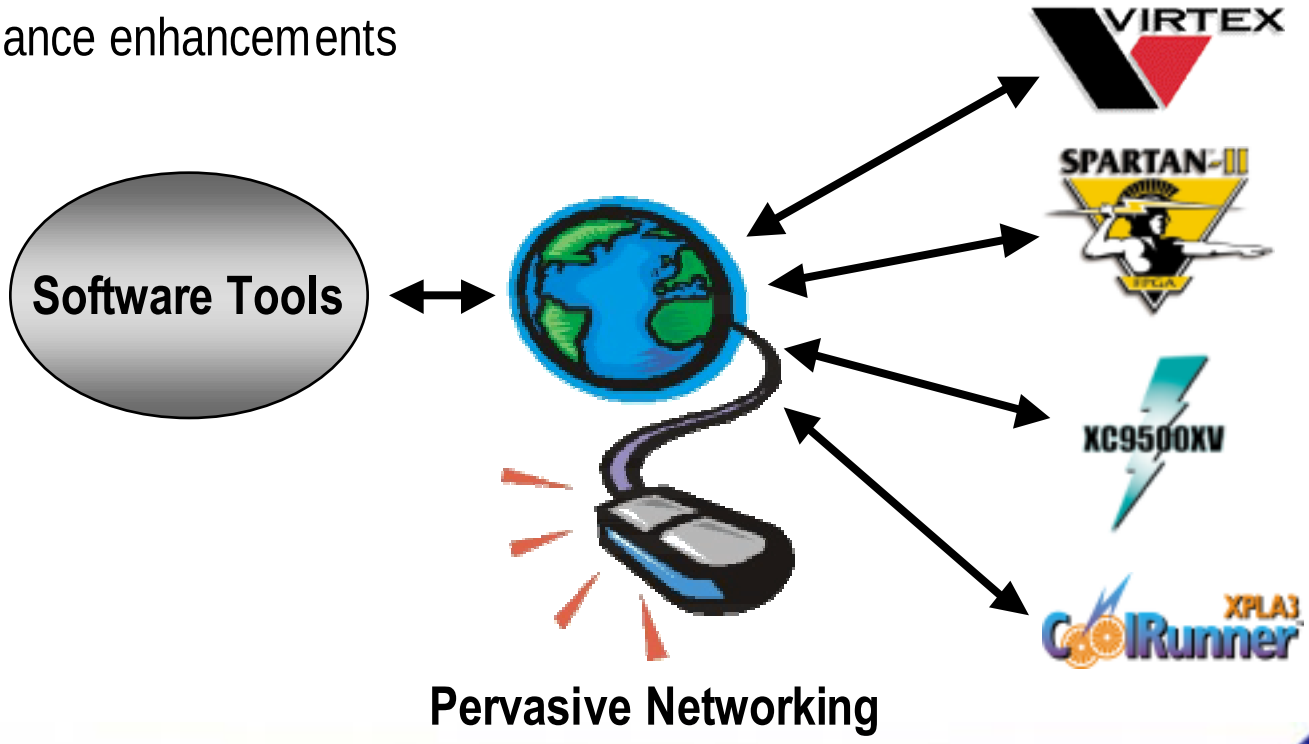
Alliance and Foundation Series Solutions

- Alliance Series — Integrates with leading third-party software
- Mentor, Cadence, Synopsys, Viewlogic, Exemplar . . .
- High density, high performance designs
- Foundation Series — Schematic centric tool chain
- Easy to use push button design flows
- Powerful auto-interactive capabilities
- Foundation ISE — HDL centric tool chain
- Integrated Synthesis Environment
  - VHDL and Verilog
  - Synopsis FPGA Express or Xilinx XSTsynthesis
  - Works with Model Technologies simulation tools
    - ModelSIM, MXE



Internet Reconfigurable Logic

- Configuration upgrades after deployment
  - Bug fixes
  - Compatibility updates
  - Performance enhancements



Why Xilinx?

- The industry's leading PLD product line
  - Virtex - The largest, fastest, FPGAs in the world
  - Spartan - The best value, high volume FPGAs in the world
  - XC9500 and CoolRunner - The lowest cost and lowest power CPLDs in the world
- Intellectual Property
  - LogiCOREs & AllianceCOREs -- optimized and supported
  - XPERTS design services community
- Software
  - WebFITTER and WebPACK online tools
  - Alliance Series: HDL, synthesis, EDA integration, optimization
  - Foundation Series: complete, ready to use solutions
  - Internet Reconfigurable Logic (IRL)

Xilinx eSP

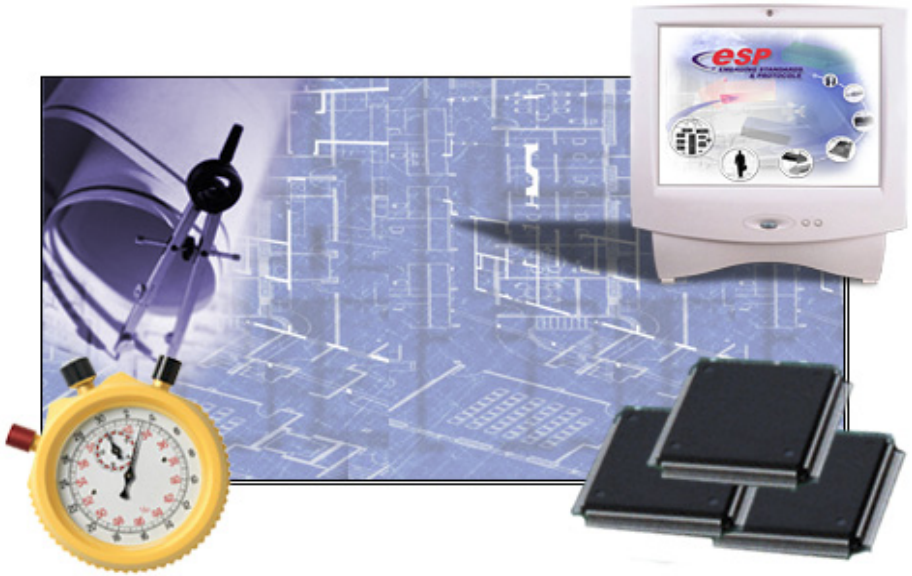
eSP Initiative

Industry's first initiative specifically dedicated to accelerating time-to-market of consumer products based upon emerging standards & protocols

www.xilinx.com/esp

Accelerating Time-to-Market Redefining the Product Development Model

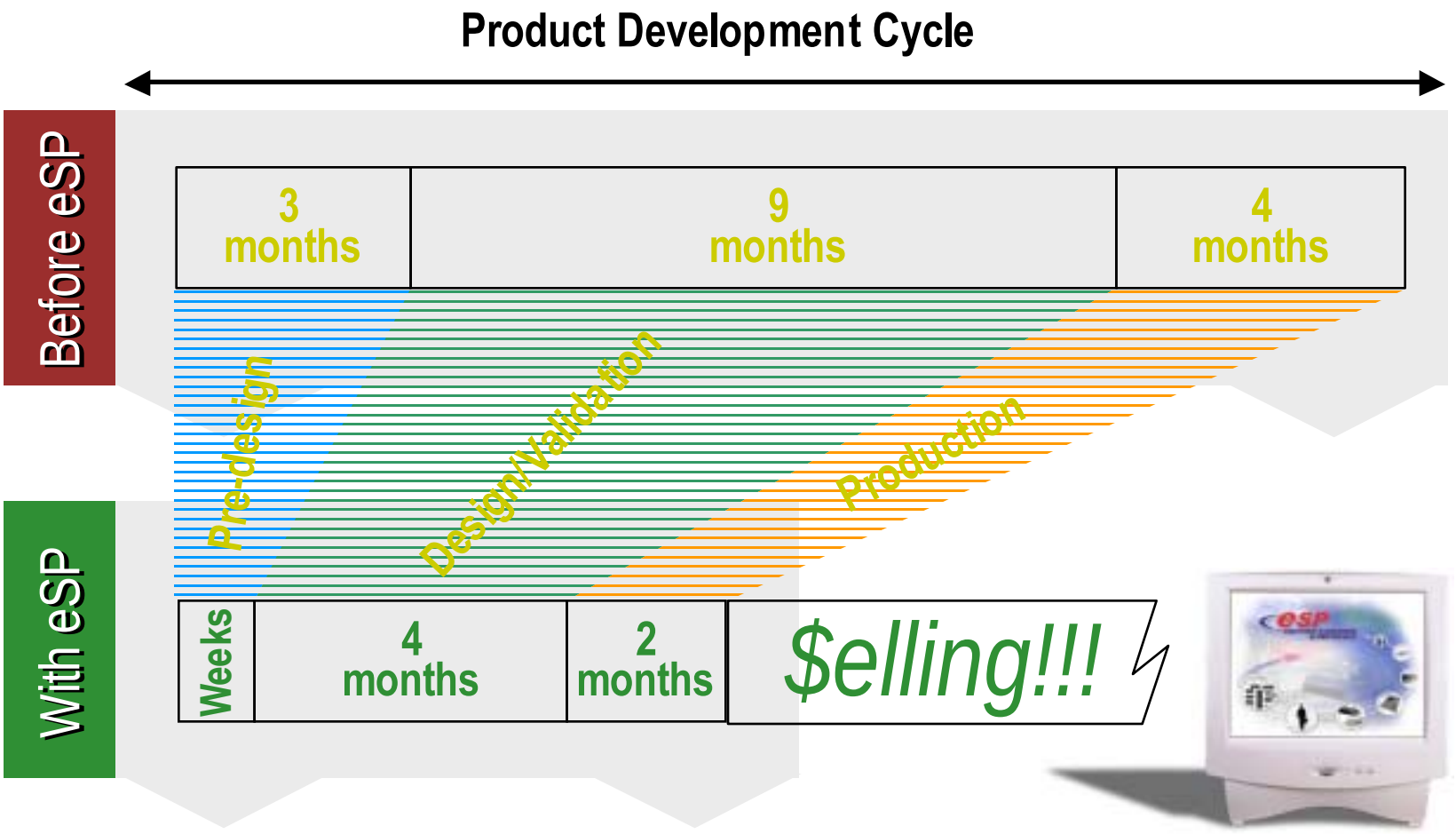
- Increasing design complexity
- Shrinking product life cycles
- Decreasing design & development time



Are driving the need for a new development model

- Pre-design has become the Achilles heel
- Increasing rather than decreasing
- Accelerating pre-design through production is today's challenge

Xilinx eSP is the Answer
Pre-Design Through Production Development



Xilinx eSP WEB Portal

Tutorials/White Papers
Technology and Market Overviews
- How they work
- Where they're headed
- Design challenges
- Where Xilinx can add value

Standards
- Specifications and updates
- Special interest groups
- Consortia

Glossaries

Technology Summits
Xilinx sponsored industry forums
International Seminars

Strategic Alliances & Reference Designs
Application Specific Solutions
- Working designs from respected industry players

Intellectual Property
LogiCORE
AllianceCORE

System Block Diagrams

FAQs

Industry Links

Consultant Directories