ECE 1352F
Analog Integrated Circuits I

Reading Assignment -

RF Power Amplifiers

Prepared by: Poon, Alan Siu Kei

Table of Content

I. Introduction

The rapid growth of mobile telecommunications services created increasing demand for low-cost, low-power and reduced size and weight equipments. An increasingly higher level of integration is needed to meet these requirements. Thanks to the advancement in deep sub-micron CMOS technology, this is easily achievable for digital signal and low-frequency signal processing. However, in order to reach the final goal of System-on-a-Chip (SoC) solution, the final piece of puzzle is still missing – the RF front end. In fact, being the most power hungry component of the RF front end, it is widely known that the RF power amplifier (PA) is one of the most critical building blocks in low power SoC integration. Therefore, it is clear that RF PA deserves increased design research to remove the bottleneck of the development of mobile communication devices. Among different classes of PAs, the Class-F topology has been drawing more attention by researchers in the last decade. In this paper, the recent development of Class-F PAs for portable devices will be discussed. In section II, an introduction to Class-F PA operation will be presented. Also, previously developed state of the art Class-F PA systems will be discussed in this section. In section III, current development of Class-F PA will be presented. The future focus and challenges to the development of Class-F PA will be revealed in section IV followed by a conclusion in section V.

II. Background

IIa. Why Class-F power amplifier?

Traditionally, PAs are categorized into different classes according to their historical precedence. Different PA classes can be divided into two major groups: linear and non-linear PAs. Class A, AB, B and C PA are some of the well-known linear PAs, which are distinguished primarily by their bias condition. Linear PAs have the advantage of high linearity that is important for variable envelope modulation schemes (e.g. π/4-QPSK). However, linear amplifiers suffer from poor maximum power efficiency which limits their applications in low-power devices. In practice, an efficiency of only below 20% can be achieved in those systems. In contrast, non-linear PAs (also known as switched mode PAs) can achieve better efficiency. As suggested by its name, non-linear PAs have poor linearity performance. Nevertheless, it is still acceptable for constant envelope modulation schemes (e.g. FSK). To overcome the problem of linearity to adapt to variable envelope systems, many linearization techniques have been proposed for non-linear amplifiers [1,2]. Therefore, due their high efficiency and the development of linearization techniques, non-linear PAs have received more attention over linear topologies in mobile communication in the last decade. Class E and F are the most common classes of non-linear PAs. In comparison, Class E PA requires fast switching driver signal that is not required for Class-F PA. Moreover, because of relatively large switch stresses to active devices, Class E amplifiers do not scale gracefully with the trend toward lower-power technology with lower breakdown voltage [1:Thomas Lee]. For these reasons,

Class-F PA has drawn more attention for its easier implementation and better integration with sub-micron CMOS technology.

IIb. Class-F power amplifier operation

A Class-F PA uses a output filter to control the harmonic content of its drain-voltage or drain-current waveforms, thereby shaping them to reduce power dissipation by the transistor and thus to increase efficiency. An example of the output voltage and current waveform of an ideal Class-F PA is shown in Fig. 1 [3].

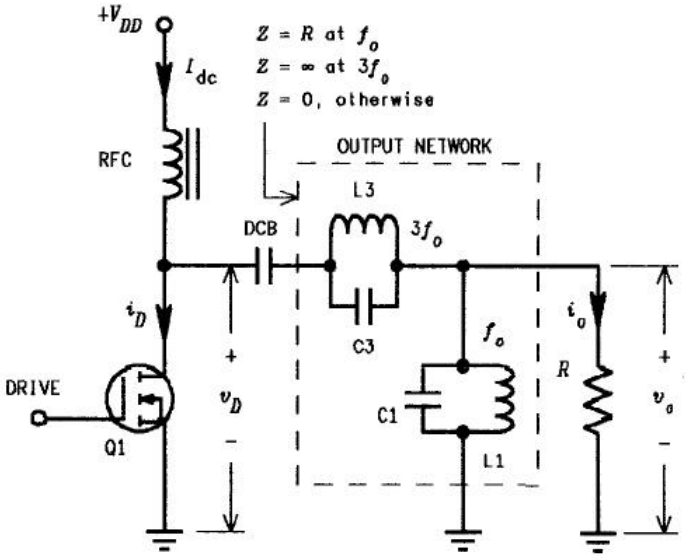

Fig. 1. Example of a Class-F power amplifier.

In the figure, it is noticed that the output voltage waveform is a square wave while the drain current is a half-rectified sinusoid. From the output waveforms it is also noticed that in the ideal case, there is no overlapping between the output voltage

and current waveform. This suggests that the maximum achievable power efficiency of the PA is 100%, since there is no power loss in the output waveform [4]. To accomplish this behavior, the active device has a bias point at the cutoff region for switching operation. Also, from Fourier analysis, it is known that the voltage square waveform only has the fundamental and odd harmonics, while the half-rectified current waveform only has the fundamental and even harmonics [4]. Therefore, the load must present an open or short at odd or even harmonics, respectively. A classical Class-F PA demonstrating these characteristics is shown in Fig. 2 [3], in which the output network consists of a quarter-wavelength transmission line and a parallel-tuned LC output tank. The output tank is tuned to resonance at the fundamental frequency (i.e. the carrier frequency).

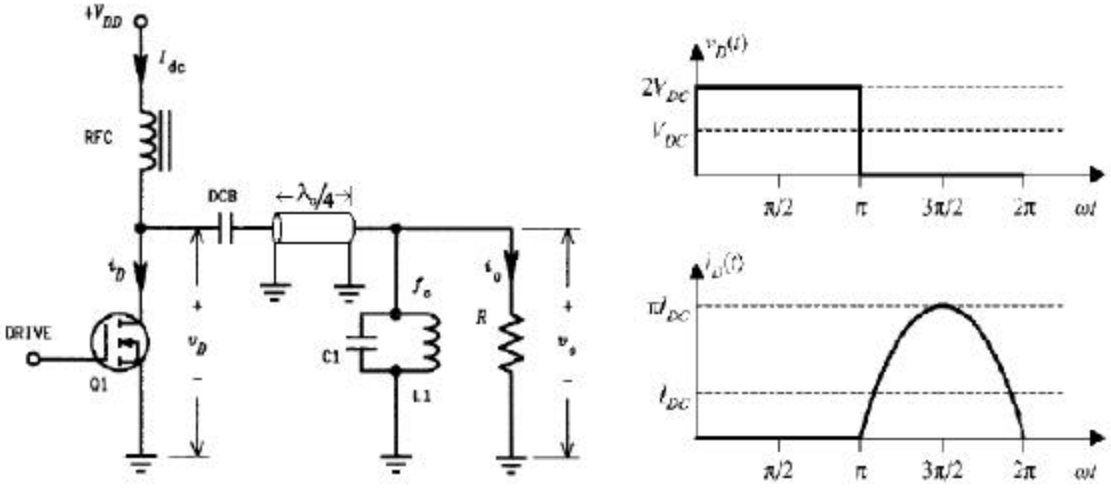

Fig. 2. A Class-F power amplifier with quarter-wavelength transmission line and parallel-tuned output.

Recall that for a quarter-wavelength transmission line, the input impedance is

$$Z_{in} = \frac{Z_o^2}{Z_L} \quad \text{.....(1)}$$

The impedance seen by the drain can be easily found from this simple equation. At fundamental frequency, the drain sees a pure resistive load of $R_L=Z_L$, since the output tank is open circuit. The tank is a short at all frequencies away from the fundamental. At even harmonics, the transmission line appears to be a half-wavelength line to the drain. We know that for half-wavelength line, the input impedance is $Z_{in}=Z_L$. Therefore, the drain sees a short at all even harmonics, which would result in a half-rectified sinusoid current output as desired. Conversely, at odd harmonics, since the output tank still appears as a short, according to equation (1) the drain sees an open circuit. That is,

$$Z_{in} = \frac{Z_o^2}{Short} = Open\ .$$

If the transistor is assumed to act as a switch, the output network will guarantee that all of the drain voltage will see an open and hence a square wave would be resulted as desired [4]. Therefore, the ideal Class-F output waveform can be achieved by this simple circuit. Note that the same ideal maximum efficiency of 100% can also be achieved by producing a square wave current and half-rectified sinusoid voltage at the output [3]. An example of such implementation using a quarter-wavelength transmission line with series-tuned tank is shown in Fig. 3 [3].

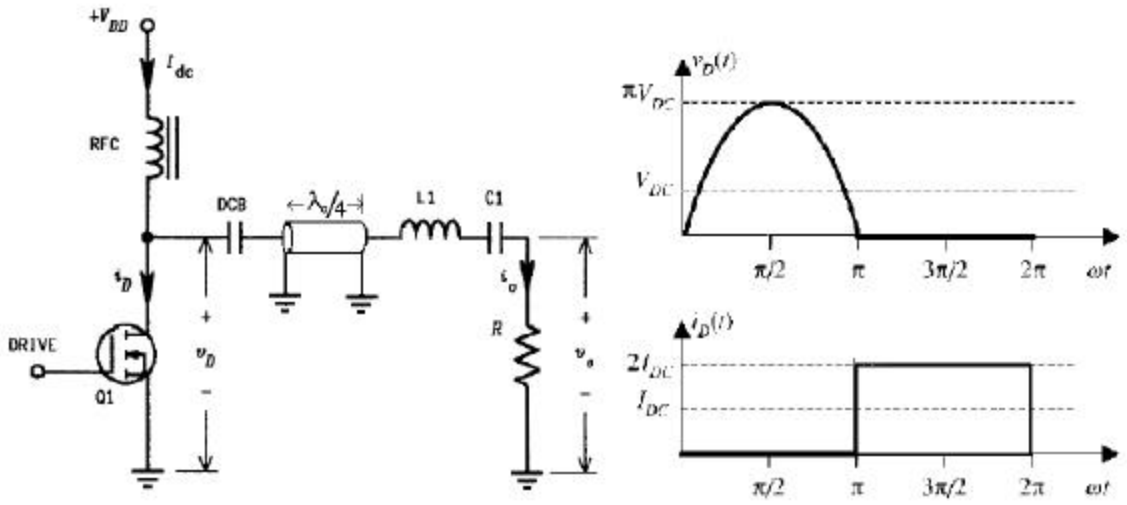

Fig. 3. A Class-F power amplifier with quarter-wavelength transmission line and series-tuned output.

IIc. Previous development of Class-F power amplifier

Due to its simple operation principles, little researches have been done on revolving the actual architecture of Class-F PA. What the researchers and developers have been doing is simply reproduce and adapt the Class-F PA architecture in difference fabrication processes and technology and try to improve the efficiency by fine tuning the loading network. In this section, several state of the art Class-F PAs implemented in CMOS technology that are previously developed will be discussed.

Although the topology discussed in last section is elegant, the transmission line may be inconveniently long or even inapplicable in fully on-chip integration. Furthermore, the ideal case of infinite impedance at odd harmonics other than the fundamental are undermined in practice by the output capacitance of the

transistor [4]. Therefore, Class-F PAs are usually implemented using finite number of parallel resonant filters connected in series in the loading network to approximate the effect of transmission line. A plot of phase angle vs. relative voltage level is shown in Fig. 4 [5] that demonstrates how the output voltage of a third order network approximates an ideal square wave. An example of such

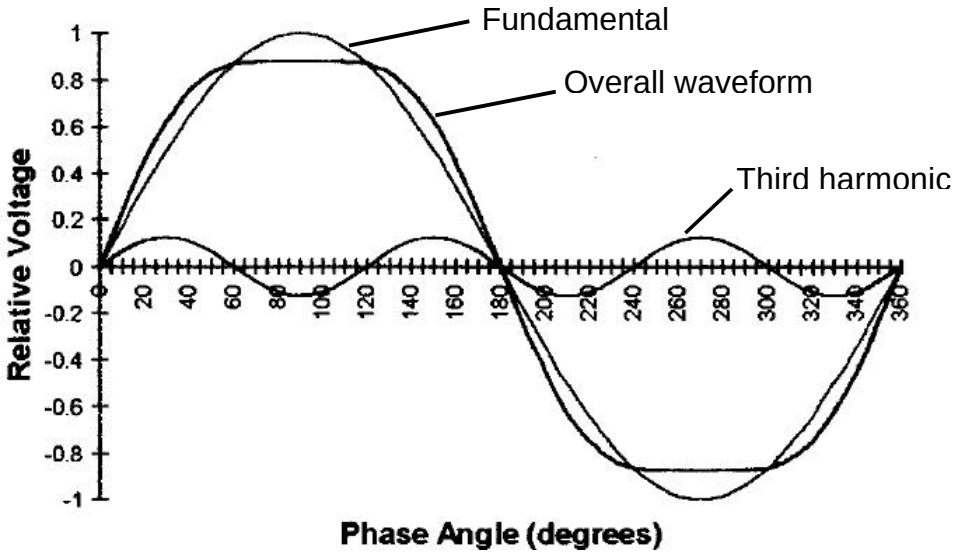

Fig. 4. Phase angle vs. relative voltage of an ideal third order network.

configuration is shown in Fig. 5 [3]. In Fig. 5, the loading network only consists of parallel resonant filters tuned to the fundamental and third harmonic components. This configuration is called *third harmonic peaking* [5]. The output voltage and current waveform is also shown in the figure. It is obvious that there is little overlap between the output voltage and current waveform, which causes power dissipation. Theoretically, an ideal third harmonic peaking network can achieve maximum efficiency of more than 80% [3]. Thus, it is shown that the use of

loading network tuned to finite number of harmonics can eliminate the use of transmission line while obtaining respectable efficiency.

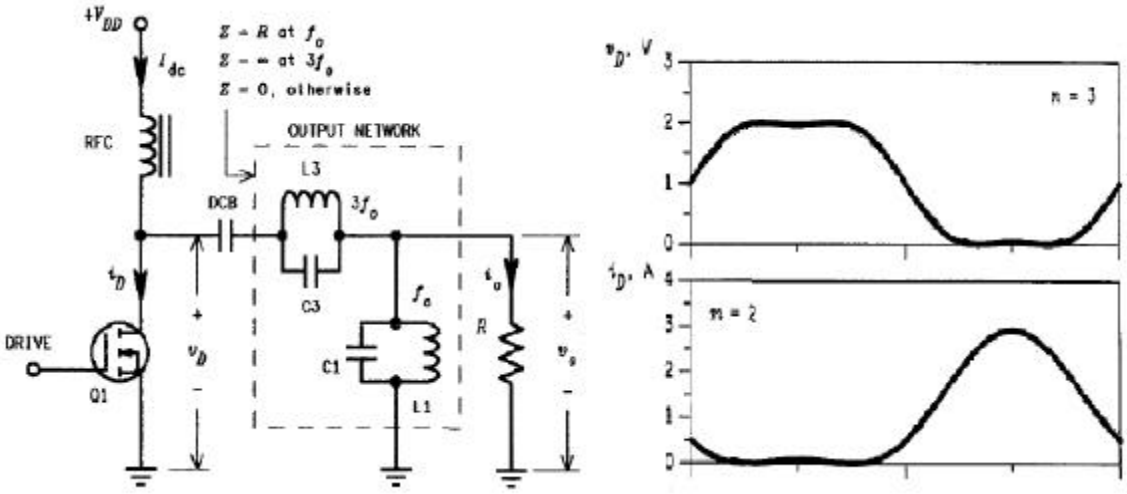

Fig. 5. Example of a third harmonic peaking Class-F power amplifier.

A fully on-chip third harmonic peak Class-F amplifier was implemented in 0.8μm CMOS technology with 3V supply in [6]. The schematic of the circuit is shown in Fig 6. The circuit consists of two stages. The first stage is designed to have maximum gain and the second stage is matched to have maximum efficiency. All of the matching and tuning networks of the PA are accomplished on chip with MOS capacitor and spiral inductors. The implemented PA can only achieve a output power of 20dBm with an efficiency of 16%. The poor efficiency is mainly due to the lossy on-chip spiral inductors of the 0.8μm CMOS technology. From the performance of the design, we can see that there are still lots of space for improvement on power efficiency when design fully on-chip CMOS PA.

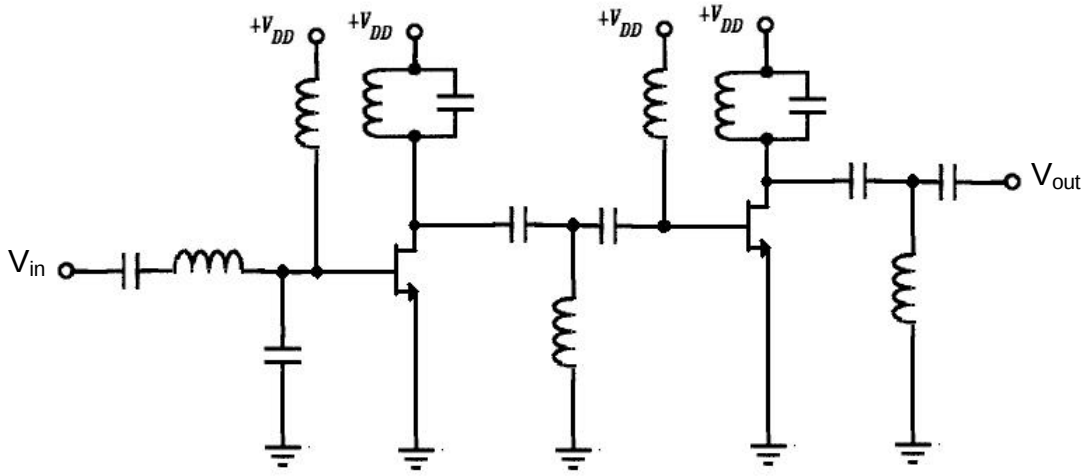

Fig. 6. Schematic of a two-stage Class-F power amplifier.

III. Present development of Class-F power amplifier

The growing demand of low-power mobile communication devices speed up the development of Class-F PA. Recently, both theoretical and practical advancements have been made in this hot area of research. In the first part of this section, new theoretical development on the subject will be presented. Then in the second part, some practical improvements on the implementation of Class-F PA in CMOS technology that has been achieved by researchers will be discussed.

IIIa. Theoretical improvement

Although the Class-F topology has became a popular technique for improving the efficiency of RF PA, the impact of using different numbers of harmonics remains only partially understood. As a consequence, some researches have been conducting researches to investigate the upper limits of output power and

efficiency as functions of the number of harmonics used in PA [3, 7, 8, 9]. This allows the designer to make reasonable tradeoff between output network complexity and efficiency since both size and power consumption is important factor when designing mobile communication devices.

The best approximation of a square waveform or half-rectified sinusoid out a finite number of harmonics is called the maximally flat waveform [8]. In order to obtain a maximally flat waveform, appropriate coefficients (or relative magnitude) of different harmonic components must be determined. To determine these coefficient values, the drain voltage and current waveforms are expressed as summation of their harmonics:

$$v_D(q) = V_{DD} + V_{0m}\sin q + V_{3m}\sin(3q) + V_{5m}\sin(5q) + \ldots$$

and

$$i_D(q) = I_{DD} - I_{0m}\sin q + I_{23m}\cos(2q) - I_{4m}\cos(4q) + \ldots$$

where $q = \omega t$ and ω is the fundamental frequency of the desired output signal. The coefficients of fundamental component can be related to dc component by basic waveform parameters γ_V, γ_I, δ_V and δ_I as:

$$\begin{aligned} V_{0m} &= g_V V_{DD} \\ v_{Dmzx} &= d_V V_{DD} \\ I_{0m} &= g_I I_{dc} \\ i_{Dmzx} &= d_{IV} I_{dc} \end{aligned} \quad \ldots\ldots\ldots (4)$$

Having the voltage and current output described by the above expressions, it is possible to determine the harmonic coefficients of a maximally flat waveform by adjusting their values so that the derivatives of the waveform are zero at the

maximum and/or minimum voltage or current. Note that the highest order of derivatives depends on the highest order of harmonics. Since it is known that the voltage waveform reaches its maximum and minimum values at $\theta = \pi/2$ and $3\pi/2$, we can substitute these angles into the derivatives and solve for the basic waveform parameters for the odd harmonic voltage wave. Similarly, the current waveform parameters can be obtained by knowing it reaches its maximum and minimum values at $\theta = 3\pi/2$ and $\pi/2$. The resulting harmonic coefficients calculated in [7] for odd and even harmonics are summarized in Table 1 and Table 2.

Harmonics	δ_V	$\gamma_V = V_{0m} / V_{DD}$	V_{3m} / V_{0m}	V_{5m} / V_{0m}
1	2	1	~~	~~
3	2	1.1547	0.1667	~~
5	2	1.0515	~~	-0.0618
3+5	2	1.2071	0.2323	0.0607
∞	2	$4 / \pi = 1.273$	$4 / 3\pi = 0.424$	$4 / 5\pi = 0.255$

Table 1. Maximally flat voltage waveform coefficients for ODD harmonics.

Harmonics	δ_I	$\gamma_I = I_{0m} / I_{dc}$	I_{2m} / I_{0m}	I_{4m} / I_{0m}
1	2	1	~~	~~
2	2.9142	1.4142	0.3540	~~
4	2.1863	1.0824	~~	-0.0957
2+4	3	1.5	0.3890	0.0556
∞	$\pi = 3.142$	$\pi / 2 = 1.571$	$2 / 3 = 0.667$	$2 / 15 = 0.133$

Table 2. Maximally flat current waveform coefficients for EVEN harmonics.

After determining the harmonic coefficients for maximally flat waveform, we are ready to calculate the maximum output power and efficiency of maximally flat waveforms with different number of harmonics. The output power is

$$P_O = \frac{V_{0m}^2}{2R} = \frac{g_V^2 V_{DD}^2}{2R} \quad \text{…….(5)}$$

where R is the impedance seen by the drain at the fundamental frequency. The DC-input power is

$$P_i = V_{DD} I_{dc} = V_{DD}\left(\frac{I_{0m}}{g_I}\right) = V_{DD}\left(\frac{V_{0m}}{R g_I}\right) = \frac{g_V V_{DD}^2}{g_I R}. \text{ ……..(6)}$$

Finally, the efficiency of the amplifier is

$$h = \frac{P_O}{P_i} = \frac{g_V g_I}{2} \quad \text{…….(7)}$$

and the maximum output power is

$$P_{\max} = \frac{P_{out}}{v_{D\max} i_{D\max}} = \frac{g_V g_I}{2 d_V d_I} = \frac{h}{d_V d_I}. \text{ …….(8)}$$

By substituting the harmonic coefficients in Table 1 and 2 into equation (7) and (8), we can calculate the maximum efficiency and output power of Class-F PA with different number of harmonics. The results obtained in [7] are summarized in Table 3. The same set of results is also plotted in bar chart as shown in Fig. 7.

Max. current harmonic, m	Efficiency, η			
	Max. voltage harmonic, n=1	Max. voltage harmonic, n=3	Max. voltage harmonic, n=5	Max. voltage harmonic, n=∞
1	0.5	0.5774	0.6033	0.6370
2	0.7071	0.8165	0.8532	0.9003
4	0.7497	0.8656	0.9045	0.9545
∞	π / 4 = 0.785	0.9069	0.9477	1
	Maximum output power, P_O			
	0.125	0.1443	0.1508	0.159

Table 3. Maximum efficiency and power output of Class-F power amplifiers with different number of harmonics.

From Fig. 7, Class-F PA designers can easily make the appropriate tradeoff between the complexity and efficiency of the amplifier. This is very useful to designers since both size and power consumption of the PA are important factors when designing modern mobile communication devices. In summary, the result of this research is very helpful for designers to have more in-depth understanding of the characteristics of Class-F PA with finite number of harmonics.

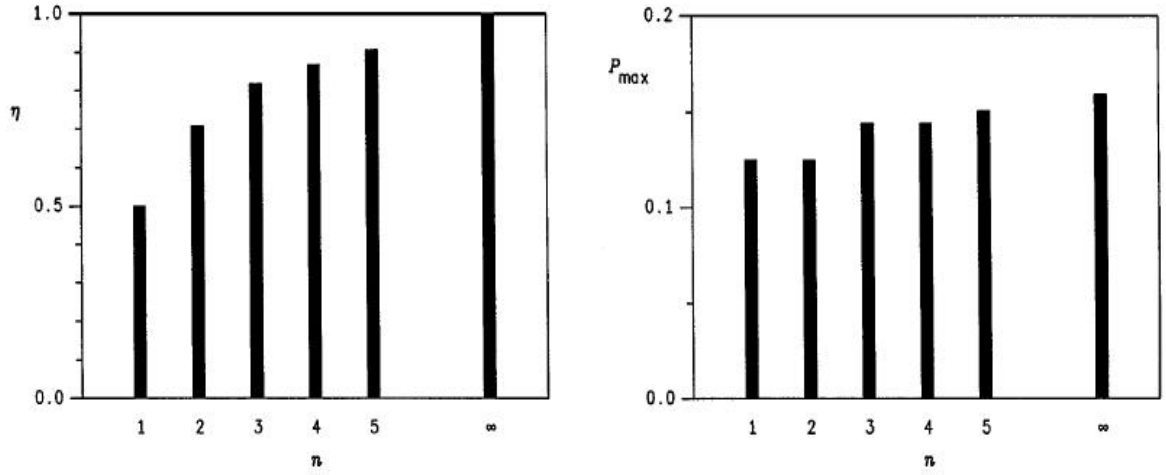

Fig. 7. Efficiency and maximum output power of maximally flat waveform with different number of harmonics (n).

IIIb. Practical improvement

Other than the theoretical improvement that has been made in the development of Class-F PA as presented in the previous part, many researchers have been concentrating on the actual implementation of Class-F PAs in deep sub-micron CMOS technology. In this section, an innovative improvement in implementing a high efficiency Class-F PA in deep sub-micron CMOS technology achieved by a researcher in [10] will be presented.

In the RF domain, it is not easy to raise the efficiency of PA by even a few percents, especially implement in CMOS technology. One of the major challenges of implementing Class-F PAs in CMOS is its low oxide breakdown voltage. The problem of low oxide breakdown voltage limits the supply voltage to the amplifier, which directly limits the maximum output power and efficiency of the amplifier. To overcome this problem, a new configuration for Class-F PA was proposed in [10] and the schematic of the circuit is shown in Fig. 8.

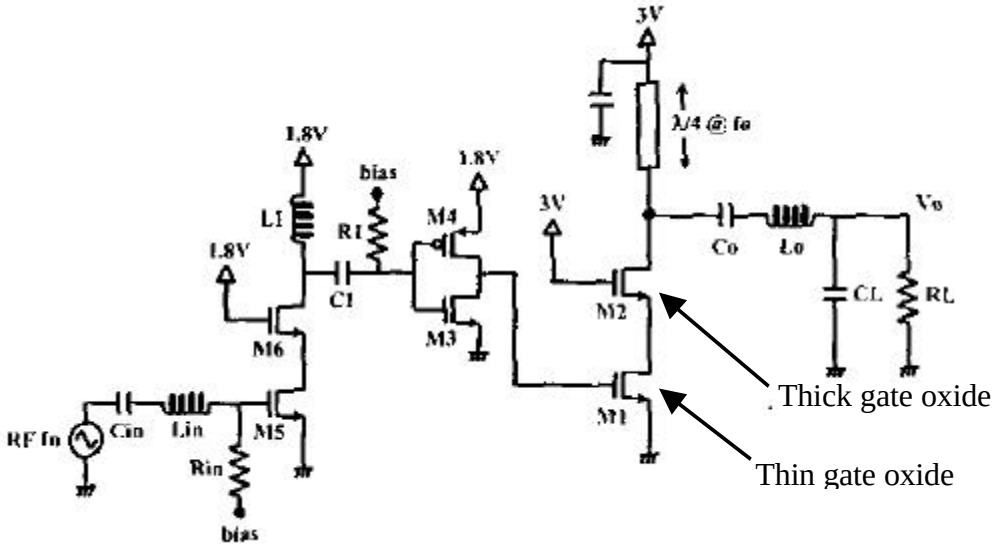

Fig. 8. Schematic of a two-stage Class-F power amplifier.

Different from to conventional Class-F PA, this new configuration places a thick oxide (80Å) transistor M2 in cascode to the conventional transistor M1. The gate of M2 is biased at 3V, which allows the output node to sustain 7V without damaging the transistor. The thin gate transistor M1 is now protected by M2 with no threat to oxide breakdown. Since dual gate oxide transistors are widely available in deep sub-micron CMOS technologies, it is not considered a special

process requirement. However, note that the higher supply voltage is gained at that cost of lower efficiency because M2 acts as a resistor in series with the output. Also, the cascode transistor M2 reduces the output voltage swing of the PA which is not desirable.

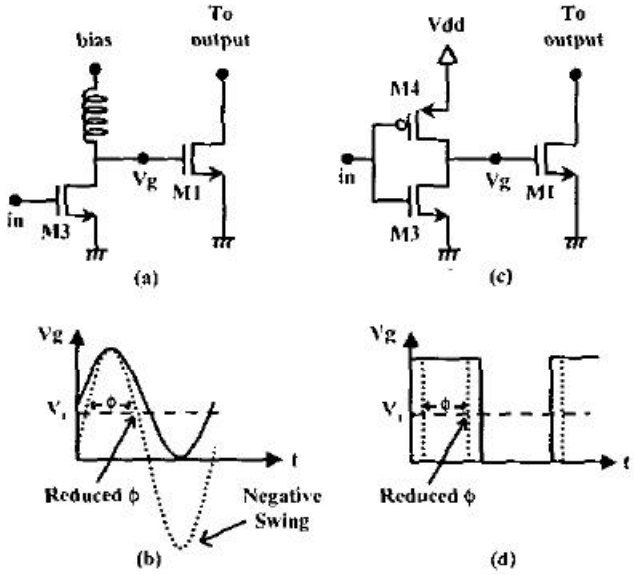

Fig. 9. (a) Induction-tuned load PA driver; (b) Reduced angle (ϕ) V_g waveform; (c) CMOS inverter driver; (d) V_g waveform of CMOS inverter driver.

Another special feature of the new configuration in Fig. 8 is the use of a CMOS inverter as the pre-driver as compared to convention inductor tuned pre-driver as shown in Fig. 9 [10]. In conventional PAs, problem exists when operating with reduced conduction angles for higher efficiency. Under this condition, the input sine wave amplitude must be increased for maximum output current in conventional Class-F PAs using inductor tuned pre-drivers. This results in negative voltage swing that is not an issue for GaAs MESFET, but a major problem for CMOS. The negative voltage swing can potentially forward bias the drain junction diode. More importantly, since the output voltage peaks at the

most negative input, this circuit will increase the peak voltage across the gate oxide of M1 and worsen the already severe problem of low oxide breakdown voltage. Thus, the researchers proposed to use a CMOS inverter pre-driver to solve this problem so that it always have non-negative voltage swing. In addition, using a square wave driver can improve the efficiency of PAs, because square wave input can switch the transistor between cut-off and saturation regions more quickly than a sine wave input. The drawback of using a CMOS inverter driver is reduction in linearity, which is not a problem for constant envelope modulation schemes.

By employing the features discussed in the last two paragraphs, the new Class-F PA configuration demonstrates respectable performance when it was implemented in deep sub-micron CMOS technology. In [10], the circuit was successfully implemented on-chip in a 0.2μm CMOS technology with a dual supply voltage of 1.8V and 3V. Operating at 900MHz, the PA can deliver a maximum output power of 1.5W with an efficiency of 43%. This is a significant improvement in performance as compared to the previous fully on-chip PA described in section IIc. The result of this work shows that higher power is achievable with deep sub-micron CMOS technology despite the low oxide breakdown voltage.

IV. Future challenges and focus

By comparing the maximum efficiency of an ideal case (~80%-90%) to that of the so-called state of the art circuit discussed in this paper (~50%), obviously there is still a lot of space for improvement in deep sub-micron CMOS Class-F PAs. Undoubtedly, researchers will continue to try to improve the efficiency of CMOS Class-F PAs by fine tuning the load network and using higher quality passive and active elements. In addition, some recent research papers reveal the possibility of improving Class-F PAs efficiency by proper shaping of the input driving signal [11]. Other than that, the development of power control of PAs is becoming another popular research area. This is because while mobile communication devices dissipate higher power during active operation, much smaller power is needed during stand-by operation mode. Thus, good power control to of PAs can greatly reduce the overall efficiency and power consumption of devices. Furthermore, in order to achieve the goal of putting the entire mobile handsets circuits in a single chip, the integration of RF front end module with the low-frequency or baseband DSP module remains the one of the most challenging research area. For example, the substrate noise from the DSP module will greatly degrade the performance of the RF front end module.

V. Conclusion

In this paper, some recent developments of Class-F power amplifiers are presented, especially on their integration with deep sub-micron CMOS technology. However, these advancements are just a little step in the development of a compact, low cost and efficient power amplifier. Although the concept of Class-F topology has been proposed for several decades, its characteristics are still not fully understood and a systematic design procedure is still yet to be defined. In addition, many issues are still needed to be resolved before the goal of System-on-a-Chip can be realized. Nevertheless, the rapid growing demand of mobile communication devices will be a good catalyst for the development of RF power amplifiers and a real SoC solution will hit the market very soon in the future.

References

[1] Gary Hau, Takeshi B. Nishimura and Naotaka Iwata, “A high efficient linearized wide-band CDMA handset power amplifier based on predistortion under various bias conditions,” *IEEE Transaction on Microwave Theory and Techniques,* Vol. 49, No. 6, pp.1194-1201, June 2001.

[2] Steve Hung-Lung Tu and Chris Toumazou, “Low-distortion CMOS complementary Class E RF tuned power amplifiers,” *IEEE Trans. on Circuits and Systems-I: Fund. Theory and Applications,* Vol. 47, No. 5, pp. 774-779, May 2000.

[3] F. H. Raab, “An introduction to Class-F power amplifies,” *RF Design,* Vol. 19, No. 5, pp. 79-84, May 1996.

[4] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge, 1999.

[5] Chris Trask, “Class-F amplifier loading networks: a unified design approach,” *IEEE MTT-S Dig.,* Anaheim, CA, pp. 351-354, June 1999.

[6] Y. J. E. Chen, M. Hamai, H. Heo, A. Sutono, S. Yoo and J. Laskar, “RF power amplifier integration in CMOS technology,” *IEEE MTT-S Dig.,* pp. 545-548, 2000.

[7] F. H. Raab, “Maximum efficiency and output of Class-F power amplifiers,” *IEEE Trans. on Microwave Theory and Techniques,* Vol. 49, No. 6, pp. 1162-1166, June 2001.

[8] F. H. Raab, “Class-F power amplifiers with maximally flat waveforms,” *IEEE Trans. on Microwave Theory and Techniques,* Vol. 45, No. 11, pp.2007-2012, Nov. 1997.

[9] F. H. Raab, “Class-F power amplifiers with reduced conduction angles,” *IEEE Trans. on Broadcasting,* Vol. 44, No. 4, pp.455-459, Dec. 1998.

[10] Timothy C. Kuo and Bruce B. Lusignan, “A 1.5W Class-F RF power amplifier in 0.2μm CMOS technology,” *ISSCC, Session 10, Wireless Building Blocks-I,* pp. 154-155, Feb. 2001.

[11] A. N. Rudiakova and V. G. Krizhanovski, “Driving waveforms for Class-F power amplifiers, “ *IEEE MTT-S Dig.,* pp. 473-476, 2000.

[12] F. H. Raab, “Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics,” *IEEE Trans. on Microwave Theory and Techniques,* Vol. 49, No. 8, pp. 1462-1468, Aug. 2001.

[13] Gary Hau, Takeshi B. Nishimura, Naotaka Iwata, “High efficiency, wide dynamic range variable gain and power amplifier MMICs for wide-band CDMA handsets,” *IEEE Microwave and Wireless Components Letters*, Vol. 11, No. 1, pp. 13-15, Jan. 2001.