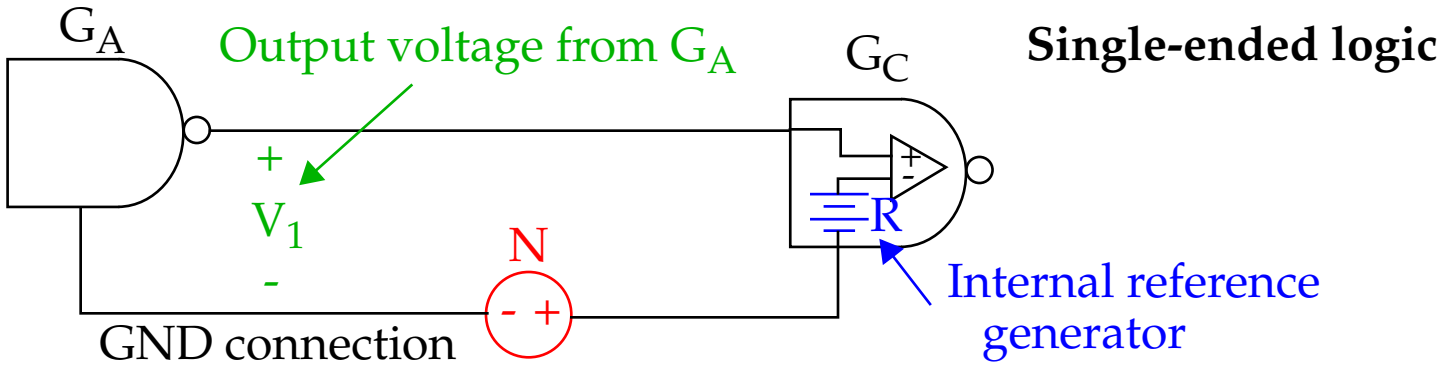
Power Systems

Serve to:

- Provide stable voltage references
- Distribute power to all logic devices

The voltage reference problem:



G_C must determine if G_A's signal is a 1 or 0 by comparing it with internal reference voltage R.

The reference voltage for CMOS is a *weighted average* of V_{CC} and V_{EE}, for TTL, its a fixed offset above V_{EE}, for ECL, it's a fixed offset below V_{CC}.

The Voltage Reference Problem

Assuming the reference is a fixed offset above GND, the voltage received at the input of the differential amplifier is:

Differential input = V_1 - N - R

Any noise voltage between the GND terminals of G_A and G_C adds to the incoming signal voltage and reduces the **noise margin** for G_C.

Noise N can be caused by the return current acting across the inductance of the GND wiring.

Common-path noise voltage (from other gates) can also cause this.

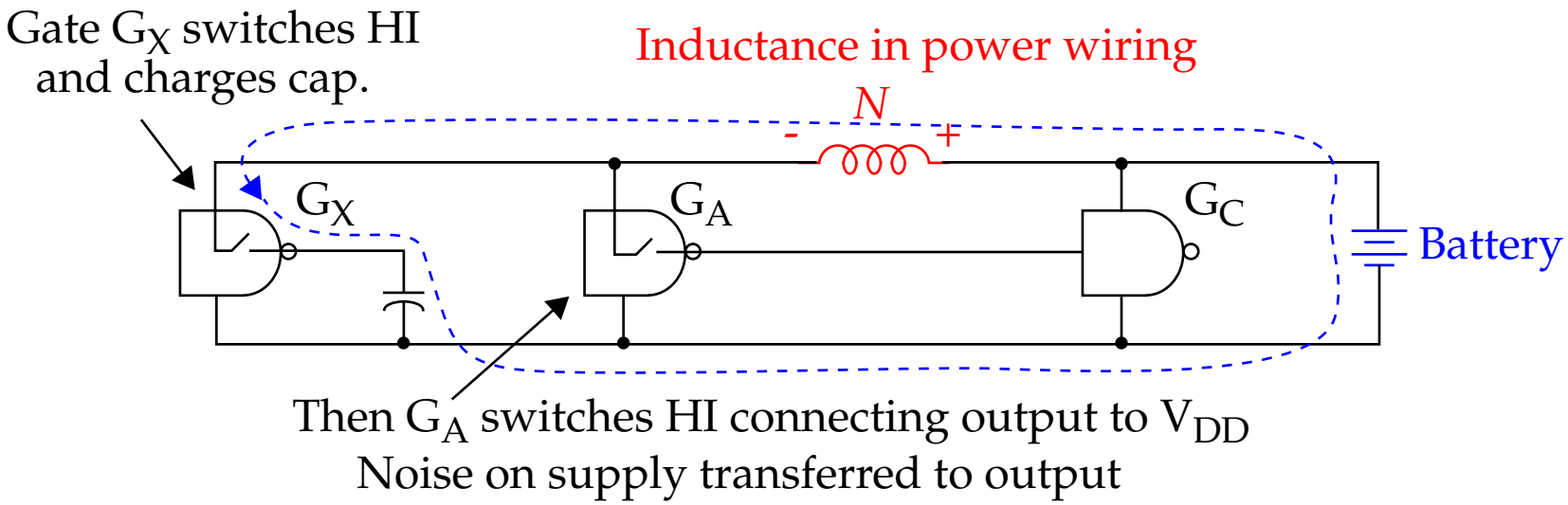
To ensure low *common-path noise*, the GND path must be low impedance between gates.

A GND plane serves this purpose very well.

Note that this refers to lumped inductance of a common wire -- we discussed *mutual inductive coupling* in nearby **separate** wires also as a source.

The Voltage Reference Problem

Low GND inductance alone does not solve the *common-path noise* problem



Impedance between power pins should be just as low as impedance between GND pins.

Also note that the impedance of the battery must also be very low to maintain stable transmitted signal levels.

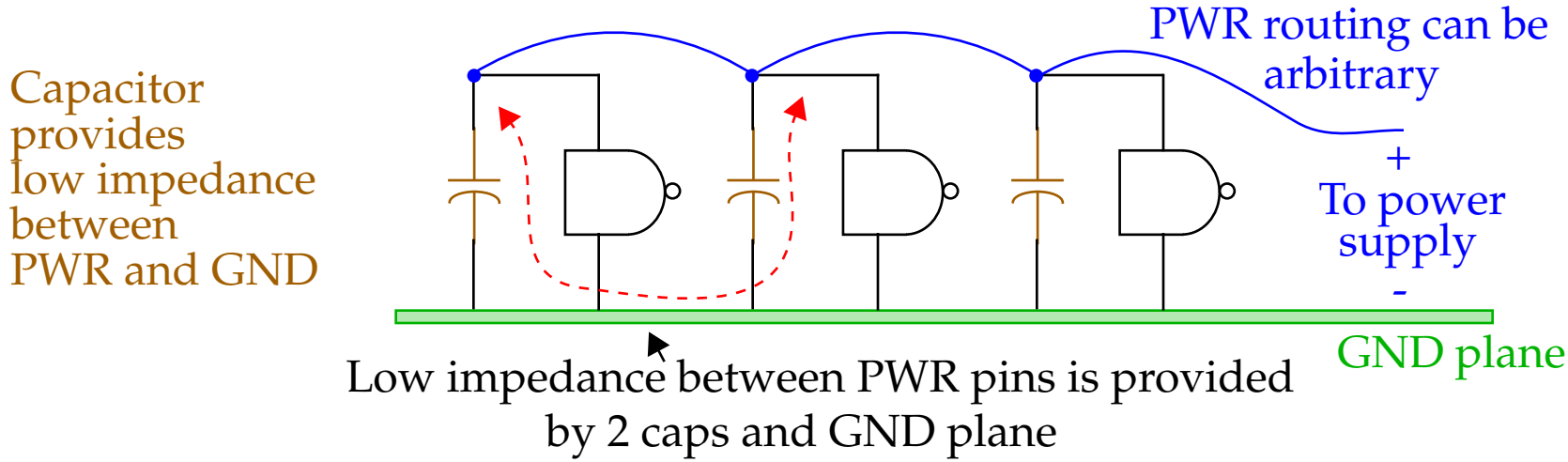
Here, the only path is through the battery -- in real systems, there are other paths, either way, **there MUST exist a low impedance path between PWR and GND**.

Power System Properties

Any system that satisfies these three power system design rules will:

- Provide a stable reference voltage
- Have a low common-path noise
- Maintain a uniform power distribution voltage everywhere

These are inseparable -- helping one property will generally help others.

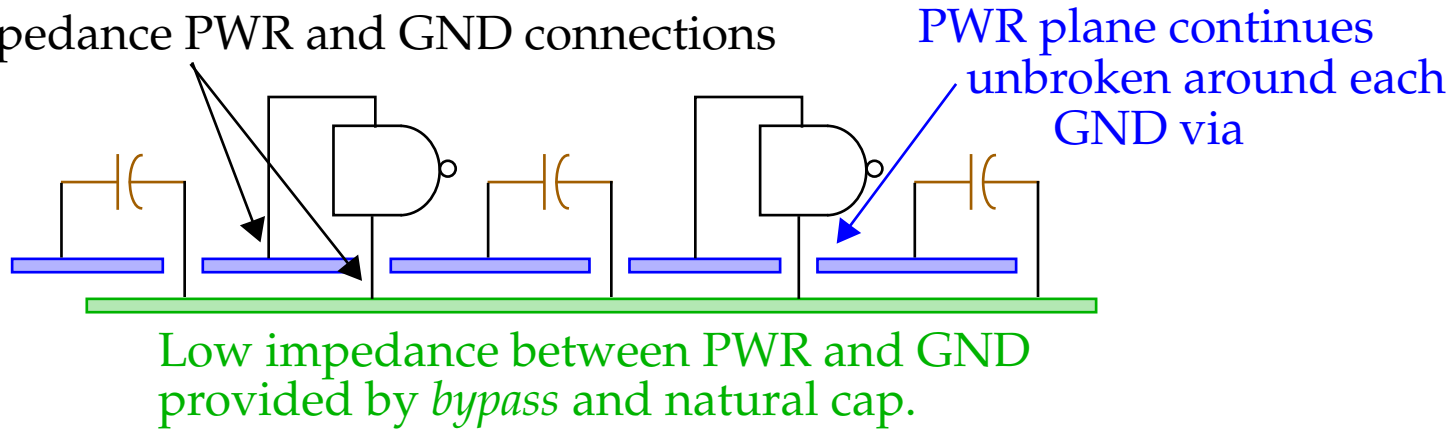


***By-pass* capacitors** provide the low impedance path between PWR and GND and also between PWR terminals through two series capacitors.

For single GND plane approach, the *bypass* caps must have low impedance.

Power System Properties

A better approach uses separate copper planes for PWR and GND:



PWR and GND planes allow high frequency currents to pass easily between planes.

The discrete capacitors provide *shorts* for lower frequency components.

The *differential transmission* configuration provides a signal return path for every signal wire.

Also, every signal carries its own reference voltage and the *receiver* does not connect to either power terminal, i.e., no reference needed.

Decouples problem of distributing power from providing a stable reference voltage.

Distributing Uniform Voltage

Power supplies generally have very low output impedances but the inductance of the *power distribution wiring* increases the high freq. impedance.

Designers typically install a large *bypass* capacitor between PWR and GND.

This capacitor is designed to reduce impedance at the point the wiring inductance becomes a problem.

Unfortunately, the *bypass* capacitor can only provide a low impedance path over a limited frequency range.

Lead inductance limits its effectiveness at high frequencies.

Designers also typically install an *array* of bypass capacitors on the card.

This array has a total capacitance less than the big bypass cap. but it has much better *series inductance.*

The combination of power distribution wiring, the big bypass capacitor and the array is called a *multi-layered power distribution* system.

Resistance of the Power Distribution Wiring

The power distribution wiring resistance causes a voltage drop between the supply and the logic proportional to the current.

This is a problem if the voltage drop falls outside of the logic's operating range.

The resistance and expected operating current is easy to compute.

- Use a bigger wire if necessary -- 40% increase in diameter reduces resistance by 1/2.

New supplies have remote sense wires which monitor the voltage at the far end of the power distribution wiring.

- Here, the supply adjusts the drive voltage to account for wiring resistance (usually up to some limit such as 1/2V).

Inductance in the PWR wiring is a more difficult problem.

- The voltage variations introduced by rapidly changing currents are usually much larger than IR drops.

Inductance of the Power Distribution Wiring

The sense wire circuitry is not able to respond quickly enough to correct for wiring inductance.

There are three approaches to deal with this problem:

- Use lower-inductance wiring
- Use logic immune to power supply noise
- Reduce the size of the changing power supply currents

Since wiring inductance is a logarithmic function of diameter, using a bigger wire is not effective.

The inductance of two parallel power distribution wires (PWR and GND):

$$L = 10.16 L \ln\left(\frac{2H}{D}\right)$$

L = length (in.)
H = ave separation between wires (in.)
D = wire diameter (in.)

Wide, flat parallel structures work **much better** than round wires.

Inductance of the Power Distribution Wiring

A stack of multiple parallel flat ribbons with PWR and GND alternating works well:

$$L = 31.9\frac{XH}{W(N-1)}$$

X = length of ribbon (in.)
W = width of ribbon (in.)
N = # of plates, e.g. 2 for single PWR and GND

Differential transmission is practically immune to power supply fluctuations.

Many times, this is the best solution w.r.t. cost and space for communication between cards.

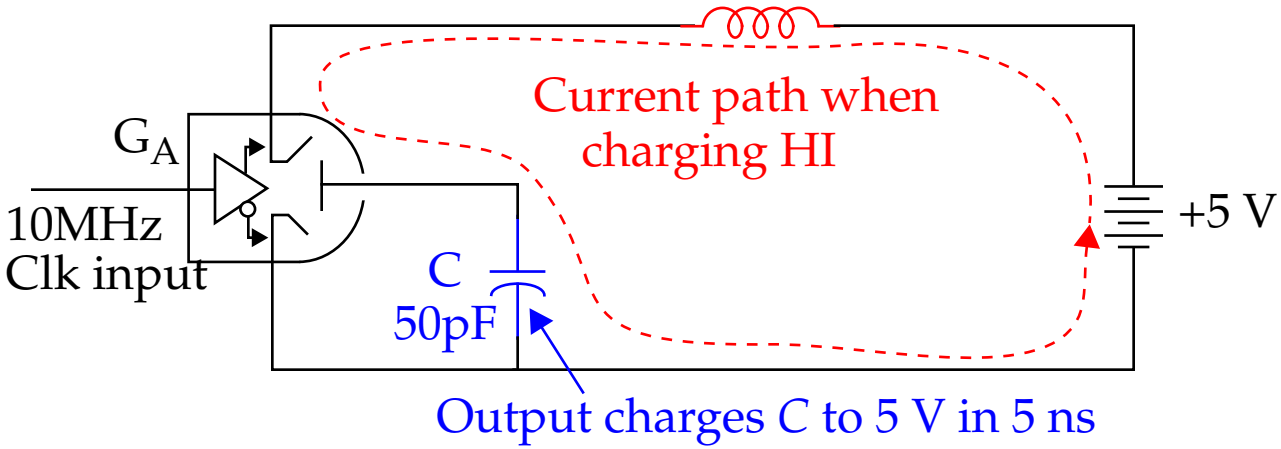
The last approach reduces the magnitude of the changing currents.

Bypass capacitors reduce the **rate of change** but do not reduce the average current.

Let's turn our attention to the design of a power distribution system.

Board-Level Filtering

To illustrate the wiring inductance problem, consider the circuit:



Every 100 ns, there is a spike at the power supply terminal of G_A.

$$Max\frac{dI}{dt} = \frac{1.52\Delta V}{(T_{10\text{-}90})^2}C = 1.5\times 10^7 \text{ A/s}$$

Now construct the inductance of the power supply wiring:

$$L = 10.16X\ln\left(\frac{2H}{D}\right) = 164nH$$

X = 10 in. (length of wire)
H = 0.1 in. (ave separation)
D = 0.04 in. (wire diameter, 18AWG)

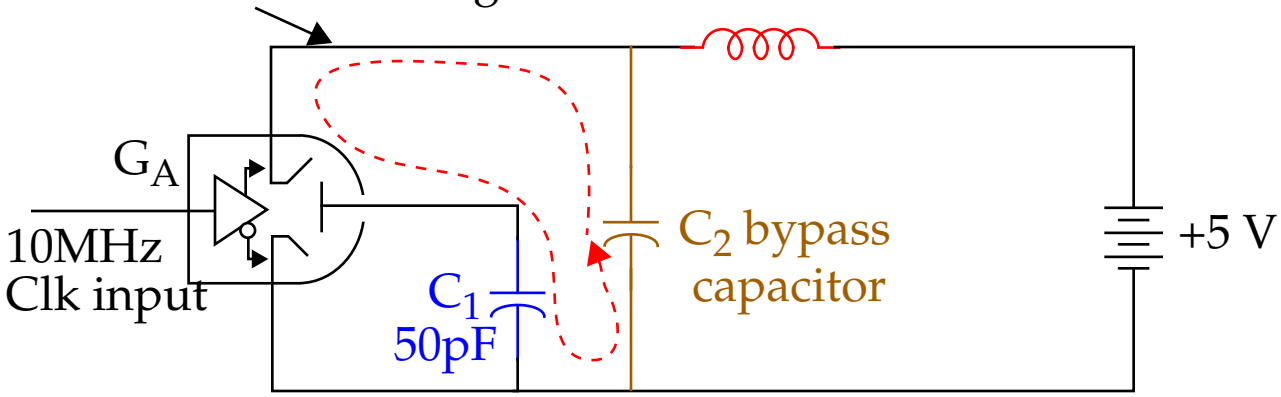
Board-Level Filtering

Multiplying the maximum *dI/dt* by the inductance gives the peak noise voltage:

$$\text{Noise} = (1.5 \times 10^{7})(164 \times 10^{-9}) = 2.5V \text{ !!!}$$

This causes the power supply input on the card to drop significantly and then slowly rise as the inductance charges the capacitor *C*.

Inductance in this short segment is small



This works because the impedance of C_2 is smaller than the impedance of the power wiring.

Board-Level Filtering

Capacitor C_2 smooths the current into a continuous *average* value.

We have effectively reduced the ***rate of change*** in the power wiring.

Here, we see the power supply providing low impedance at **low frequencies** while the bypass capacitor provides low impedance at **high frequencies**.

To determine the correct value of the bypass capacitance:

- Compute the expected maximum step change in supply current (ΔI).
  Use worst case and assume all gates switch simultaneously.

- Compute the maximum amount of power supply noise (ΔV) that your logic can tolerate (add a safety margin (derate)).

- The *maximum* common path impedance is $X_{max} = \Delta V / \Delta I$.
  If solid PWR and GND planes are used, then X_{max} is the maximum impedance of the connection between power and ground.

  Otherwise, portions must be allocated for the PWR and GND wiring.

Board-Level Filtering

To determine the correct value of the bypass capacitance (cont.):

- Compute the inductance of the power supply wiring, L_{PSW}.

  Combine with X_{max} to find the frequency below which the power supply wiring is adequate

  If all gates switch together at this frequency, the power supply noise will be less than ΔV:

$$F_{PSW} = \frac{X_{max}}{2\pi L_{PSW}}$$

- Below frequency F_{PSW}, the power supply wiring is fine, otherwise a ***bypass*** capacitor is needed.

  Find the **lower bound** value of capacitance that has impedance X_{max} at frequency F_{PSW}.

$$C_{\text{bypass}} = \frac{1}{2\pi F_{PSW} X_{max}}$$

Board-Level Filtering

For example, assume:

- 100 gates are switching a 10 pF load in 5 ns.
- The power supply inductance is 100 nH.

The proper value of the *bypass* capacitor is derived from:

$$\Delta I = NC\frac{\Delta V}{\Delta t} = 100(10\times10^{-12})\frac{5V}{5ns} = 1\ A \qquad \text{(worst case peak)}$$

The noise margin is $\Delta V = 0.1$ V

$$X_{max} = \frac{\Delta V}{\Delta I} = 0.1\ \Omega$$

With L_{PSW} at 100 nH, the value of the *bypass* cap is:

$$F_{PSW} = \frac{X_{max}}{2\pi L_{PSW}} = 159\ kHz$$

$$C_{\text{bypass}} = \frac{1}{2\pi F_{PSW} X_{max}} = 10\ \mu F$$

Local Filtering

So far, the power supply and wiring prevent noise up to F_{PSW}.

Above F_{PSW}, the *bypass* capacitor prevents the noise.

Above F_{bypass}, the *bypass* capacitor stops working.

A single "perfect" *bypass* capacitor would solve the problem since the F_{bypass} would be infinite.

Unfortunately, every discrete capacitor has some finite **equivalent series inductance** (lead inductance), L_{C2}.

This increases its impedance at high frequencies.

Whether or not lead inductance is a problem depends on F_{knee} and X_{max}.

The highest frequency for which the *bypass* capacitor is effective is given by:

$$F_{bypass} = \frac{X_{max}}{2\pi L_{C2}}$$

Local Filtering

For example, assume:

- The 10 uF capacitor used in the previous example has a *equivalent series inductance* of L_{C2} = 5 nH.
- Our target impedance is X_{max} is 0.1 Ω.

The maximum frequency it is effective is given by:

$$F_{bypass} = \frac{X_{max}}{2\pi L_{C2}} = 3.18\ MHz$$

Therefore, the effective frequency range of the bypass capacitor is 159 kHz to 3.18 MHz, a range of about 16:1.

To keep below the target impedance above F_{bypass} we need another capacitor with a lower *equivalent series inductance*.

The best way to reduce inductance is to insert an array of capacitors in **parallel** around the circuit board.

Local Filtering

Assume we want our system to work up to F_{knee}.

- First calculate the maximum tolerable inductance:

$$L_{tot} = \frac{X_{max}}{2\pi F_{knee}} = \frac{X_{max} T_r}{\pi}$$

- Look up or measure the *equivalent series inductance* of the *bypass* capacitor that you plan to use, L_{C3}.

  Typical values of **surface mount** capacitors with very short, flat vias is 1 nH while a typical value for **through-hole** is 5 nH.

  Use this value to determine how many *parallel* copies you need to meet the target:

$$N = \frac{L_{C3}}{L_{tot}}$$

Local Filtering

- The total array must have an impedance less than X_{max} at frequencies down to F_{bypass}:

$$C_{array} = \frac{1}{2\pi F_{bypass} X_{max}}$$

- Calculate the capacitance of each element in the array:

$$C_{element} = \frac{C_{array}}{N}$$

To summarize, the impedance between power and ground is upper bounded by:

- The inductance of the power supply routing at low frequencies
- The impedance of a *card-level bypass* capacitor at middle frequencies
- The impedance of a *distributed capacitor array* at high frequencies

Local Filtering

For example, given:

- A 10 uF *bypass* capacitor with a *equivalent series inductance* of 5 nH
- A target impedance of $X_{max} = 0.1\ \Omega$
- $T_r = 5$ ns:

$$L_{tot} = X_{max}\frac{T_r}{\pi} = 0.159nH$$

$L_{C3} = 5$ nH (using the **through-hole** capacitors).

$$N = \frac{L_{C3}}{L_{tot}} = 32 \qquad \text{(\# of caps required)}$$

From the previous example, $F_{bypass} = 3.18$ MHz:

$$C_{array} = \frac{1}{2\pi F_{bypass} X_{max}} = 0.5\ \mu F$$

$$C_{element} = \frac{C_{array}}{N} = 0.016\ \mu F$$

Therefore, we need
32, 0.016 uF capacitors