Capacitance of PWR and GND Planes

Parallel PWR and GND planes provide a third level of *bypass* capacitance and has no lead inductance and no ESR.

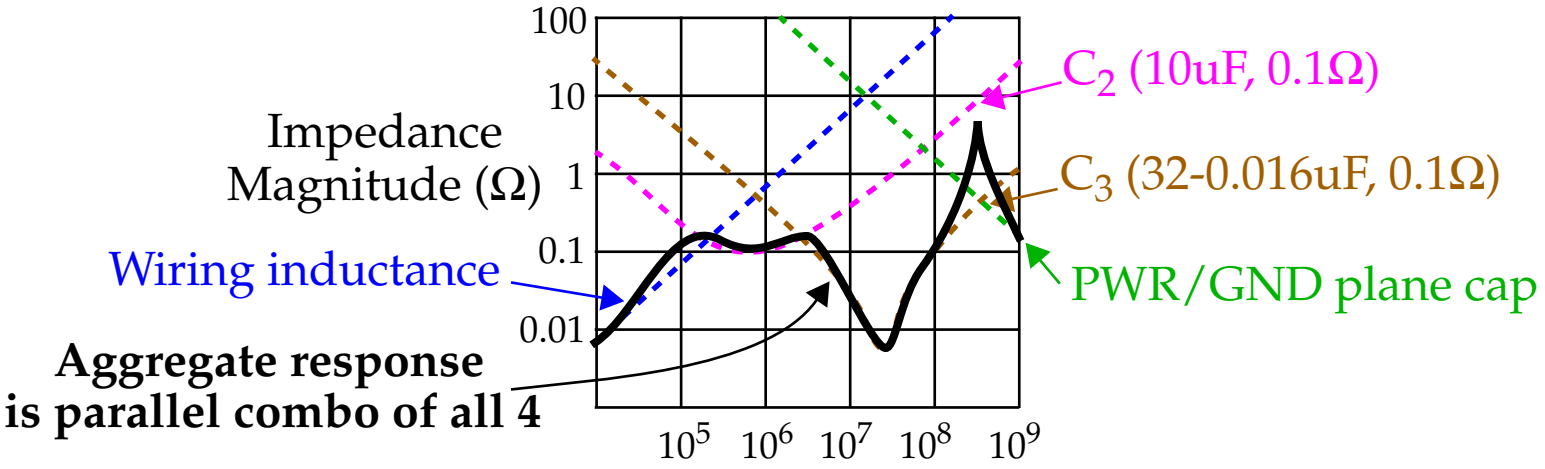
It helps to reduce power and ground noise at very high frequencies.

The capacitance is given by:

$$C_{\text{power plane}} = \frac{0.225\varepsilon_r A}{d}$$

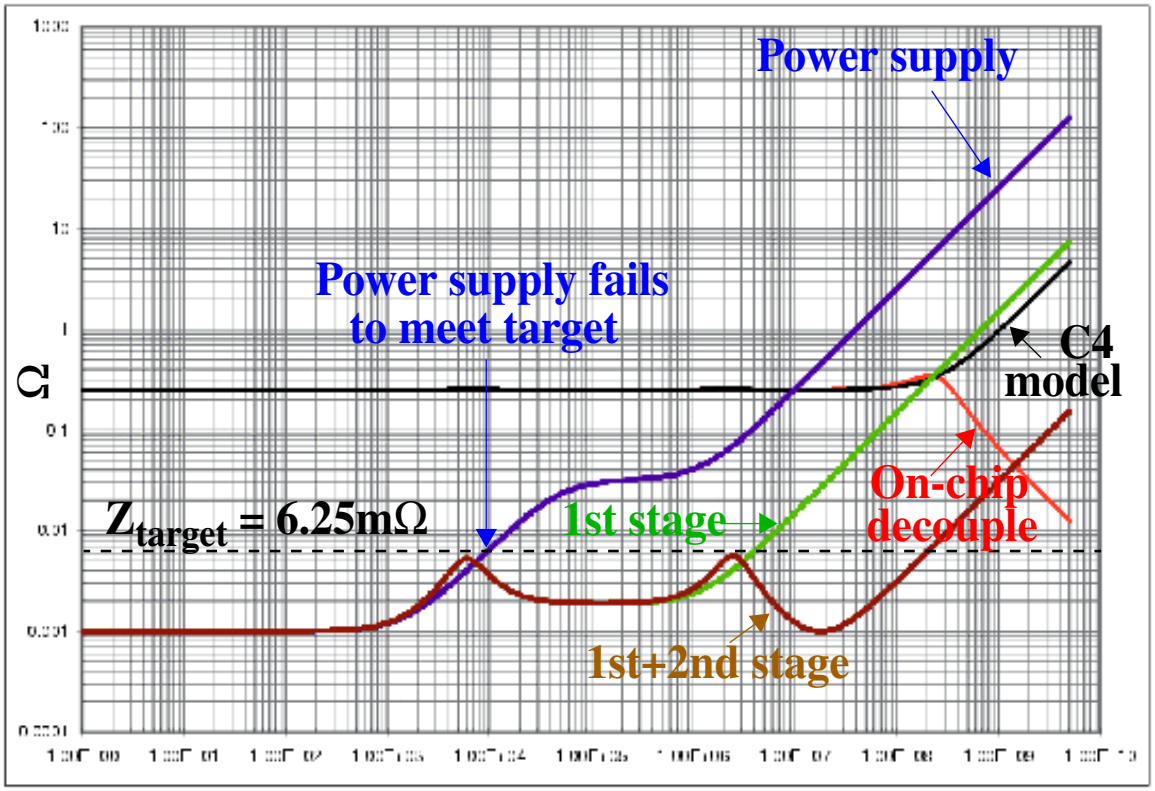
ε_r = relative permeability of FR-4 (4.5)
A and d are the area and separation.

For FR-4, PWR and GND plane capacitance for planes separated by 0.01 in. is 100pF/in^2.



Capacitance of PWR and GND Planes

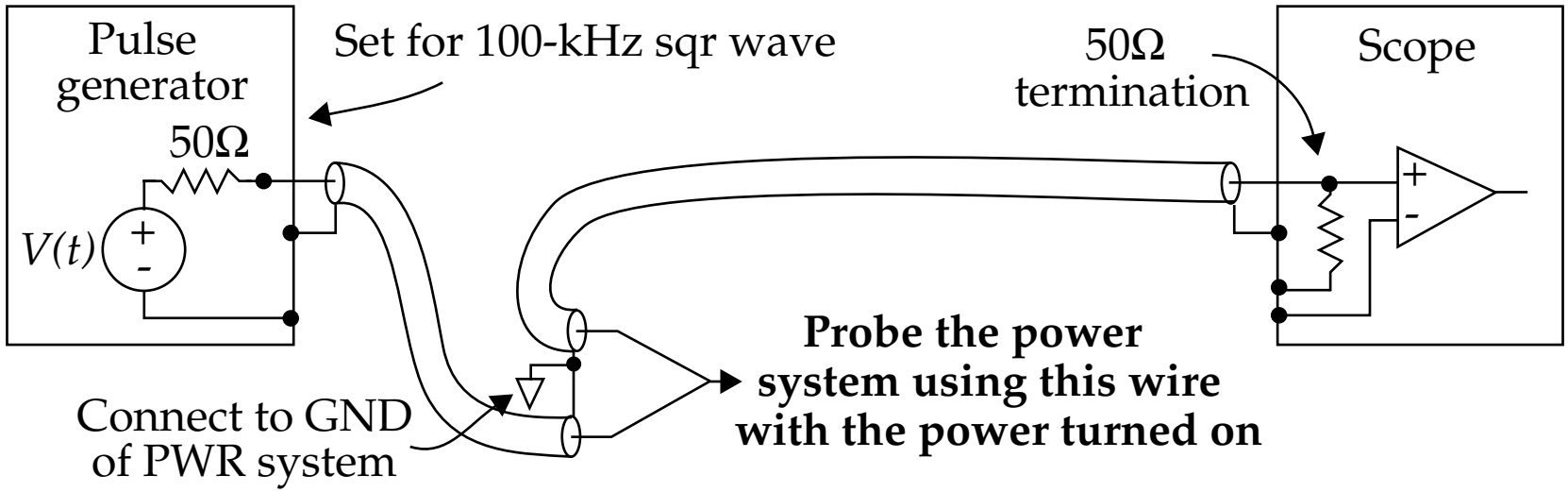
The analysis that Joy did for the 2003 ITC paper on the probe card and chip power grid:



Note that both of these impedance profile plots include the effect of parasitic series resistance of the capacitors called **equivalent series resistance** or **ESR**.

Test Gig for Measuring Step Response of Power Distribution System

This setup applies a small current step to the power system and observes the reaction.



The output impedance of this arrangement is 25 Ω (parallel of 50 Ω from pulse and scope).

Set rise time from pulse generator to rise time expected in system and set output step size to 5 V.

This gives an output current step of 5 V/25 Ω = 0.2 A.

So scale the measured response by ΔI/0.2 to obtain response for ΔI.

Choosing a Bypass Capacitor

Capacitors are not perfect -- each has

- Lead inductance
- Package inductance
- Mounting inductance
- Equivalent series resistance (ESR)
- A dielectric that has significant temperature sensitivity
- A voltage limit over which it "blows out" or shorts out

The ESR is a *real-valued* impedance (not imaginary like inductance) and is not a strong function of frequency.

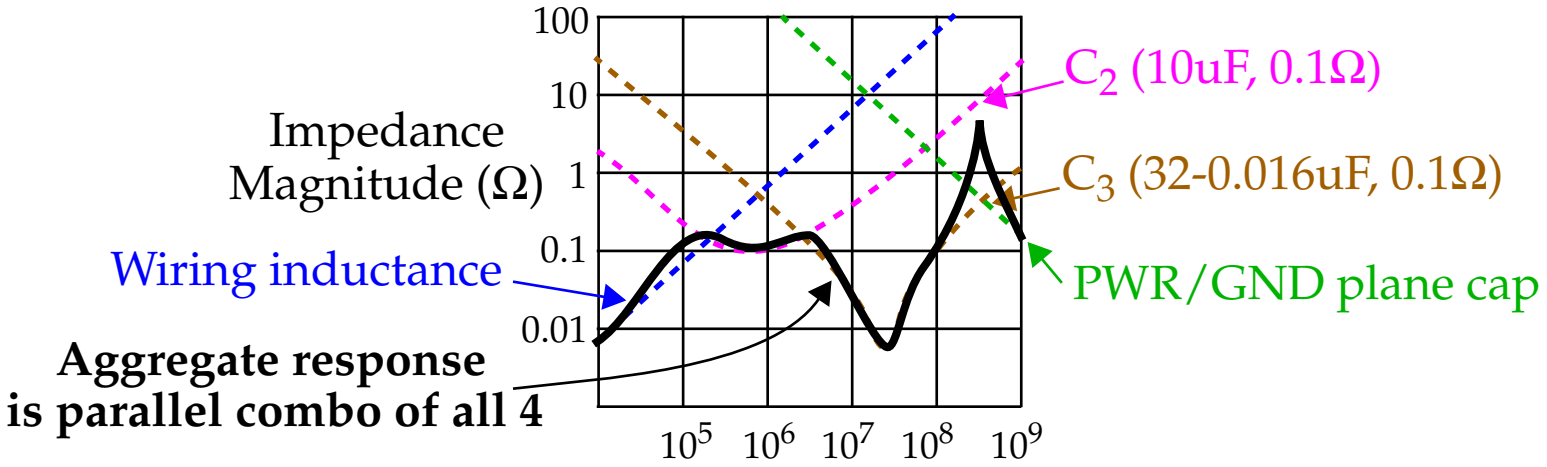
Both *lead inductance* and ESR act in series with the capacitor, degrading its effectiveness as a *bypass* element.

The **impedance magnitude**, *X(f)*, is given by:

$$X(f) = \sqrt{ESR^2 + \left(\frac{-1}{2\pi fC} + 2\pi fL\right)^2}$$

Choosing a Bypass Capacitor

The resonance peak at ~300 MHz is caused by the lead inductance of the capacitor array and the capacitance between PWR and GND planes.



This is not an issue if F_{knee} is down around 100 MHz.

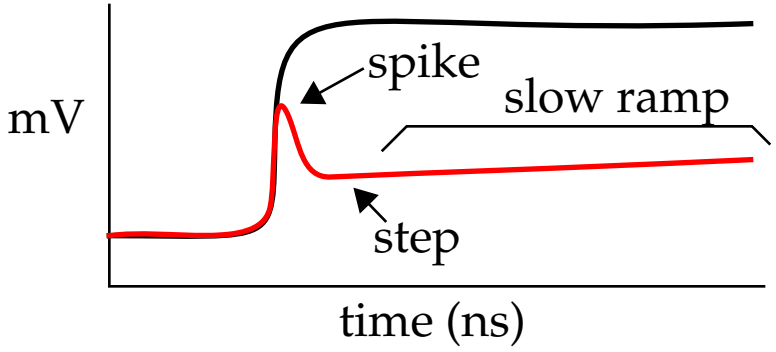
If it is higher, a *surface-mounted* capacitor array raises the resonance frequency and reduces its amplitude.

ESR does not always appear on the manufacturer's data sheet but it is extremely important.

Choosing a Bypass Capacitor

The lead inductance and ESR effect an RC circuit when the R is low.

It quickens the rise time.



The *spike* results from the lead inductance.

The area under the *spike* can be used to compute the inductance.

$$L = \frac{R_S A}{\Delta V}$$

R_S is src resistance of test jig

ΔV is open circuit step voltage of test jig

Immediately following the spike, the wfm is flat and offset from 0.

This is caused by the ESR (capacitor has not yet begun to charge).

$$ESR = \frac{R_S X}{\Delta V - X}$$

X is measured step voltage after spike

Choosing a Bypass Capacitor

Here, a good model is the capacitor is the ESR tied directly to ground.

The source impedance in series with the ESR forms a resistor divider.

The voltage fraction from previous equation X the source resistance yields the ESR.

The effect of the capacitor charging is given by the ramp.

dV/dt is equal to the charging current divided by the capacitance.

$$C = \frac{\Delta V - X}{R_S(dV/dt)}$$

The charging current is equal roughly to the test circuit open-circuit voltage (ΔV) divided by the source resistance.

Bear in mind that the *spike* includes the effect of the lead inductance and ESR.

Remember to subtract out the ESR before measuring the area.