# Design Review: 140W, Multiple Output High Density DC/DC Converter

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## ABSTRACT

*This seminar topic reviews the most common solutions used in multiple output power supply designs. In the focus of the detailed design review is the current-fed push-pull converter, one of the most cost effective solution available for the practicing designer. A step-by-step design procedure will guide the reader through the most important decisions and their effect on the ultimate performance of the circuit. Measurement results, in particular cross-regulation data without using any post regulation technique concludes the topic.*

## INTRODUCTION

Designing multi-output converters presents a remarkable challenge for the power supply designer. There is no comparable power supply design task where specification, topology selection and the choice of output voltage regulation technique would have a more profound effect on the performance, cost and complexity of the final circuitry.

Converters utilizing a single primary power stage and generating more than one isolated output voltage are called multi-output converters. These circuits provide isolation and several output voltages using one high frequency isolation transformer as opposed to individual power modules for each output as it is frequently done in distributed power systems. The decreased system complexity of the multi-output approach is realized primarily on the account of output voltage regulation accuracy. Several approaches have been explored for multi-output converters to address complexity, overall efficiency, output voltage and cross-regulation issues. These circuit solutions can be divided into two radically different groups.

The first group of multi-output converters regulate their main output, from which the feedback signal is generated, with very good accuracy. Their auxiliary outputs are regulated with lesser accuracy since they are not part of a closed loop regulation scheme. These solutions tend to be the most economical ones but their application can be limited because of their inadequate output voltage accuracy. The best known topologies of this category are the flyback, forward and current or voltage-fed push-pull converters.

The second circuit family provides a remedy for those applications where tight voltage regulation of **each** output is necessary. These approaches can be based on almost any topology since they are utilizing some sort of post regulation technique to regulate the auxiliary outputs of a multiple output converter. Accordingly, these solutions are differentiated by the post-regulation technique they are employing. Post regulation of the auxiliary outputs can be achieved by linear post-regulators, individual DC/DC converters, magamp circuits or switchmode Secondary Side Post Regulators (SSPR). All of these techniques are based on closed loop output voltage regulation of their respective outputs.

Before reviewing these power supplies a little bit closer, Figure 1 can be used to position the different solutions on the Cost/Complexity vs. Performance plane. For simplicity and for fair comparison, a three output forward converter is used where it was possible. In each case, it was assumed that the main output is regulated directly by the PWM controller of the power supply. The performance scores of the different solutions were based on expected efficiency and output voltage regulation characteristic. The cost/complexity score was determined by the number of power components (MOSFET and diode switches, inductive components, energy storage capacitors), by the number of integrated circuits required and by the number of control loops employed in that particular solution.

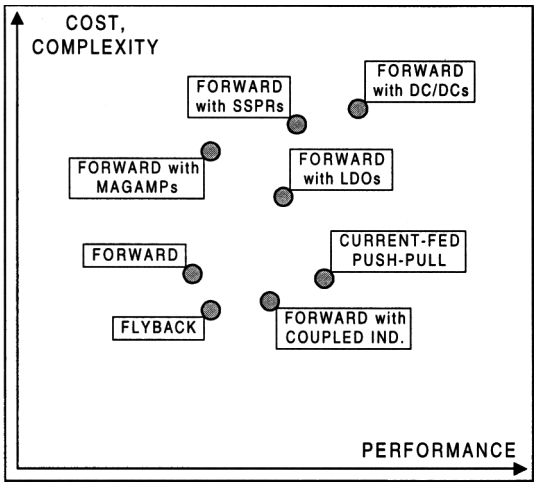


*Figure 1. Cost/Complexity vs. Performance Comparison for Three Output Isolated Converters*

As Figure 1 shows, better performance requires more elaborate solutions which are more complex and more costly. As the specified output voltage accuracies increase for a given multi-output power supply, the solution offers less and less possible simplification. The best performing solution, a forward converter with individual DC/DC converters for the auxiliary outputs, has striking resemblance in complexity and in the number of converters employed, to the starting point, where individual converters have been used for each outputs. The point to make here is that multi-output converters can not offer cost savings and simpler solutions unless the power supply output specification is relaxed accordingly.

## TOPOLOGY OVERVIEW

### *Solutions Without Post Regulator*

Generally, any isolated topology with several secondary windings in the transformer can provide multiple output voltages. These circuits employ a single primary side power stage including the input filter, energy storage capacitor, a high frequency power switch, usually a MOSFET transistor and a PWM controller. On the secondary side, isolated by the transformer, are the output components, rectifiers, energy storage capacitors and output inductors where it is applicable. Among those outputs, one is distinguished as the **main** output whose output voltage is regulated by a feedback loop. The fundamental element of the feedback loop is the voltage error amplifier. Its output provides the feedback signal which is transmitted to the primary side over the isolation barrier. On the primary side, the feedback signal is received by the PWM controller and ultimately determines the duty-cycle of the power switch. It is important to emphasize, that in all of these cases, there is only one controlled quantity, the duty-cycle of the MOSFET, which allows control of only one output parameter, which is the output voltage of the main output. Thus, the output voltage of the main output is accurately regulated.

On the other hand, the auxiliary outputs are not directly regulated by the PWM modulator. The nominal auxiliary output voltages are determined by the turns ratio of the output windings. Their voltage regulation accuracy is a function of the coupling among the **secondary** windings, the voltage drop difference among the rectifier diodes and the voltage drop on the parasitic resistance of the series components of those outputs. These parasitic resistive components, secondary winding resistance, rectifier diode equivalent series resistance, the resistance of the output inductor and the wiring or trace resistance represent a load dependent voltage drop between the secondary winding and the actual output of the power supply. As the load current changes, the auxiliary output voltages will vary accordingly, causing the well know cross regulation error.

#### Flyback Converter

The flyback converter with multiple output windings is the simplest implementation for multi-output power supply. Typical application area for this solution is the low power, low current, multi-output power conversion where semi-regulated output voltages are acceptable and noise requirements are significantly relaxed. To improve noise performance, additional LC post-filters can be added to the outputs. Figure 2 shows a typical circuit diagram of a multi-output flyback converter.

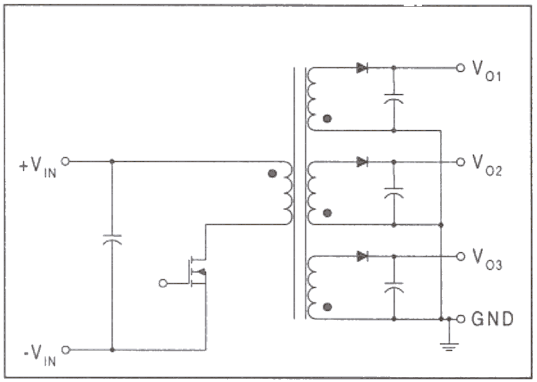


*Figure 2. Multi-Output Flyback Converter*

The advantages of this solution are:

- simple, economical approach
- only one magnetic component
- smallest number of semiconductors
- fair overall efficiency
- single control loop system

The disadvantages are:

- semi-regulated auxiliary outputs
- power throughput is limited by the flyback transformer
- high stress on the energy storage capacitors
- meeting output noise specifications frequently requires post filters
- right half-plane zero in continuous conduction mode limits the control loop bandwidth

**Forward Converter with Individual Outputs**

The forward converter of Figure 3 is rarely used because it utilizes a large number of inductive components. Furthermore, the outputs of the forward converter have more parasitic resistances than the flyback output circuits due to the additional filter inductors. Thus, the cross regulation among the outputs are usually worse than in the flyback converter. Balancing the fact of the poorer output tolerances, the forward converter offers better noise performance. The output filter inductor stores energy and it ensures continuous current flow to the load. Consequently, less output capacitance is required and lower noise specification can be achieved.

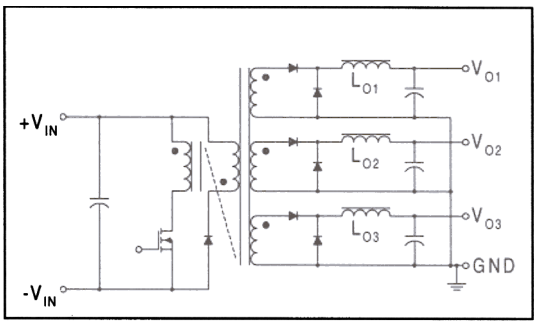


*Figure 3. Forward Converter with Individual Output Inductors*

This solution offers the following benefits:

- simple, well understood power stage
- good for medium power multi-output converters
- continuous current flow to the outputs
- low noise outputs
- good overall efficiency (single stage power conversion)
- single control loop system

The most significant drawbacks are:

- semi-regulated auxiliary outputs
- poor cross-regulation characteristic especially in discontinuous conduction mode of the output filter inductors
- large number of magnetic components

As mentioned before, this solution is rarely found in multi-output power supplies. Remarkably, the fundamental reason for that unpopularity is not the deficiencies of the topology, but the improvements offered by the circuit described in the next section.

**Forward Converter with Coupled Inductors**

The forward converter with coupled filter inductors is well accepted for multi-output power supplies. As shown in Figure 4, the output inductors are wound on a single core. This technique allows all outputs to be dynamically coupled through the shared magnetic core. The coupled inductor stores energy like traditional output inductors and also works like a transformer, improving cross regulation among the outputs. In addition to the performance improvement, using a coupled inductor reduces the number of costly, magnetic components.

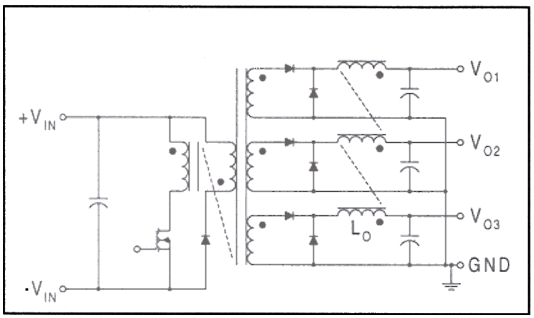


*Figure 4. Coupled Output Inductors in Multi-Output Forward Converter*

In comparison, this circuit has a similar set of advantages and disadvantages as the forward converter with individual output inductors. Additionally, this approach is more cost effective and offers better output voltage regulation due to the coupled output inductors. Therefore, this approach is almost exclusively preferred over individual output inductors.

**Current-Fed Push-Pull Converter**

As one can conclude from the forward converter examples, adding series components to the output circuits, such as filter inductors or current sense resistors will have a negative impact on output voltage and cross regulation properties. On the other hand, having no output inductor, like in the flyback converter, causes higher component stresses, more output noise and limits the output power capability of the converter.

These seemingly antagonistic requirements are conquered in the current-fed push-pull converter shown in Figure 5. The output circuit resembles the flyback configuration since there is no output filter inductor. That minimizes the output voltage regulation error caused by the excess parasitic resistances. Furthermore, the push-pull transformer is driven by a 50%-50% duty-cycle bipolar signal providing continuous power flow to the outputs. That optimizes the core utilization in the isolation transformer as well as reduces output component stresses, noise and makes this circuit suitable for high power applications. The cross regulation of a current-fed push-pull converter is significantly better than any of the previously mentioned topologies.

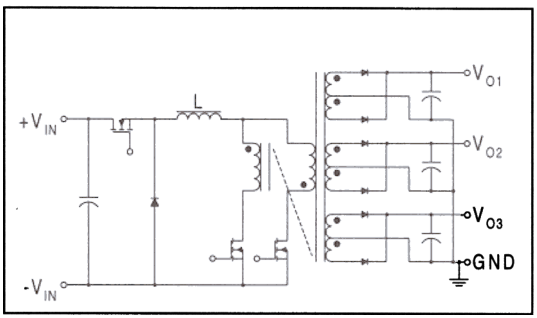


*Figure 5. Three-Output Current-Fed Push-Pull Converter*

The current-fed push-pull converter has the following advantages:

- single winding inductor serves any number of outputs
- few secondary side parasitic components (Rdiode and Rsec)
- continuous current flow to the outputs
- good cross regulation characteristic
- good for medium to high power multi-output converters
- low noise outputs
- good overall efficiency (despite the two stage power conversion)
- single control loop system (push-pull stage is free running)

Disadvantages:

- semi-regulated auxiliary outputs
- highest number of controlled switches in the semi-regulated circuit family
- two stage power conversion

This circuit will be further analyzed and a detailed design procedure is presented later in this paper.

## *Solutions With Post Regulators*

In many applications, especially at lower output voltages, adequate output voltage tolerances can not be achieved without some sort of post regulation of the auxiliary (not directly regulated) outputs. These power supplies might employ any topology with multiple output windings. The main output is still regulated by direct feedback and pulse width modulation of the primary switch in the isolating power stage. Once post regulation is considered, tight cross regulation among the outputs is not critical, however

it might be beneficial to reduce power dissipation and/or optimize the design of the selected post regulator. The four most popular post regulation techniques are reviewed next.

**Linear Post Regulator**

Linear post-regulators are extensively used for low current outputs. A typical application with a multiple output forward converter is shown in Figure 6. Since linear regulators require a minimum voltage drop across the pass element, their application is usually restricted by power dissipation at higher output currents. This voltage drop together with the load current represent a relatively large variable power loss. Although, a low drop out (LDO) linear regulator requires smaller voltage drop between its input and output terminals, this advantage can be utilized only at the minimum input voltage. Unless the input voltage is tightly regulated, at high input voltage the maximum power dissipation of the traditional and the LDO linear regulator is the same.

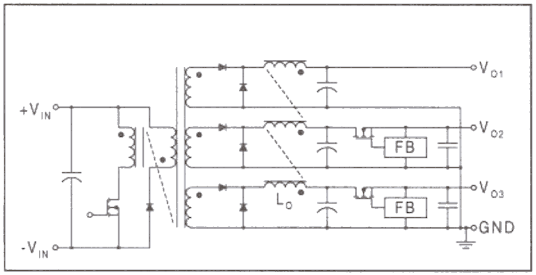


*Figure 6. Typical Linear Post-Regulator Application*

The most significant advantages of using linear post-regulators are:

- simple, cost effective and highly integrated at low currents
- low noise auxiliary outputs
- voltage regulation is independent from the main converter's duty-ratio
- independent overload and short circuit protection

The drawbacks involve:

- limited efficiency
- high dissipation across pass element in overload

**DC/DC Switching Post Regulator**

DC/DC converters, usually simple buck converters, provide efficient, local regulation of the auxiliary outputs in a multi-output power supply. As Figure 7 indicates, this technique employs two cascaded switch mode power converters. The two converters operate independently and offer a great degree of flexibility for the system designer. Since the buck post regulator works from a semi-regulated input voltage, its operating conditions and efficiency can be easily optimized. Synchronization is desirable in most of the cases to reduce interaction between the main converter and the post regulators.

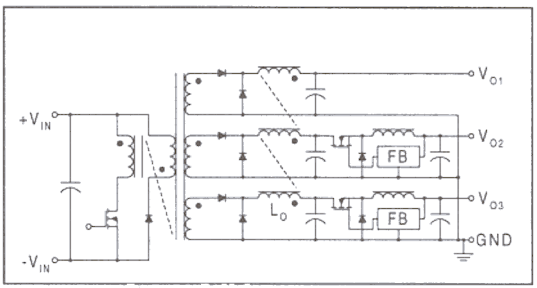


*Figure 7. Buck DC/DC Post Regulator Simplified Schematic*

The switch mode post regulators offer the following advantages:

- high efficiency
- high accuracy
- independent over-load and short circuit protection
- voltage regulation is independent from the main converter's duty-ratio

The list of disadvantages includes:

- complex circuitry
- costly
- usually requires additional bias voltage for controller and/or floating buck driver

**Magamp Post Regulator**

Magamp circuits are very popular in medium to high power application where the limited efficiency of the linear regulators are not acceptable. The saturable reactor in the magamp post regulator functions as a magnetic switch. Before the core of the magamp inductor saturates, it represents a large impedance in series to the secondary winding of the isolation transformer preventing power transfer to that output. By properly positioning the operating point of the magnetic core on the B-H curve, a vari-

able portion of the secondary pulse can be blocked. Thus the effective duty-ratio for the buck inductor can be further modulated, allowing precise regulation of the auxiliary output voltage.

A typical application is depicted in Figure 8.

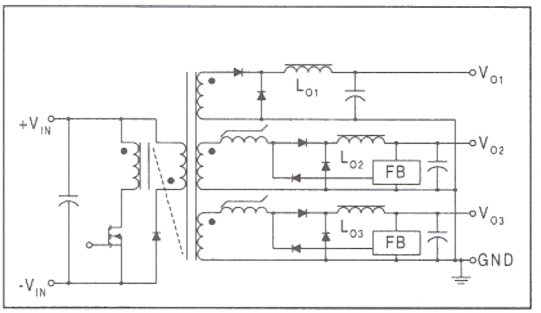


*Figure 8. Typical Magamp Post-Regulator Implementation*

The magamp advantages are:

- good accuracy
- high efficiency at nominal output current

The disadvantages are:

- large number of inductive components
- high cost
- limited operating frequency
- troublesome short circuit protection and no load operation
- auxiliary output duty-cycle is limited by the main output duty-ratio

**Secondary Side Post Regulators (SSPR)**

Integrated circuit manufacturers recently developed several controllers which allow using a cost effective, N-channel MOSFET switch in place of the saturable reactor of the magamp circuit. These solutions are referred to as Secondary Side Post Regulators or SSPRs, in the literature. While the distinct implementations might differ slightly, they can be represented by the simplified schematic of Figure 9. The SSPR circuits address most of the major drawbacks of the magamp solutions. They are compatible with higher switching frequencies, allow easy operation at light load and in short circuit conditions. In addition, they are less expensive and usually take up less board area.

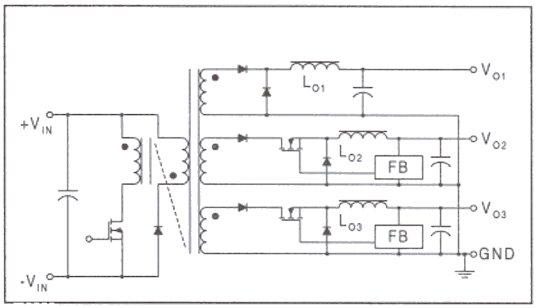


*Figure 9. Secondary Side Post Regulator (SSPR) Circuit Diagram*

SSPR applications profit from:

- high accuracy
- high efficiency under all load conditions
- high frequency operation
- fast transient response
- independent over-load and short circuit protection
- moderate cost

The most significant shortcomings are:

- usually requires additional bias voltage for controller and/or floating buck driver
- high parts count
- large number of controlled switches
- auxiliary output duty-cycle is limited by the main output duty-ratio

## DESIGN REVIEW

The following design review focuses on the design procedure of a three-output DC/DC converter. The first step in any successful design is to determine the power supply specification. The most important parameters are listed in the next paragraph:

### *Specification Overview*

| | |
|---|---|
| Input DC Voltage: | 12V . . . 15V |
| Output DC Voltages: | 28V±0.5V@ 0.5A . . .4A |
| | 12V±0.5V@ 0.2A . . .2A |
| | 5V±0.25V@ 0.2A . . .1.5A |
| Output Power: | 17.5W . . . 143.5W |
| Efficiency: | >85% |
| Isolation: | none |
| Noise: | $100mV_{PP}$@28V |
| | $100mV_{PP}$@12V |
| | $50mV_{PP}$@5V |
| Target Size: | 2.25"x1.3"x0.5" |
| Power Density: | ~$100W/in^3$ |

## *Step-By-Step Design Procedure*

### Topology Selection

The first step is to examine the output voltages, currents, power ratings and their respective tolerance bands. Simple calculations translate the specifications into the following output characteristics:

| | | |
|---|---|---|
| $V_{O1} = 28V \pm 1.8\%$ | $I_{O1} = 4A$ | $P_{O1} = 112W$ |
| $V_{O2} = 12V \pm 4.2\%$ | $I_{O2} = 2A$ | $P_{O2} = 24W$ |
| $V_{O3} = 5V \pm 5\%$ | $I_{O3} = 1.5A$ | $P_{O3} = 7.5W$ |

Assuming that $V_{O1}$ is regulated directly by the power supply's PWM controller, the other output voltage tolerances are adequately relaxed to consider a solution without post regulators. Also note that the currents of the auxiliary outputs are low, therefore voltage drop on the parasitic resistors of the circuits can be kept under control to meet output voltage tolerances including cross-regulation errors.

The next factor influencing the circuit selection is the efficiency and power density goals. Although, the flyback converter appears very attractive because of its simplicity and low parts count, it would be difficult to meet the anticipated 85% efficiency goal especially at high switching frequency which seems inevitable to reach the targeted power density. Furthermore, the flyback approach would require higher than necessary output capacitance values to handle ripple currents due to the high switched current waveform of the output stage. More than likely, additional LC filter stages would also be required to meet the output noise specifications.

The forward converter is the next candidate to explore. Because of its simplicity and lower number of magnetic components, only the coupled filter inductor version is contemplated. This solution can be used at high switching frequency and it has a continuous power flow towards the outputs due to the filter inductor. The output capacitor stresses are reasonable and in continuous conduction mode of the output inductor, the voltage regulation of the auxiliary outputs can be achieved. What makes this implementation less attractive is the duty-cycle limitation determined by the reset time requirements of the isolation transformer and the interaction between leakage inductances and turns ratios between the transformer and the coupled filter inductor windings. Moreover, the coupled filter inductor represents additional load dependent voltage drop in series to the auxiliary outputs.

Ultimately, the current-fed push-pull converter has been selected for this application. As Figure 5 showed, the outputs have minimum number of components, thus cross regulation specification can be met easier than in the forward converters. Also, continuous power flow to the outputs are insured considering the push-pull transistors operate at a nominal 50%-50% duty-ratio all the time. The core utilization of the isolation transformer is optimal because of the first and third quadrant operation, and lack of duty-cycle modulation in the push-pull stage. A single winding inductor resides on the primary side which allows simpler inductor design and better optimization. Consequently, high efficiency and power density can be achieved using the current-fed push-pull solution.

### Operating Frequency

The switching frequency has the utmost influence on the efficiency and size of the power supply. Usually, higher efficiency can be achieved at lower or moderate frequencies as the switching losses of the semiconductors are lower. On the other hand, the size of the reactive components is getting smaller as the operating frequency increases. The trade-off between size and efficiency has to be evaluated very carefully. Remember, that in many applications the final size of the power supply must include the bulk of the heatsink as well. Volume gained in component sizes can be easily forfeited to larger heatsinks as switching losses increase at higher operating frequencies. Therefore, the choice of clock frequency shall be based on the detailed analysis of the switching and conduction losses in the circuit, calculated later in this paper.

### Control Technique

The underlying operating principle of the current-fed push-pull converter is that a current source, i.e. the buck stage, feeds an ideal "switched mode transformer" comprised by the push-pull circuit. By adjusting the source current to the transformer, the output voltage is regulated across the load. Since the basic objective is regulating the inductor current, the

best suited control technique is average current mode control. Average current mode control offers short circuit and overload protection, inherent rejection of input voltage changes, fast transient response and easy current loop setup since slope compensation is not required. Furthermore, using current mode control simplifies the compensation network around the voltage error amplifier. In order to implement average current mode control, the current of the buck inductor has to be sensed and that information is processed by a dedicated current error amplifier. To maximize the overall efficiency of the solution, a low value current sense resistor is desirable. Therefore, the control circuit should also include a current sense amplifier. Ultimately, voltage regulation is accomplished by employing a voltage error amplifier. Another necessity of the control circuit is to be able to drive the floating MOSFET switch of the buck converter and the two ground referenced MOSFET switches of the push-pull power stage. Traditionally, such a controller had to be built from several integrated circuits. Fortunately, all these requirements can be effortlessly addressed using the UC3827-1 integrated circuit, dedicated to control the current-fed push-pull converter.

**Power Components**

Figure 10 shows the final schematic of the power components and their respective reference designators.

***MOSFET Transistors***

The first step is to analyze the operating conditions and losses of the semiconductors on the primary side, which can be separated into switching and conduction losses. The conduction losses are determined by the RMS current of the MOSFET switches and by the average current in D4. Assuming an infinite inductor value, i.e. small ripple current in the buck inductor, the current waveforms are depicted in Figure 11, where $I_L$ is the DC current in the buck inductor, $D_{BUCK}$ is the duty ratio of the buck converter and $t_D$ is the overlap time of the conduction intervals of the push-pull switches.

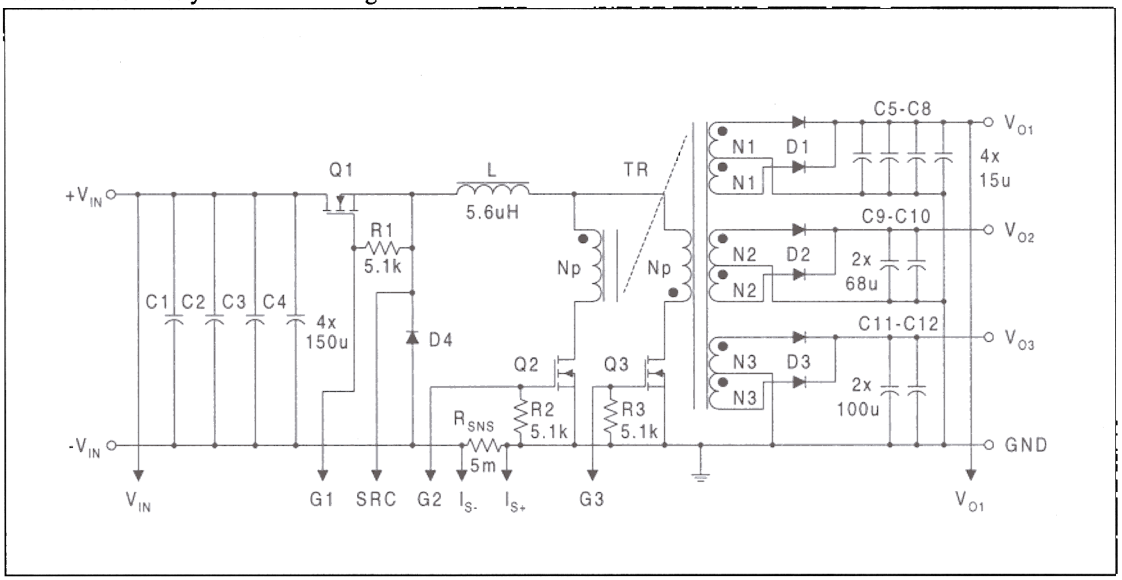


*Figure 10. Three-Output Current-Fed Push-Pull Converter*

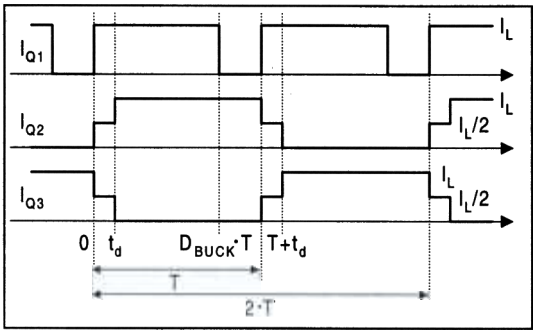


*Figure 11. Current-Fed Push-Pull Converter Current Waveforms*

In all buck derived topologies, efficiency can be maximized if the switch duty ratio is maximized. That condition is fulfilled if the output voltage of the buck converter is just slightly lower then the minimum input voltage of the converter. Assuming $D_{BUCK,MAX}$ = 0.9, the buck output voltage, i.e. the voltage at the centertap terminal of the push-pull transformer, $V_{CT}$ can be calculated:

$$V_{CT} = V_{IN,MIN} \cdot D_{BUCK,MAX} \quad (1)$$

Therefore, $D_{BUCK}$ for any input voltage is given as:

$$D_{BUCK} = \frac{V_{CT}}{V_{IN}} \quad (2)$$

The efficiency of the push-pull stage can be maximized if $t_D$ is minimized. Note, that during the period when Q2 and Q3 conduct simultaneously, there is no energy transfer to the outputs. Therefore, the overlap interval shall be minimized to maintain efficiency and maximum utilization of the push-pull transformer. On the other hand, $t_D$ must be longer than the estimated turn-on time of Q2 (or Q3). The switching times of a MOSFET transistor can be estimated based on the device parameters according to:

$$t_{ON} = \frac{Q_{GD} \cdot R_{GATE}}{V_{GATE} - V_{TH}} \quad (3)$$

$$t_{OFF} = \frac{Q_{GD} \cdot R_{GATE}}{V_{TH}} \quad (4)$$

To ensure that the turn-on switching actions of Q2 (or Q3) are fully completed and both switches are ON by the end of the $t_D$ interval, $t_D > t_{ON}$ must be selected. To provide proper margins under all operating conditions, $t_D$ = 150ns was chosen for this design.

The switch RMS currents and the diode average current value can be determined from the current waveforms. The derivation yields the following expressions:

$$I_{RMS,Q1} = I_L \cdot \sqrt{D_{BUCK}} \quad (5)$$

$$I_{RMS,Q2} = I_{RMS,Q3} = I_L \cdot \sqrt{0.5 - \frac{t_D}{4 \cdot T}} \quad (6)$$

$$I_{AVE,D4} = I_L \cdot (1 - D_{BUCK}) \quad (7)$$

The conduction losses are calculated at 125°C worst case junction temperature according to:

$$P_{COND,Q1} = 1.6 \cdot R_{DSON} \cdot I^2_{RMS,Q1} \quad (8)$$

$$P_{COND,Q2} = P_{COND,Q3} = 1.6 \cdot R_{DSON,Q2} \cdot I^2_{RMS,Q2} \quad (9)$$

$$p_{COND,D4} = V_{FWD,D4} \cdot I_{AVE,D4}$$

The MOSFET switching losses are broken down as gate charge loss, $C_{OSS}$ loss, turn-on and turn-off losses as given by the following equations:

$$P_{GATE} = Q_{GATE} \cdot V_{GATE} \cdot f_S$$

$$P_{COSS} = \frac{1}{2} \cdot C_{OSS} \cdot V^2_{OFF} \cdot f_S$$

$$P_{ON+OFF} = \frac{1}{2} \cdot V_{OFF} \cdot I_L \cdot (t_{ON} + t_{OFF}) \cdot f_S$$

where $Q_{GATE}$ is the total gate charge, $V_{GATE}$ is the gate drive voltage, $f_S$ is the clock frequency, $C_{OSS}$ is the drain-source capacitance of the MOSFET, $t_{ON}$ and $t_{OFF}$ are the switching times estimated in (3) and (4). $V_{OFF}$ is the drain voltage during the off-time of the transistor which equals:

$$V_{OFF,Q1} = V_{IN}$$

$$V_{OFF,Q2} = V_{OFF,Q3} = 2 \cdot V_{CT}$$

The switching losses for the buck freewheeling diode can be neglected since a Schottky rectifier is considered. Schottky rectifiers are inherently free from the reverse recovery phenomena which is the

major source of switching losses in the rectifier diodes.

In order to see the effect of the die size and to find the optimum balance between switching and conduction losses versus operating frequency, two different MOSFETs, a 24mΩ IRFZ44N and an 8mΩ IRF3205 were examined. After collecting all device parameters, (5) through (15) were evaluated quantitatively at full load and nominal input voltage. The losses of the buck transistor and one of the push-pull transistors for this application are shown in Figure 12.

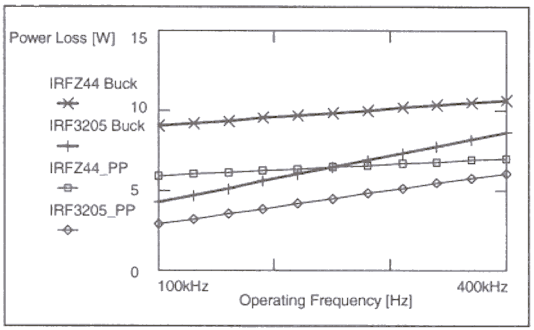


*Figure 12. MOSFET Losses vs. Frequency*

The graph shows the power dissipation from 100kHz to 400kHz which was considered the practical clock frequency range for this application. In this frequency range, the larger MOSFET offers significantly lower losses due to lower conduction losses. Note, that examining the trends in the graph suggest that at even higher switching frequencies the two curve pairs would cross each other. Above the crossover points the higher $R_{DSON}$ device would be more desirable because of the lower switching losses. The clock frequency where the two curves cross is a function of the device currents and supply voltages. In this application the MOSFETs are carrying high currents and working with low voltages, and therefore, the crossover point is at very high frequency. Another conclusion of Figure 12 is that the operating frequency should be kept as low as possible in order to improve efficiency. Taking into account the desired size and power density, a 200kHz clock frequency and the IRF3205 MOSFETs have been selected for Q1, Q2 and Q3 switches.

***Rectifier Diodes***

Next, the rectifier diodes, D1 through D4 will be selected. Since the input side of the circuit processes high current and low voltage levels, it is most common to use a Schottky rectifier. Schottky diodes are usually selected by their forward voltage drop at their rated current. While low voltage drop is definitely an essential parameter here, there is one more important property to consider. That is the maximum junction temperature of the device.

| Part Number | Vfwd@25°C and 25A | $T_{J,MAX}$ |
|---|---|---|
| MBR2535CT | 0.76V | 150°C |
| MBR2535CTL | 0.55V | 125°C |
| MBR2515L ("ORING" diode) | 0.45V | 100°C |

*Table 1. Schottky Diode Parameters*

For instance, comparing the three Motorola Schottky rectifiers in Table 1 reveals that lower forward voltage drop and maximum junction temperature are traded against each other in Schottky technology. Therefore, it is important to check both parameters. In this design, MBR2535CTL is used as the freewheeling diodes of the buck stage (D4) and the rectifier diode of the 5V output (D3).

The other two output rectifiers, D1 and D2 employ ultrafast epitaxial diodes. A unique property of the current-fed push-pull stage is that the reverse voltage across the rectifier diodes is independent of the input voltage. Due to the symmetrical waveform of the transformer windings and the lack of output inductors, all diodes block twice their respective output voltages. Leaving sufficient safety margin for possible switching spikes, D1 must be rated for at least 100V while D2 is at least a 50V diode. Ultimately, D1 and D2 have been selected as the BYQ28-100 from Philips Semiconductors.

***Transformer Design***

The following section is dedicated to define the transformer turns ratios. The fundamental problem in the turns ratio selection is to find the smallest number of turns which provide sufficient resolution to set the required output voltages. In order to obtain fairly accurate results, the calculation has to take into account the voltage drop across the rectifier diodes. There-

fore, the following parameters have to be found based on the diode datasheets:

a) $V_{D1}$, the forward voltage drop of the rectifier diode at the rated output current of the 28V output, $V_{O1}$.
b) $V_{D2}$, the forward voltage drop of the rectifier diode at the rated output current of the 12V output, $V_{O2}$.
c) $V_{D3}$, the forward voltage drop of the rectifier diode at the rated output current of the 5V output, $V_{O3}$.

The process is somewhat iterative and starts by selecting the number of turns for the lowest output voltage, N3. Once N3 is chosen, using the nominal output voltage values, the required number of turns for the other outputs can be obtained according to:

$$N1 = \frac{V_{O1,NOM} + V_{D1}}{V_{O3,NOM} + V_{D3}} \cdot N3 \quad (16)$$

$$N2 = \frac{V_{O2,NOM} + V_{D2}}{V_{O3,NOM} + V_{D3}} \cdot N3 \quad (17)$$

$$Np = \frac{V_{CT}}{V_{O3,NOM} + V_{D3}} \cdot N3 \quad (18)$$

After all the number of turns are found, the actual value of the output voltages can be determined. For this calculation, assume that $V_{O1}$ always equals its nominal value (28V) because that output is directly regulated by the feedback loop. For the other outputs, the following equations prevail:

$$V_{O2} = (V_{O1} + V_{D1}) \cdot \frac{N2}{N1} - V_{D2} \quad (19)$$

$$V_{O3} = (V_{O1} + V_{D1}) \cdot \frac{N3}{N1} - V_{D3} \quad (20)$$

$$V_{CT} = (V_{O1} + V_{D1}) \cdot \frac{Np}{N1} \quad (21)$$

The results from solving equations (16) through (21) for this particular application, are summarized in Table 2.

| N3 | N1 | N2 | Np | $V_{O1}$ | $V_{O2}$ | $V_{O3}$ | $V_{CT}$ |
|---|---|---|---|---|---|---|---|
| 1 | 3 | 6 | 2 | 28V | 13.65V | 4.57V | 9.63V |
| **2** | **5** | **11** | **4** | **28V** | **12.34V** | **5.01V** | **10.51V** |
| 3 | 7 | 16 | 6 | 28V | 12.8V | 4.85V | 10.02V |
| 3 | 8 | 17 | 6 | 28V | 11.84V | 5.17V | 10.84V |
| 4 | 10 | 22 | 8 | 28V | 12.34V | 5.01V | 10.51V |
| 5 | 12 | 27 | 10 | 28V | 12.04V | 5.10V | 10.7V |
| 7 | 17 | 38 | 14 | 28V | 12.13V | 5.07V | 10.65V |
| 16 | 39 | 88 | 32 | 28V | 12.01V | 5.01V | 10.51V |

*Table 2. Different Turns Ratio and Output Voltage Variations*

Table 2 demonstrates the iterative nature of turns ratio selection. The calculations are executed starting with different number of turns for N3, then the results is compared to the regulation range given in the power supply specification.

The inaccuracies are caused by rounding the number of turns, thus recalculating the actual output voltages with integer turns is essential. For this example, the second row has already provided an acceptable solution, the rest of Table 2 is just for demonstration purposes. As the number of turns for N3 increased, the resolution increases, and the voltages close in on the nominal values. The best resolution has been achieved in the last row. Although, N3 = 16 looks rather arbitrary pick for $V_{O3}$, it is not. Close to optimum resolution can be reached when the voltage across one turn in the transformer equals the lowest voltage drop across the rectifier diodes. The problem with this approach is that the resulting number of turns are usually too high for practical purposes.

Next the transformer core is selected based on the maximum volt·second product the transformer has to withstand:

$$V \cdot S = V_{CT} \cdot (T - t_D) \quad (22)$$

Although, the details of the core selection are not discussed here, two alternative winding structures are worthwhile mentioning.

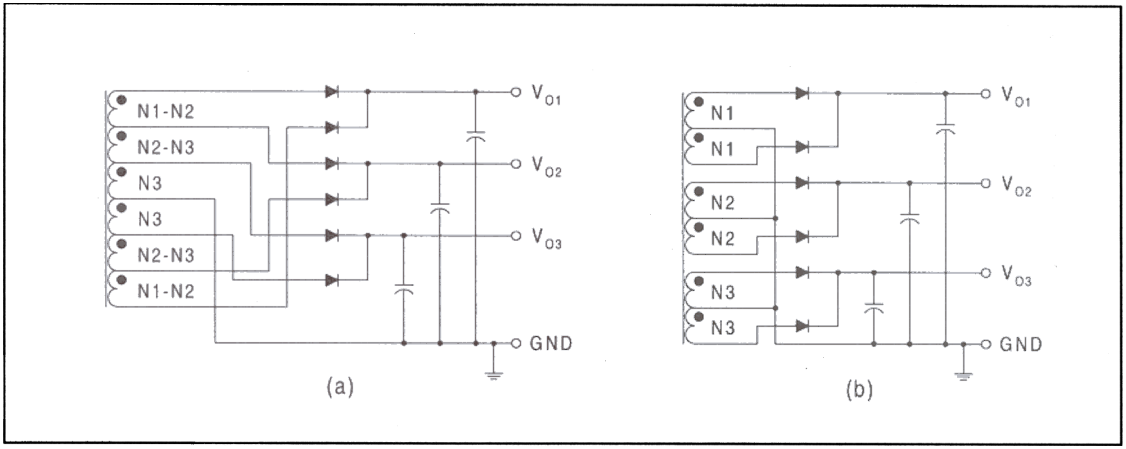


*Figure 13. Different Output Winding Arrangements*

Version (a) of Figure 13 shows an incremental winding structure, where the different output voltages are generated by tapping the N1 winding at the required number of turns. Version (b) indicates individual windings for each outputs. To decide which solution gives better cross regulation, the following equivalent circuits are introduced in Figure 14.

Estimating cross regulation properties starts at calculating the voltage across a single turn in the transformer, V1T. For this, all parasitic resistor values and the current through them must be known. The transformer winding resistances can be estimated using the average turn length and the wire cross section or can be measured once the transformer is wound. The diode parameters can be read from the diode manufacturers' datasheet. The unknown currents I1, I2 and I3 can be calculated from the load currents and from the effective duty-ratio of the push-pull converter:

$$I1 = \frac{I_{O1}}{D_{EFF}} \tag{23}$$

$$I2 = \frac{I_{O2}}{D_{EFF}} \tag{24}$$

$$I3 = \frac{I_{O3}}{D_{EFF}} \tag{25}$$

where

$$D_{EFF} = 1 - \frac{t_D}{T} \tag{26}$$

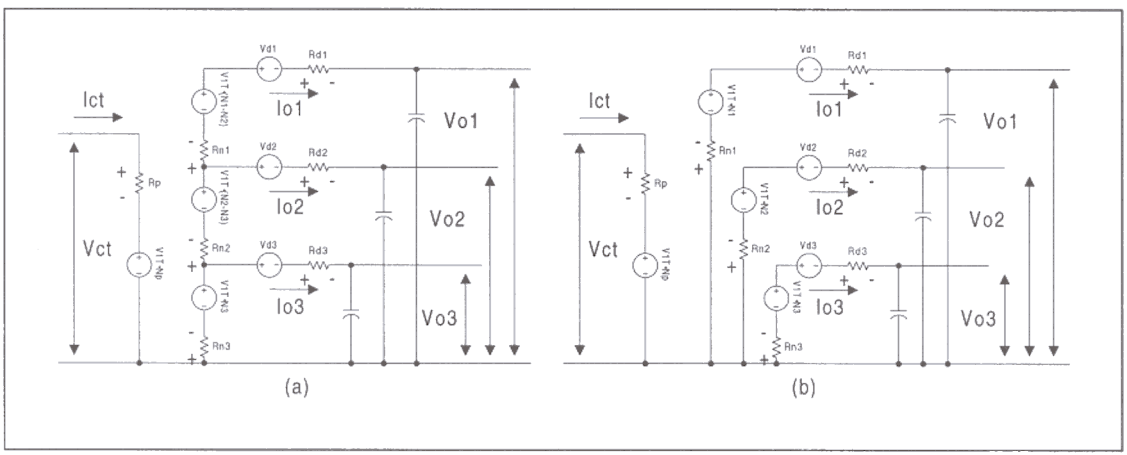


*Figure 14. Equivalent Output Circuits*

Until this point the equations are identical for both equivalent circuits. Hereafter, the relationships for version (b) are determined. Similar equations can be derived and solved for (a) the results of which will also be presented later. Assuming that $V_{O1}$ is regulated, the voltage across a single turn is given as:

$$V1T = \frac{V_{O1} + V_{D1} + I1 \cdot (R_{D1} - R_{N1})}{N1} \quad (27)$$

The unregulated output voltages can be obtained from:

$$V_{O2} = V1T \cdot N2 - V_{D2} - I2 \cdot (R_{N2} + R_{D2}) \quad (28)$$

$$V_{O3} = V1T \cdot N3 - V_{D3} - I3 \cdot (R_{N3} + R_{D3}) \quad (29)$$

The incremental winding structure shown in Figure 14(a), can be analyzed using the same approach. In this case, the single secondary winding has 11 turns in three sections. The first section is composed of N3 = 2 turns, after which the secondary is tapped to supply the 5V output, $V_{O3}$. The middle section has 3 turns which, together with the 2 turns of the first section, comprises N2 = 5 turns. Thus, the series connection of the first and second section provides for the 12V output, $V_{O2}$. The third section of the secondary winding has 6 turns. Similarly, this section is connected in series to the first two winding sections. The total number of turns in the three section is then N1 = 11 turns which is required to supply the 28V output, $V_{O1}$. Note that the parasitic resistances shall be determined for each individual sections separately.

The predicted cross regulations for both (a) and (b) versions, using the numerical values of this application, are summarized in Table 3.

| Load Currents | | | Version (a) | | Version (b) | |
|---|---|---|---|---|---|---|
| $I_{O1}$ | $I_{O2}$ | $I_{O3}$ | $V_{O2}$ | $V_{O3}$ | $V_{O2}$ | $V_{O3}$ |
| min | min | min | **12.272V** | **4.98V** | 12.317V | 4.992V |
| min | min | max | 12.22V | 4.891V | 12.317V | **4.87V** |
| min | max | min | 12.12V | 4.939V | **12.226V** | 4.992V |
| max | min | min | 12.094V | 4.905V | **12.35V** | **5.005V** |
| min | max | max | 12.068V | 4.85V | **12.226V** | **4.87V** |
| max | min | max | 12.042V | 4.816V | **12.35V** | 4.883V |
| max | max | min | 11.941V | 4.864V | 12.259V | **5.005V** |
| max | max | max | **11.889V** | **4.775V** | 12.259V | 4.883V |

*Table 3. Cross Regulation Predictions*

Several conclusions can be drawn from the data listed in Table 3. First of all, cross regulation is better in (b) because there is no cross regulation effect between the auxiliary outputs. For instance, $V_{O2}$ in equation (28) does not contain any term which would depend on $I_{O3}$. Furthermore, the numbers show that the cross regulation between the regulated output and each of the auxiliary outputs is improved as well. That can be explained by the fact that the voltage drop on $R_{N2}$ and $R_{N3}$ is not changing when $I_{O1}$ varies. The cross regulation error is caused by the variation in the term V1T only, when the load is changing on the main output. All these conclusions warrant the choice of output configuration (b) for this design.

There are some warnings which have to be made at this point. The numbers above are just rough estimates on cross regulation error and the transformer leakage inductances will definitely make them worse. Therefore, it is very important that the transformer is optimized for minimum leakage inductance. Among all the different techniques to reduce leakage inductance, interleaving and using the lowest number of layers are the most important ones. Be aware also that the transformer windings carry high frequency currents. Minimizing the number of layers will have a beneficial effect on the ratio between AC and DC resistances of the windings. Also important to remember is that coupling between the different windings is maximized if they occupy the same width in the bobbin and the vertical distance is minimized between them.

Finally, it is noteworthy to mention that for a two-output application versions (a) and (b) provide almost identical cross regulation. In that case, the most optimal layout of the transformer windings should be considered as the guiding rule.

***Buck Inductor***

The second, and last magnetic component of the current-fed push-pull converter is the buck inductor which is much easier to design. To improve performance, the buck inductor is designed to stay in continuous conduction mode at minimum output power. Therefore, the maximum ripple current is calculated from:

$$\Delta I_{L,MAX} = \frac{2 \cdot P_{OUT,MIN}}{V_{CT} \cdot D_{EFF}} \quad (30)$$

The largest ripple current occurs at $V_{IN,MAX}$ hence the minimum inductance of the buck inductor is given as:

$$L = \frac{V_{IN,MAX} - V_{CT}}{\Delta I_{L,MAX}} \cdot D_{BUCK,MIN} \cdot T \qquad (31)$$

where

$$D_{BUCK,MIN} = \frac{V_{CT}}{V} \qquad (32)$$

The peak inductor current is calculated at maximum input voltage and full output power according to:

$$I_{L,PEAK} = \frac{P_{OUT,MAX}}{V_{CT} \cdot D_{EFF}} + \frac{1}{2} \cdot \Delta I_{L,MAX} \qquad (33)$$

Note, that in buck derived topologies the average inductor current is independent from the input voltage. It is always equal to the DC output current. As the input voltage changes, the varying duty-ratio of the buck switch will cause the average input current to change. That is why the peak inductor current is calculated at full load current and at maximum input voltage where the largest ripple current amplitude occurs. Substituting the application parameters, the inductor value is found to be 5.4µH and it is rated for at least 16A.

As the reader might have already realized, the core selection procedure, core loss analysis are not discussed in this article. For those intricate details, refer to Lloyd Dixon's numerous and excellent publications on magnetic design.

***Energy Storage Capacitors***

The next components to select are the filter capacitors. Starting on the output side and assuming infinite buck inductance, the waveforms of $C_{O1}$ (C5-C8), $C_{O2}$ (C9-C10) and $C_{O3}$ (C11-C12) can be approximated by the ones of Figure 15.

The output capacitors are determined by the ripple voltage specification, $V_{PP}$, and by their RMS current handling capability. The switching frequency ripple is due to the voltage drop caused by current flowing through the equivalent series resistor (ESR) of the capacitor and due to the fact that the capacitor supplies the load current while power flow from the

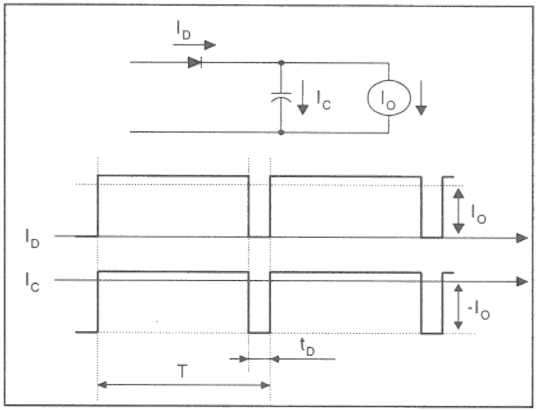


*Figure 15. Output Capacitor Current Waveforms*

input is interrupted, i.e. during $t_D$ in this particular design. As a starting point, half of the specified ripple amplitude has been allocated for voltage drop across the ESR of the capacitors, approximately twenty percent for voltage decay during the gap time and the remaining amplitude is reserved to cover spikes caused by the switching actions in the circuit. Based on these assumptions, the following relationships can be established:

$$C_{O,MIN} = \frac{I_O \cdot t_D}{0.2 \cdot V_{PP}}$$

$$ESR_{MAX} = \frac{0.5 \cdot V_{PP}}{I_O \cdot \left(1 + \frac{t_D}{T - t_D}\right)} \qquad (35)$$

The output capacitor RMS currents can be determined from the current waveforms of Figure 15, yielding:

$$I_{C,RMS} = I_O \cdot \sqrt{\left(1 + \frac{t_D}{T - t_D}\right) \cdot \frac{t_D}{}}$$

Substituting the output current ratings and respective ripple voltages, equations (34), (35) and (36) give the minimum capacitance, maximum ESR and RMS current requirements listed in Table 4:

| | $C_{O1}$ | $C_{O2}$ | $C_{O3}$ |
|---|---|---|---|
| $C_{O,MIN}$ | 30µF | 15µF | 23µF |
| $ESR_{MAX}$ | 12mΩ | 24mΩ | 16mΩ |
| $I_{C,RMS}$ | 0.7A | 0.35A | 0.26A |

*Table 4. Output Capacitor Requirements*

The actual output capacitance values listed in the schematic, Figure 10, were chosen to provide the required ESR values. Following this approach to calculate output capacitance requirements allows the use of a very small LC post-filter stage if necessary because that post filter stage will not have to work at the switching frequency. It would be used only to suppress the switching spikes which are much higher frequency signals.

On the input side, the filter capacitor is designed following a similar approach. For the buck converter the input capacitor stresses are the highest at D = 0.5. In this application D = 0.5 is never reached, thus the calculation is executed at maximum input voltage, where the duty ratio is the closest to 50%. The capacitor current waveform is indicated in Figure 16.

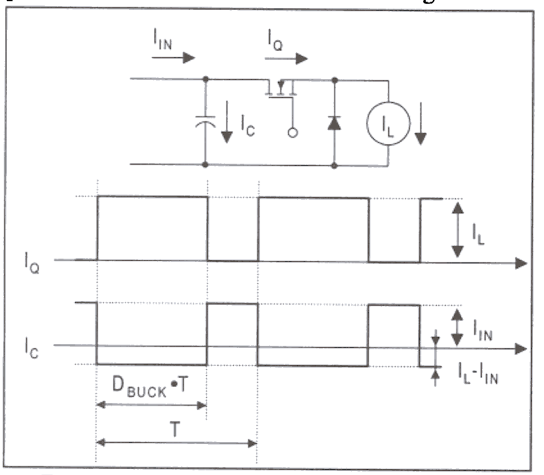


*Figure 16. Input Capacitor Current Waveforms*

Allowing 200mV ripple on the input capacitor and following the same guidelines established for the output capacitors, the capacitor parameters can be found from the modified equations (37) through (39).

$$C_{IN,MIN} = \frac{I_L \cdot (D - D^2) \cdot T}{0.2 \cdot V_{PP}} \quad (37)$$

$$ESR_{MAX} = \frac{0.5 \cdot V_{PP}}{I_r} \quad (38)$$

$$I_{C,RMS} = I_L \cdot \sqrt{D - D^2} \quad (39)$$

Substituting for the worst case conditions, the minimum input capacitance value equals 450µF, the maximum acceptable ESR is 6.3mΩ and the capacitor RMS current rating has to be higher than 7.6A. These numbers required several parallel connected capacitors at the input as shown in Figure 10.

***Current Sense Resistor***

Lastly, the current sense resistor value is calculated. In order to minimize power dissipation and taking advantage of the internal current sense amplifier of the UC3827, the current sense resistor is chosen to furnish only a 100mV signal at maximum current in the circuit. This maximum current shall be determined to give sufficient margin for parameter tolerances. Therefore, instead of the calculated 16A peak inductor current, $I_{MAX}$ = 20A is taken into consideration.

Accordingly, the sense resistor value and its power dissipation is defined as:

$$R_{SENSE} = \frac{0.1V}{I_{MAX}} \quad (40)$$

$$P_{RSENSE} = R_{SENSE} \cdot I_{MAX}^2 \quad (41)$$

which yields 5mΩ at a 2W power rating.

**UC3827 Current/Voltage-Fed Push-Pull Controller**

First the block diagram and the basic functions of the integrated controller are presented. Figure 17 shows the internal architecture of the UC3827 used in this design. The IC operates within the 10V to 20V supply voltage range and includes all of the usual housekeeping functions, undervoltage lockout, soft start circuitry, an externally accessible 5V reference and synchronizable oscillator. The push-pull control section comprises of the push-pull latch, the delay block and two ground referenced high current gate drive outputs serving the two MOSFETs of the push-pull converter. The delay circuit in the UC3827-1 provides a user programmable interval for overlapping conduction time between the push and pull outputs for current-fed operation. In another version of this controller, the UC3827-2, the delay circuit provides a dead time between the conduction intervals for voltage-fed operation.

The buck pulse width modulator section consists of a PWM comparator, a current limit comparator, a PWM latch and a high voltage, floating driver stage. The PWM comparator inputs receive the control signal from the output of the current error amplifier and

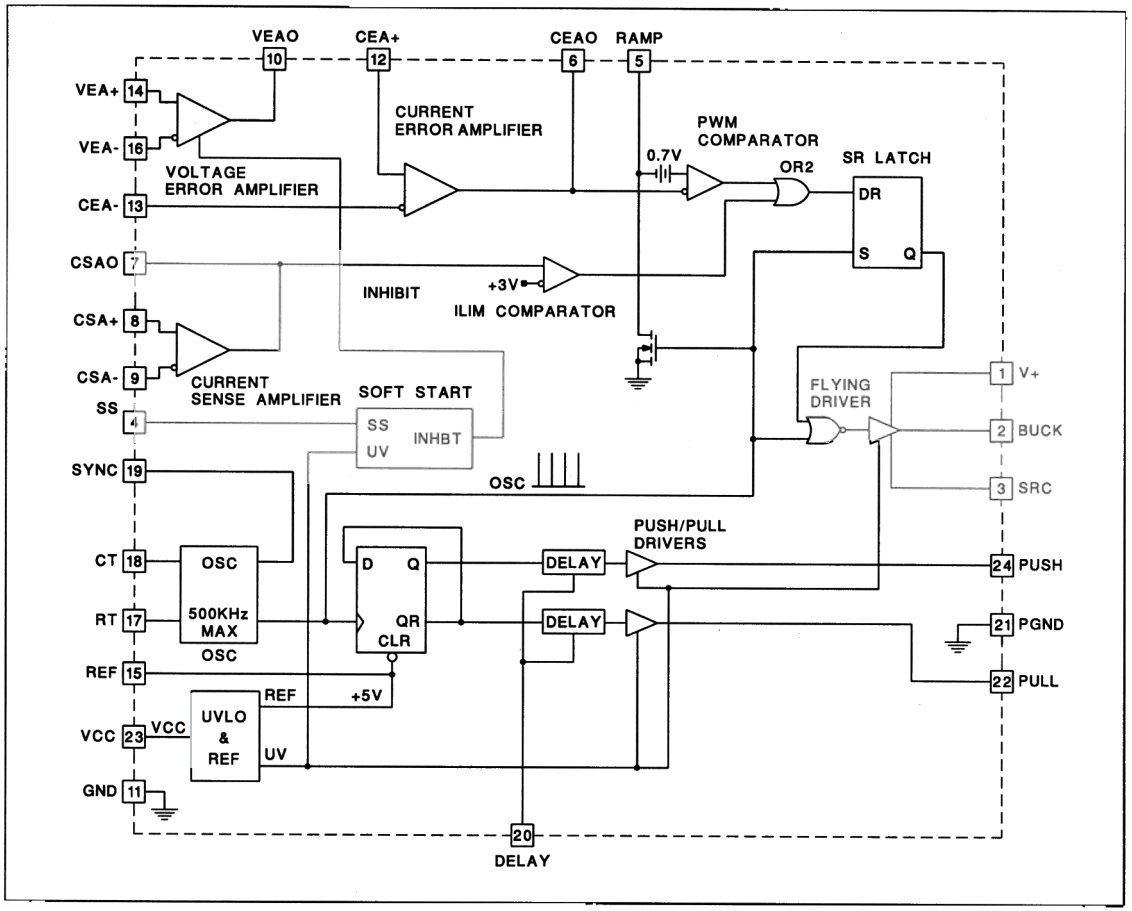


*Figure 17. UC3827 Block Diagram*

the ramp signal straight from the RAMP pin. The output of the PWM comparator determines the pulse width of the gate drive signal. An external MOSFET transistor is then turned on and off accordingly by the floating gate driver of the UC3827. The operating voltage of the floating driver can exceed the IC's bias supply, thus it can directly interface to an external switch up to 72V input voltage.

The converter's output voltage is regulated by the voltage error amplifier. Note, that all three amplifiers of the UC3827 are uncommitted amplifiers, i.e. all inputs and outputs are available. That makes the IC extremely adaptable to any control technique including voltage mode control with or without input voltage feedforward, voltage mode control with average current mode short circuit protection, traditional peak current mode control or even average current mode control. These different control techniques can be implemented by modifying the interconnections among the amplifier pins.

The different setup possibilities are depicted in the next few figures.

The first version as shown in Figure 18, is simple voltage mode control. The voltage error amplifier output is compared to the sawtooth waveform of the timing capacitor to determine the pulse width of the gate drive signal. Since the other two amplifiers are not used, their outputs are forced to a neutral state, not to influence the circuit operation. Accordingly, the current sense amplifier output is forced to ground while the current error amplifier output is forced high.

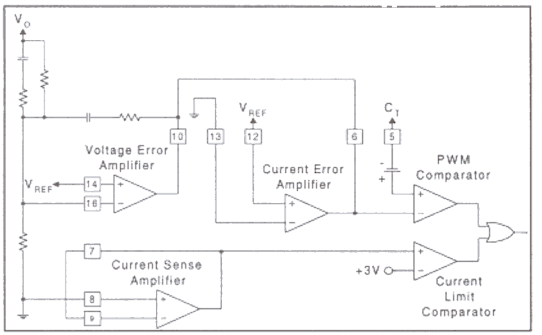


*Figure 18. Simple Voltage Mode Control*

Note, that the voltage and the current amplifier outputs are directly connected externally to the chip. The amplifiers of the UC3827 are designed with current limited asymmetrical outputs. The sink capability of the amplifiers is greater than their source capability. Therefore, OR connection of the amplifiers is possible without using diodes. This feature will be exploited several times later in other configurations. The advantages of voltage mode control are its simplicity and stable operation at light load when narrow duty-cycle is required. The disadvantages are that it can not protect the switches against excessive current stresses during overload condition and the output voltage is susceptible to rapid input voltage changes.

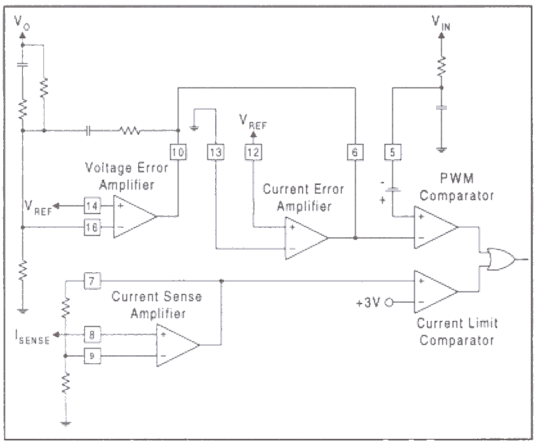


*Figure 19. Voltage Mode Control with Input Voltage Feedforward And Peak Current Limit*

The second arrangement in Figure 19, shows voltage mode control with input voltage feedforward and current protection of the main switch. For input voltage feedforward, the oscillator waveform is replaced by another sawtooth waveform, generated from the input voltage by a resistor and a capacitor. As shown in Figure 17, the ramp capacitor is discharged at the end of every switching cycle by an internal circuit driven from the clock synchronization pulse. Since the resistor is connected between the input voltage and the capacitor, the charge current of the capacitor varies with the input voltage producing a variable slope ramp signal. That signal is connected than to the RAMP pin providing the input voltage feedforward function. Current protection of the main switch is provided by the current sense amplifier and the current limit comparator. In this example, a positive polarity current sense signal is amplified by the current sense amplifier. The output of the current sense amplifier is compared to a 3V internal reference. If the current exceeds the level required to produce 3V at the output of the current sense amplifier, the gate drive signal is terminated immediately providing pulse-by-pulse primary side current limiting. This voltage mode method maintains the benefits of the previous one. Moreover, input voltage feedforward technique provides rejection of input voltage variation, while utilizing the current limit circuit can prevent catastrophic failures of the semiconductors.

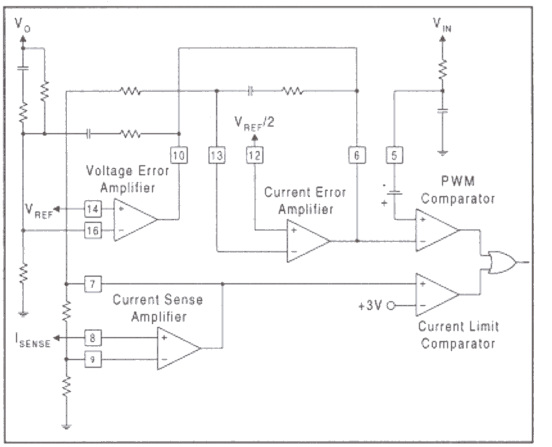


*Figure 20. Voltage Mode Control With Input Voltage Feedforward And Average Current Mode Overload Protection*

In Figure 20, another very popular voltage mode setup is displayed. In this version, two parallel control loops can be recognized. Under normal operation, the voltage loop which still incorporates input

voltage feedforward, determines the necessary pulse width. The voltage error amplifier is in its active mode while the current error amplifier idles. As the current increases in the converter the amplified current signal reaches the preset level on the noninverting input of the current error amplifier. At that point, the current loop takes over the duty cycle control and the voltage error amplifier becomes disengaged. In addition to all the benefits of the previous implementations, this circuit provides average current mode control during overload and short circuit condition when the voltage loop is open. That allows precise control of short circuit current and full protection of the entire circuit.

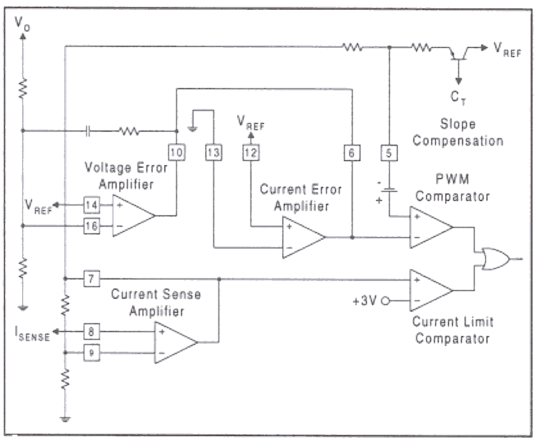


*Figure 21. Peak Current Mode Control*

In peak current mode control, the ramp pin receives the sum of the amplified current information and slope compensation as shown in Figure 21. The current sense amplifier is left in the circuit to allow using a low value current sense resistor and in order to utilize the whole control range of the amplifiers. Furthermore, the current limit comparator can provide additional current protection for the switching transistors. Note, that the compensation network around the voltage error amplifier is simplified accentuating the single pole transfer function of the power stage in current mode control. Peak current mode control offers simple voltage loop compensation, inherent input voltage feedforward and current protection. The known disadvantages are noise sensitivity, multiple control loops, the need of slope compensation and the troublesome operation under light load condition due to the leading edge spike in the current waveform.

Average current mode control is considered the ultimate control technique in power supply design. A typical implementation is demonstrated in Figure 22.

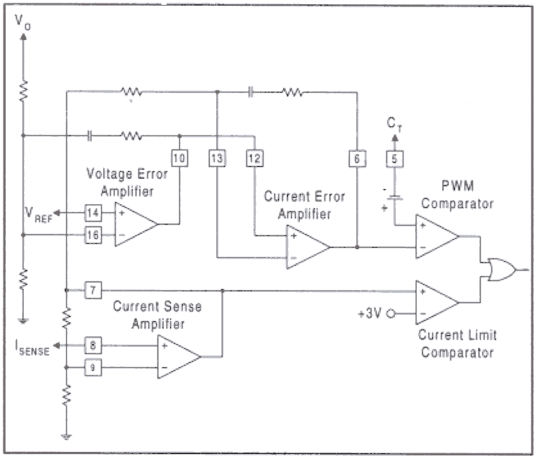


*Figure 22. Average Current Mode Control*

In this traditional setup, the voltage error amplifier processes the output voltage information through the feedback divider. The voltage error amplifier output signal, proportional to the voltage error, sets the reference value for the current error amplifier. The current error amplifier compares the amplified current signal to the voltage error signal and produces a current error voltage. This voltage, at the output of the current error amplifier is the control voltage for the PWM comparator. As Figure 22 reveals, the PWM comparator utilizes the timing capacitor waveform to determine the pulse width of the drive signal. Thus, average current mode control is less noise sensitive and more stable at light load than peak current mode control. Additional advantage of this technique is that slope compensation is not required for stable operation. As mentioned before, the major benefit using average current mode control is the precise control of the short circuit current and full protection of the entire circuit.

## UC3827-1 Setup

This application employs the UC3827-1 integrated circuit for simple, cost effective implementation of all control functions. The schematic diagram is detailed in Figure 23. Power to the IC is provided

through a low value resistor which forms a low pass filter with the IC's local energy storage capacitors. The VCC pin is filtered by an electrolytic and a parallel connected high frequency ceramic capacitors. The bootstrap supply for the floating driver has its own 1µF local ceramic bypass capacitor. The bootstrap diode, D5 separates the gate drive circuit from the ground referenced control section during the ON time of the buck MOSFET transistor. Note, that the floating driver has its gate current limiting resistor in the source return path. This technique is used extensively in all floating driver circuits because the source pin is inevitably forced to a negative potential when the freewheeling diode of the buck converter conducts. Placing the resistor to the source return lead, as shown in Figure 23, prevents the excessive negative voltage on the SRC pin and limits the current in those instances. The output drivers of the UC3827 are rated for 1A (BUCK) and 0.8A (PUSH and PULL) peak currents. Taking into consideration the internal gate resistances of the IRF3205s, 3Ω gate resistors are used in this design to limit power dissipation and to damp oscillations in the gate drive circuits.

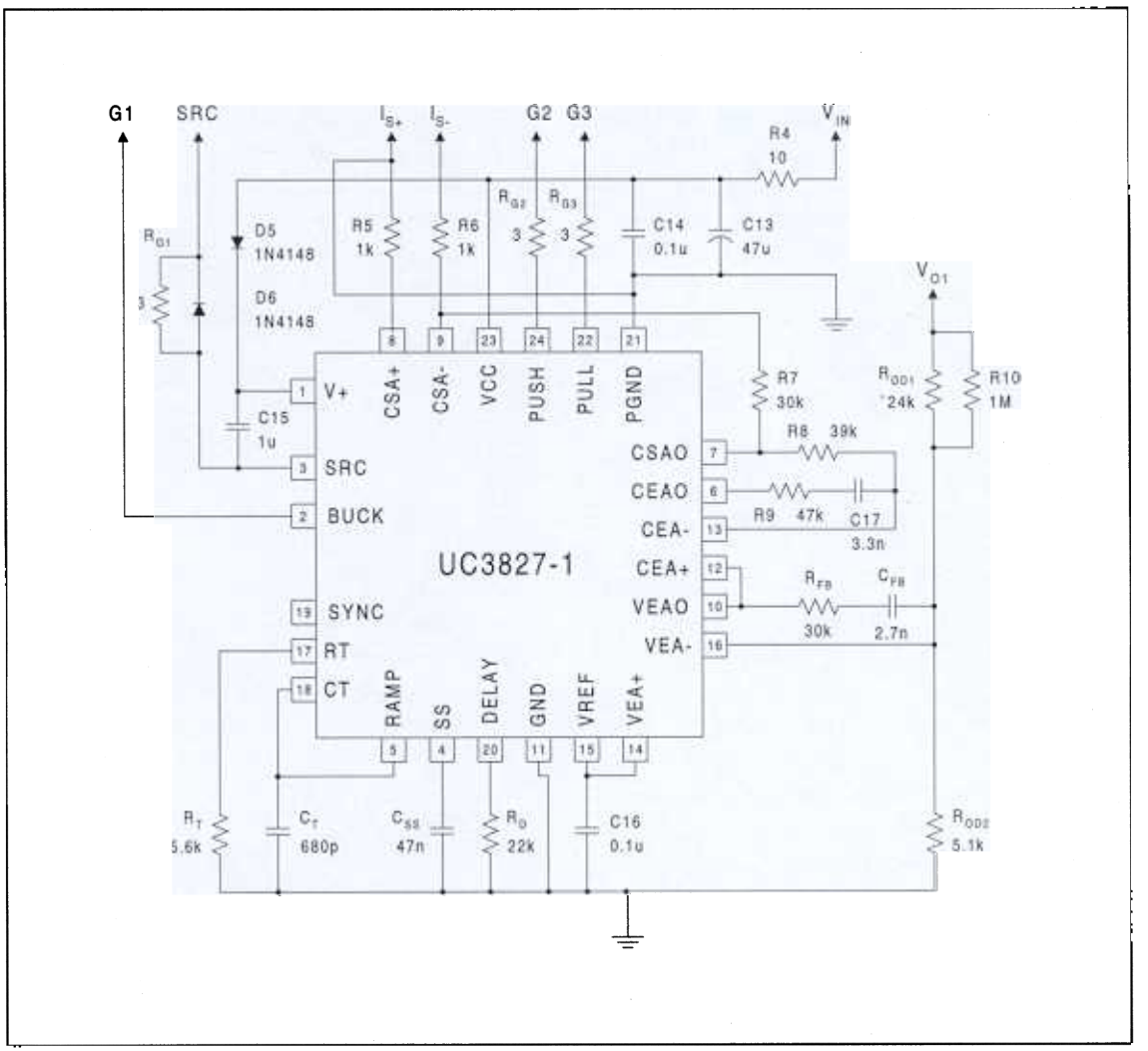


*Figure 23. Controller Schematic*

The clock frequency is set at the RT and CT pins of the UC3827. First the timing capacitor value is selected. It is important to keep in mind, that a stable clock is crucial for proper operation. Too small of a capacitor value will make the oscillator noise sensitive while too large of a value will increase power dissipation in the clock circuit and induce large current peaks in the sensitive analog circuitry during the discharge of $C_T$. This design uses a 680pF timing capacitor as a cautious compromise. The timing resistor value is calculated from the timing equation given in the datasheet:

$$R_T = \frac{0.77}{f_S \cdot C_T} \tag{42}$$

where $f_S$ is 200kHz, $C_T$ is 680pF and the equation yields a 5.6kΩ timing resistor.

Next the overlapping conduction time of the push-pull outputs are designed. Again, using the relationship from the datasheet:

$$R_D = t_D \cdot 150\frac{\Omega}{ns} \tag{43}$$

where $t_D$ is in nanoseconds. Using $t_D$=150ns, $R_D$ equals to 22.5kΩ.

The UC3827 incorporates a soft-start function. The ramp up time of the error amplifier output voltage depends on how quickly the soft-start capacitor is charged from approximately 0.3V to 3V which is the useful control range of that amplifier. Using the typical value of the soft start capacitor charge current, $I_{SS}$, the soft start interval equals:

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \cdot (3V - 0.3V) \tag{44}$$

Using a 0.047μF soft start capacitor gives approximately 10ms soft start duration.

The current sense amplifier gain is calculated from the $I_{MAX}$ and $R_{SENSE}$ values. The 3V threshold of the current limit comparator shall be triggered when $I_{MAX}$ is reached which requires a current sense amplifier gain of:

$$A_{CSA} = \frac{3V}{I_{MAX} \cdot R_{SENSE}} \tag{45}$$

yielding $A_{CSA}$=30.

Next the gain of the average current loop is investigated. The gain at the switching frequency can be defined using the slope matching technique as described in reference [3]. In this method, the representation of the buck inductor current downslope at the output of the current error amplifier is made equal (or smaller) to the slope of the timing capacitor voltage waveform. The maximum gain at the switching frequency can be obtain from:

$$A_{CEA,MAX} = \frac{\Delta C_T}{T} \cdot \frac{L}{V_{CT}} \cdot \frac{1}{R_{SENSE} \cdot A_{CSA}} \tag{46}$$

where $\Delta C_T$ is the amplitude of the timing capacitor waveform, T is the switching period, L is the buck inductor, $V_{CT}$ is the voltage on the center tap of the push-pull transformer during energy transfer, $R_{SENSE}$ is the current sense resistance and $A_{CSA}$ is the gain of the current sense amplifier. The result of (46) is $A_{CEA,MAX}$=1.75. The actual gain, as shown in Figure 23, is set by R9 and R8 to 47kΩ/39kΩ=1.2 to provide some margin for component tolerances and variation in operating conditions. The capacitor, C17 was added to the feedback loop of the amplifier to boost the DC gain of the amplifier. The zero introduced by C17 was placed to $f_Z$=1kHz. The required capacitance is given by:

$$C17 = \frac{1}{\omega_Z \cdot R9} \tag{47}$$

The resultant capacitor value is 3.3nF.

The feedback divider has to be calculated next. The noninverting input of the voltage error amplifier is directly connected to the 5V reference of the chip. Therefore, the feedback divider has to provide 5V at the noninverting input of the amplifier at nominal output voltage, $V_{O1}$=28V. Selecting the lower member of the divider, $R_{OD2}$=5.1kΩ, $R_{OD1}$ is defined as:

$$R_{OD1} = \frac{(V_{O1} - V_{REF})}{V_{REF}} \cdot R_{OD2} \tag{48}$$

For exactly 28V output voltage, $R_{OD1}$=23.46kΩ, which is realized by the parallel combination of a 24kΩ and a 1MΩ resistors.

Closing the voltage loop is the last step in the paper design phase. This article's primary focus is to give a practical design review, thus the loop stability analysis are omitted. For optimum loop design refer to reference [3], while a short-cut to a conservative solution with low crossover frequency of the voltage loop will be briefly explained here. For this simplified calculation, the first step is to simplify the outputs. The equivalent single output shall be normalized to the main output of the power supply then the equivalent output capacitor, ESR and load impedance values can be determined. Once the outputs are normalized to a single output rated to full power, the output impedances shall be transformed back to the primary side of the transformer. Be careful, the impedances transform by the square of the turns ratio. Now the problem is simplified to closing the voltage loop of a buck converter. If we take into consideration and assume that the average current loop is closed and stable, the control to output transfer function **at low frequencies** can be looked at as a voltage controlled current source ($G_M$ stage) with a gain of:

$$G_{M,CONTROL>OUTPUT} = \frac{I_{MAX}}{\Delta V_{EAO}} \qquad (49)$$

The $G_M$ stage is terminated by the transformed output capacitor in series with its ESR and by the load impedance as shown in Figure 24.

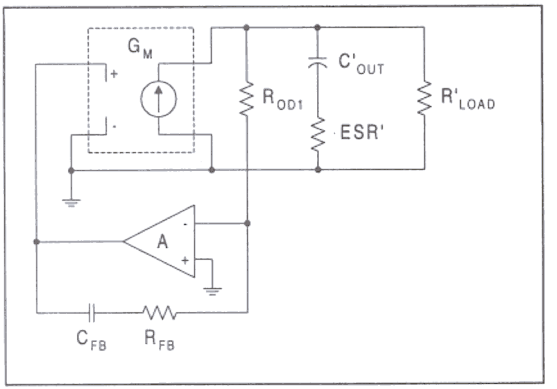


*Figure 24. Voltage Loop Equivalent Circuit*

From this equivalent circuit, the poles and zeros of the power stage are given and the compensation components of the voltage amplifier can be calculated. For a crossover frequency of $f_0$=2kHz, the required error amplifier gain at $f_0$ is approximately 2dB in this application, therefore the feedback resistor equals to $R_{FB}$=30kΩ.

The zero in the error amplifier's feedback path is placed close to the crossover frequency to increase the DC accuracy of the voltage regulation. The capacitor value is given as:

$$C_{FB} = \frac{1}{\omega_0 \cdot R_{FB}} \qquad (50)$$

which gives approximately $C_{FB}$=2.7nF.

Please, keep in mind, that this short-cut in closing the voltage loop works only at low frequencies i.e. when the voltage loop crossover frequency is in the couple of kilohertz range. This method does not account for any high frequency and second order effects nor the double pole at half of the switching frequency caused by the sampled data system.

## *Measurement Results*

This chapter highlights some of the measurement data obtained from the breadboard. First, a couple of the characteristic waveforms of the circuit are displayed. Figure 25 shows the switched waveform at the source of Q1 and the inductor current waveform. One of the push-pull transistor's voltage and current waveforms is shown in Figure 26. Figure 27 gives the waveforms at the anodes of the output rectifier diodes, D1, D2 and D3 respectively.

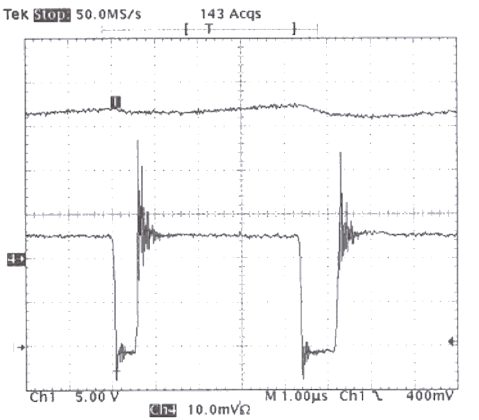


*Figure 25. Buck Transistor Voltage and Inductor Current (5A/div) Waveforms*

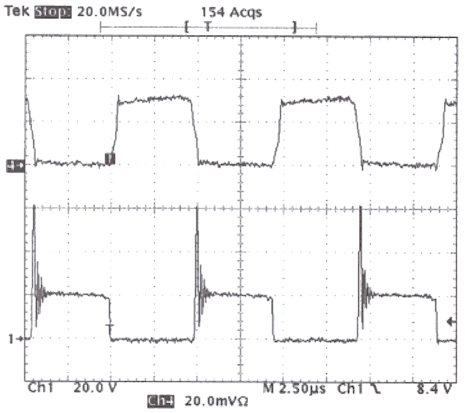


*Figure 26. Q2 Current (10A/div) and Voltage Waveforms*

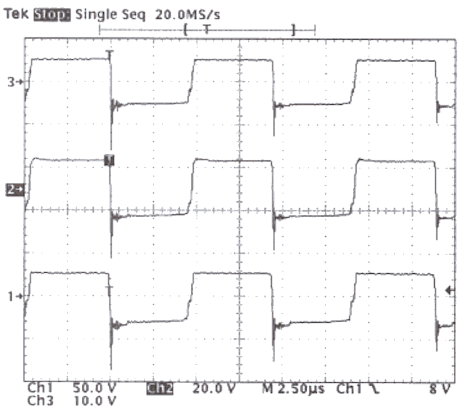


*Figure 27. D1, D2 and D3 Switching Waveforms*

The next three charts report cross regulation data. Figure 28 is the regulation of the 28V main output. Similar curves are generated for the two auxiliary outputs as shown in Figure 29 and Figure 30. The output regulation of $V_{O3}$ is very close to the predicted value. On the other hand, $V_{O2}$ performed worst than expected. The very likely cause of that relatively poor cross regulation behavior is the higher than expected resistances of N1 and N2, the 28V and 12V output windings of the prototype transformer. As Figure 31 shows, this effect also has an impact on the circuit efficiency demonstrated by the decreasing efficiency at higher load currents.

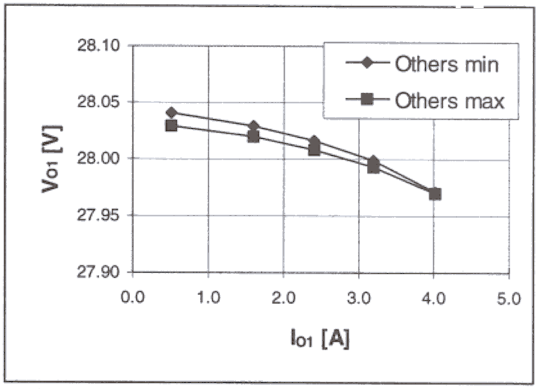


*Figure 28. $V_{o1}$ Line Regulation vs. Load Current*

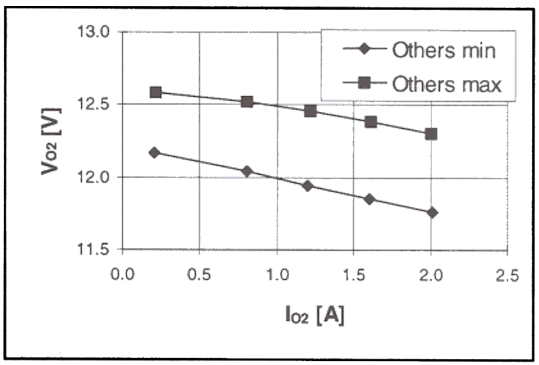


*Figure 29. $V_{o2}$ Line Regulation vs. Load Current*

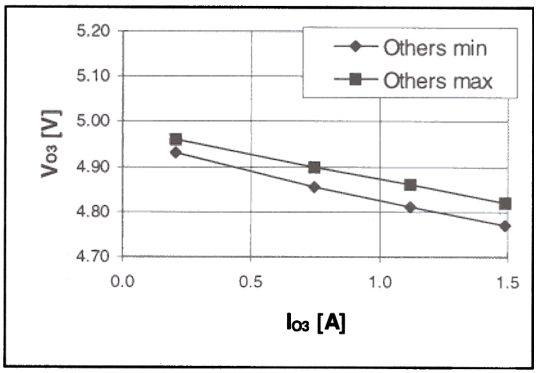


*Figure 30. $V_{o3}$ Line Regulation vs. Load Current*

The efficiency of the circuit is indicated in Figure 31. On the horizontal axis, the summed output power of all three outputs is normalized to the maximum output power of 143W.

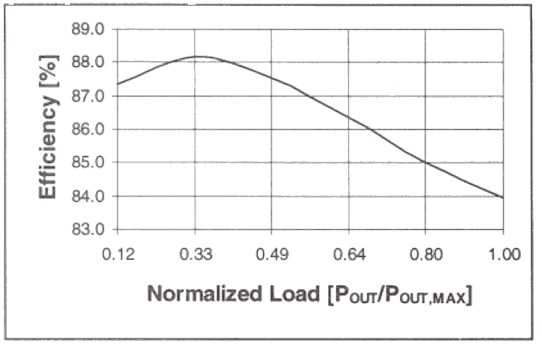


*Figure 31. Efficiency vs. Normalized Load*

As the graph shows, the efficiency peaks at about 88% then decreases due to the increasing resistive power losses. At full load, the efficiency is 84% which is close to the desired 85%. Once the circuit is built on a printed circuit board using the final planar magnetic components and optimized layout, it is very likely that the efficiency goal will be met.

## SUMMARY

This topic has presented the most frequently used topologies for multi-output power supply design. Pros and cons of each implementation have been listed in addition to the most popular application areas. The detailed design review of a three output current-fed push-pull converter culminated in the description of a step-by-step design procedure to insure meeting certain power supply specifications. The completed prototype circuit and the measurement results proved the effectiveness of the presented approach and the benefits of the selected topology.

## REFERENCES

[1] Spaziani, *"A Study of MOSFET Performance in Processor Targeted Buck and Synchronous Buck Converters"*, HFPC Power Conversion Conference, 1996, pp 123-137

[2] Carsten, *"Cross Regulation Effects In Multiple "Batch Regulated" Outputs"*

[3] Lloyd H. Dixon, *"Control Loop Cookbook"*, Unitrode Power Supply Seminar - SEM1100, Topic 5, 1996

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