A Fast Locking Scheme for PLL Frequency Synthesizers

National Semiconductor
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ABSTRACT

Frequency synthesizers are used in a large number of time division multiplexed (TDMA) and frequency hopping wireless applications where quickly attaining frequency lock is critical. A new frequency synthesizer is described which employs a scheme for reducing lock time by a factor of two using a conventional phase locked loop architecture. Faster lock is attained by shifting the loop filter's zero and pole corner frequencies while maintaining the PLL's gain/phase margin characteristics.

INTRODUCTION

RF system designers of TDMA based cellular systems, such as PHS, GSM and IS-54, need local oscillator (L.O.) or frequency synthesizer blocks capable of tuning to a new channel within a small fraction of each time slot. The suppression of reference spurs and phase noise is also critical for these modern digital standards. Base station and data transmission applications are now striving to utilize all the time slots available in each frame using a single synthesizer. This push towards a ''zero blind slot'' solution has put stringent demands upon the radio frontend's L.O. section.

The communication systems channel spacing determines the upper bound for the synthesizer's frequency resolution and loop filter bandwidth. More closely spaced channels dictate that the synthesizer's frequency resolution be finer, which in turn means the loop makes frequency corrections less often. A wider loop filter bandwidth would make it easier to attain lock within a given time constraint, but the price paid is less attenuation of the reference frequency sidebands and a higher integrated phase noise for the locked condition. An examination of the equations which govern the responsiveness of a closed loop system will provide some solutions to this dilemma.

CLOSED LOOP OPERATION

The basic phase-lock-loop configuration we will be considering is shown in *Figure 1*. The PLL consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2335TM, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. A passive loop filter configuration is desirable for its simplicity, low cost, and low phase noise.

The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency that sets the tuning resolution of the L.O. This reference signal, fr, is then presented to the input of a phase detector and compared with another signal, fp, the feedback signal, which was obtained by dividing the VCO frequency down by way of the N counter. The phase detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The phase/frequency comparators function is to adjust the voltage presented to the VCO until the feedback signals frequency (and phase) match that of the reference signal. When this ''phase-locked'' condition exists, the VCO's frequency will be N times that of the comparison frequency.

Increasing the value of the N counter by 1 will cause the phase comparator to initially sense a frequency error between the reference and feedback signals. The feedback loop responds and eventually shifts the VCO frequency to be N+1 times the reference signal. The VCO's frequency has in effect increased by the minimum tuning resolution of the PLL. The rate at which the transition to the new operating frequency occurs is determined by the closed loop gain and stability criteria.

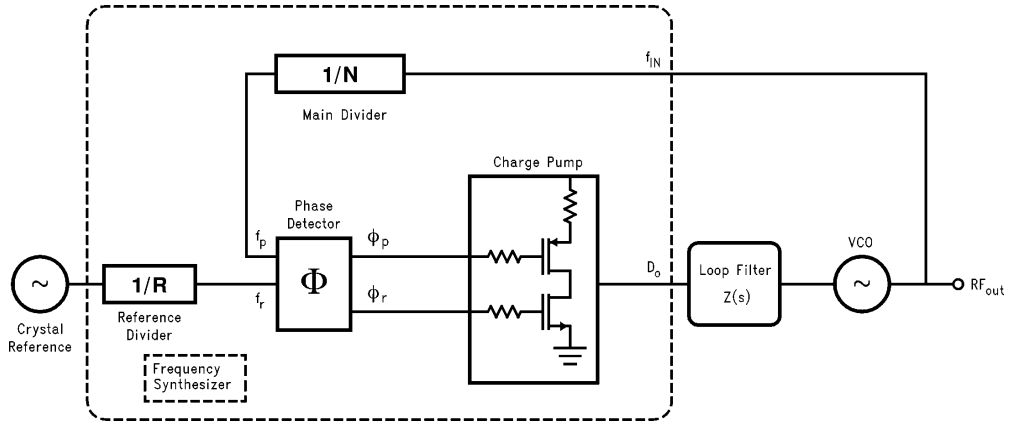

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FIGURE 1. Conventional PLL Architecture

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LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (Kϕ), the VCO gain (Kvco/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in equation 2. [Ref 5]

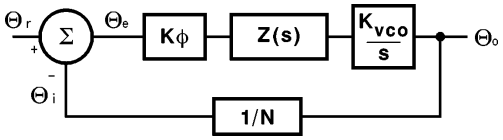

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FIGURE 2. PLL Linear Model

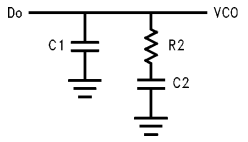

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FIGURE 3. Passive Loop Filter

$$\text{Open loop gain} = H(s)\,G(s) = \Theta i/\Theta e = K\phi\, Z(s)\, Kvco/Ns \quad (1)$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2 (C1 \bullet C2 \bullet R2) + s\,C1 + s\,C2)} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3a)$$

and

$$T2 = R2 \bullet C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants Kϕ, Kvco, and N.

$$G(s) \bullet H(s)\Big|_{s = j\bullet\omega} = \frac{-K\phi \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\, C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (5)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45°. Given the pressure to minimize lock time, the cutoff frequency of the loop would be selected just wide enough to suppress the PLL's reference frequency spurs to a tolerable level.

If we were now to redefine the cut off frequency, ω_p', as double the frequency which gave us our desired level of spurs, ω_p, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed FastLock™ scheme, the higher spur levels and wider loop filter conditions would ex ist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "$1/\omega$" or "$1/\omega^2$" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "ω" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at $\omega_p' = 2\,\omega_p$. Kvco, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract the ω^2 term present in the denominator of equation 3. Altering Kvco could be difficult at best, however, both N and Kϕ gain terms are readily available in an integrated PLL IC. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in FastLock. Changing the N gain term could also have been chosen to accomplish our objective. In fact, doing so causes the PLL's reference frequency to be pushed over in the frequency domain along with the loop cutoff frequency. Unfortunately changing N also means changing the R counter value by the same factor. And while this is feasible, it probably means employing fractional counter techniques along with all the associated problems of this approach, as an N/4 term may no longer be an integer.

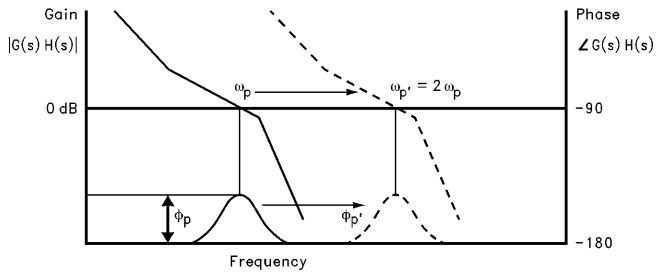

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FIGURE 4. Open Loop Response Bode Plot

CIRCUIT IMPLEMENTATION

A diagram of the FastLock scheme as implemented in National Semiconductors LMX2335 PLL is shown in *Figure 5*. When a new frequency is loaded, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second resistor element, R2, to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the PLL will then return to standard, low noise operation. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between FastLock and standard mode.

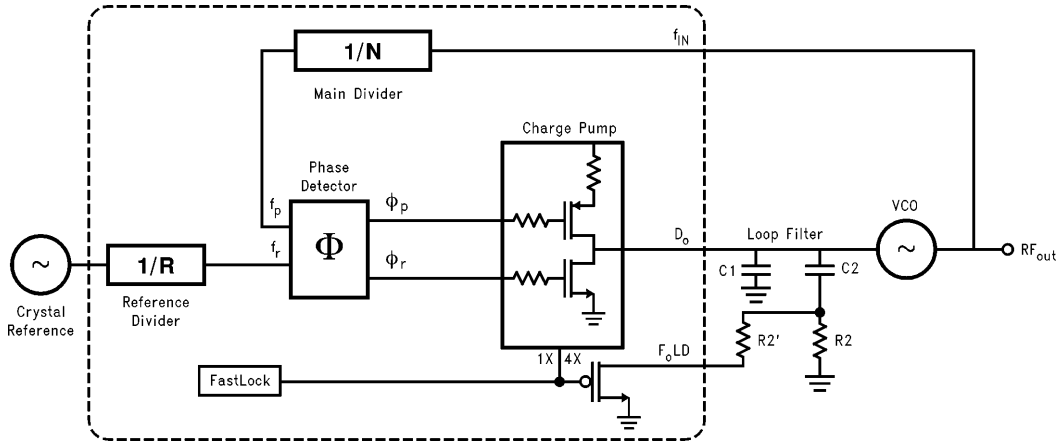

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FIGURE 5. FastLock PLL Architecture

RESULTS

An LMX2335 PLL was utilized to address the following IS-54 application constraints:

$$Fvco = 900\ MHz, \quad Kv = 20\ MHz/V,$$

$$Channel\ spacing = 30\ kHz.$$

The PLL's device attributes were as follows:

$$K\phi = 1\ mA/2\pi, \quad N = 30{,}000,$$

$$Fref = 30\ kHz, \quad Fo = 3\ kHz.$$

The loop filter values used were:

$$C1 = 1800\ pF, \quad R2 = 12\ k\Omega, \quad C2 = 0.012\ \mu F$$

The modulation domain analyzer graphs in *Figures 6–9* show the transient lock responses for the normal 1 mA mode condition side by side with the response for the FastLock mode. The FastLock operation in *Figure 9* shows lock being attained within 1 ms (to within ± 1 kHz) for a frequency jump of 50 MHz, compared with 1.8 ms for the standard condition *(Figure 8)*. As much as a 2 kHz frequency disturbance can result when switching back to normal operation after steady state is fully attained. By switching out of the FastLock mode when the PLL has settled to near the desired frequency tolerance, almost the entire 2X increase in lock time can be achieved.

SUMMARY

The FastLock circuitry of the LMX2335 frequency synthesizer provides a means of improving TDMA channel switching speed, without compromising reference spur quality or phase noise. Zero blind slot RF synthesizer designs can more easily be attained through this technique.

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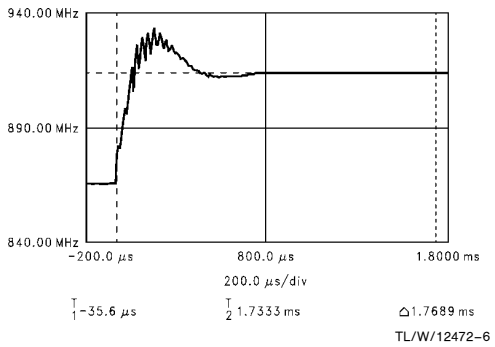

FIGURE 6. Normal Switching Waveform

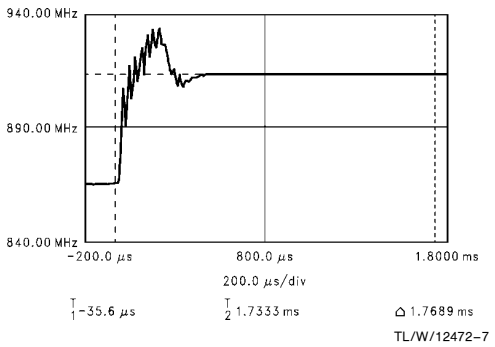

FIGURE 7. FastLock Switching Waveform

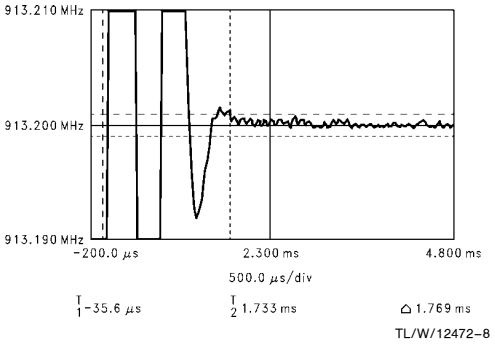

FIGURE 8. Normal Mode Lock Time

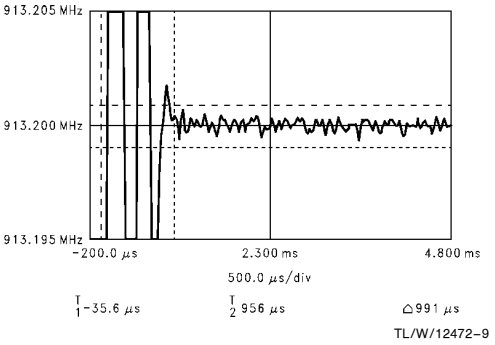

FIGURE 9. FastLock Mode Lock Time

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